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Master's thesis presented to the Graduate Program in Electrical Engineering of the Santa Catarina State University, as requirement for obtention of the title of Master in Electrical Engineering, concentration area of Electronic Systems.
Supervisor: Yales Rômulo de Novaes, Dr.
Co-supervisor: Sandro Guenter, Dr.

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ABSTRACT

The Dual Active Bridge (DAB) is a DC-DC power converter which offers bidirectional power flow, galvanic isolation and natural soft-switching. Such characteristics are interesting for applications like electric vehicles, energy storage systems and DC distribution/transmission grids. In this Master's thesis, an in-depth circuit analysis of the DAB converter employing its simplest modulation (Single Phase-Shift) is done, presenting steady-state waveforms, deriving equations of important parameters for converter design and explaining concepts like circulating power and soft-switching. A 600 W prototype is built for experimental validation of the mathematical model. Furthermore, an automatic algorithm for the Dual Phase-Shift modulation named mCSPT is proposed for reducing the current stress in the transformer and the power switches. The algorithm is validated by both simulation and experimental results.

Keywords: Dual Active Bridge; Single Phase-Shift; Dual Phase-Shift; Algorithm; Current Stress.

RESUMO

O *Dual Active Bridge* (DAB) é um conversor estático CC-CC que oferece fluxo de potência bidirecional, isolação galvânica e comutação suave natural. Tais características são interessantes para aplicações como veículos elétricos, sistemas de armazenamento de energia e redes CC de distribuição/transmissão de energia elétrica. Nesta dissertação, uma profunda análise da topologia é feita do conversor DAB empregando sua modulação mais simples (*Single Phase-Shift*), apresentando formas de onda em regime permanente, deduzindo equações de importantes parâmetros para projeto do conversor e explicando conceitos como potência circulante e comutação suave. Um protótipo de 600 W é construído para validar experimentalmente a teoria. Além disso, um algoritmo automático para a modulação *Dual Phase-Shift* nomeado de mCSPT é proposto para reduzir os esforços de corrente no transformador e nos interruptores de potência. O algoritmo é validado tanto por resultados de simulação quanto experimentais.

Palavras-chave: *Dual Active Bridge*; *Single Phase-Shift*; *Dual Phase-Shift*; Algoritmo; Esforços de Corrente.

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LIST OF ABBREVIATIONS AND ACRONYMS

NASA	National Aeronautics and Space Administration
IPCC	Intergovernmental Panel on Climate Change
CO_2	Carbon Dioxide
IEA	International Energy Agency
EIA	United States Energy Information Administration
BESS	Battery Energy Storage System
IRENA	International Renewable Energy Agency
EV	Electric Vehicles
V2G	Vehicle to Grid
DC	Direct Current
AC	Alternate Current
DAB	Dual Active Bridge
PWM	Pulse Width Modulation
ZVS	Zero Voltage Switching
MEA	More Electric Aircrafts
SST	Solid State Transformer
RMS	Root Mean Square
SPS	Single Phase-Shift
EPS	Extended Phase-Shift
DPS	Dual Phase-Shift
TPS	Triple Phase-Shift
PS	Phase-Shift
LV	Low Voltage
MV	Medium Voltage
HV	High Voltage
NPC	Neutral Point Clamped
ISOP	Input Series Output Parallel
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
5LDAB	5 (Five) Level Dual Active Bridge
DSP	Digital Signal Processor
ANPC	Active Neutral Point Clamped

Si	Sillicon
SiC	Sillicon Carbide
GaN	Gallium Nitride
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
PFC	Power Factor Correction
G2V	Grid to Vehicle
ZCS	Zero Current Switching
PCB	Printed Circuit Board
mCSPT	Minimum Current Stress Point Tracking
ADC	Analog-to-Digital Converter
IIR	Infinite Impulse Response

LIST OF SYMBOLS

V_i	Input Voltage [V]
V_o	Output Voltage [V]
n	Transformer Turns Ratio
K	Voltage Conversion Ratio
L	Inductance [H]
C_i	Input Capacitance [F]
C_o	Output Capacitance [F]
T	Transformer
P_x	Power Switch “x” of the Primary Bridge
S_x	Power Switch “x” of the Secondary Bridge
ϕ	External Phase-Shift [rad]
N_1	Number of Turns on the Primary Side of the Transformer
N_2	Number of Turns on the Secondary Side of the Transformer
v_{ab}	Output Voltage of Primary Bridge [V]
v_{cd}	Output Voltage of Secondary Bridge [V]
v'_{cd}	Output Voltage of Secondary Bridge Referred to the Primary [V]
i_i	Input Current [A]
i_L	Inductor Current [A]
i_o	Output Current [A]
T_s	Switching Period [s]
t	Time [s]
t_x	Time Instant “x” [s]
V'_o	Output Voltage Referred to the Primary [V]
i_1	Primary Side Transformer Current [A]
i_2	Secondary Side Transformer Current [A]
φ_i	Phase Angle of the Input Voltage Source [°]
φ_o	Phase Angle of the Output Voltage Source [°]
P_i	Input Power [W]
P_o	Output Power [W]
I_1	Switching Current 1 (value of inductor current at instant t_1) [A]
I_2	Switching Current 2 (value of inductor current at instant t_2) [A]

f_s	Switching Frequency [Hz]
P	Power Transmission [W]
P_b	Base Value of Power Transmission [W]
$\bar{P}$	Normalized Power Transmission [p.u.]
$I_{2,rms}$	RMS Value of Secondary Side Transformer Current [A]
$I_{L,rms}$	RMS Value of the Inductor Current [A]
$I_{L,b}$	Base Value of RMS Value of the Inductor Current [A]
$\overline{I_L}$	Normalized RMS Value of the Inductor Current [p.u.]
I_i	Average Value of the Input Current [A]
$I_{i,rms}$	RMS Value of the Input Current [A]
I_o	Average Value of the Output Current [A]
$I_{o,rms}$	RMS Value of the Output Current [A]
Q_c	Circulating Power [W]
$V_{ab,rms}$	RMS Value of Voltage Between Nodes “a” and “b” [V]
$I_{ab,rms}$	RMS Value of Current Between Nodes “a” and “b” [A]
Q_T	Transformer Reactive Power [var]
D_T	Transformer Distortion Power [VA]
N_T	Transformer Non-Active Power [VA]
S_T	Transformer Apparent Power [VA]
$S_{T,f}$	Transformer Apparent Power by Fundamental Component [VA]
I_P	Average Value of Current in Unidirectional Switch “P” [A]
I_{DP}	Average Value of Current in Diode of Power Switch “P” [A]
I_S	Average Value of Current in Unidirectional Switch “S” [A]
I_{DS}	Average Value of Current in Diode of Power Switch “S” [A]
$I_{P,rms}$	RMS Value of Current in Unidirectional Switch “P” [A]
$I_{DP,rms}$	RMS Value of Current in Diode of Power Switch “P” [A]
$I_{S,rms}$	RMS Value of Current in Unidirectional Switch “S” [A]
$I_{DS,rms}$	RMS Value of Current in Diode of Power Switch “S” [A]
P_R	Rated Power [W]
ϕ_R	Rated Phase-Shift [rad]
v_c	Capacitor Voltage [V]
i_C	Capacitor Current [A]

i_{C_o}	Output Capacitor Current [A]
ΔV_o	Output Voltage Ripple [V]
$I_{C_o,rms}$	RMS Value of Output Capacitor Current [A]
C_1	Series Capacitance in the Primary Bridge [F]
C_2	Series Capacitance in the Secondary Bridge [F]
v_{C_1}	Voltage of the Capacitor C_1 [V]
v_{C_2}	Voltage of the Capacitor C_2 [V]
f_{LC}	Resonant Frequency [Hz]
C	Capacitance [F]
V_{max}	Maximum/Peak Voltage [V]
V_{min}	Minimum Voltage [V]
ΔV_C	Voltage Ripple in the Series Capacitor C_1 [V]
V_{max,C_1}	Maximum Voltage of the Capacitor C_1 [V]
V_{max,C_2}	Maximum Voltage of the Capacitor C_2 [V]
ϕ_a	Applied External Phase-Shift Angle [rad]
ϕ_{dt}	External Phase-Shift Angle for Compensating Dead-time [rad]
ϕ_{db}	Full Dead-time Phase-Shift Angle [rad]
T_{dt}	Dead-time Period [s]
$\bar{I_1}$	Normalized Switching Current I_1 [p.u.]
$\bar{I_2}$	Normalized Switching Current I_2 [p.u.]
K_{PB}	Boundary Value of K for ZVS Region in the Primary Bridge
K_{SB}	Boundary Value of K for ZVS Region in the Secondary Bridge
$\bar{P}_{PB}$	Normalized Power Transmission Boundary Value of ZVS Region in the Primary Bridge [p.u.]
$\bar{P}_{SB}$	Normalized Power Transmission Boundary Value of ZVS Region in the Secondary Bridge [p.u.]
I_{ZVS}	Minimum Inductor Current Value at Switching Instant Necessary for ZVS [A]
V_Q	Voltage Over Power Switch [V]
m	Number of Turned-On Power Switches
C_P	Output Capacitance of Power Switch in the Primary Bridge [F]
C_S	Output Capacitance of Power Switch in the Secondary Bridge [F]

$I_{ZVS,P}$	Minimum Inductor Current Value at Switching Instant Necessary for ZVS in the Primary Bridge [A]
$I_{ZVS,S}$	Minimum Inductor Current Value at Switching Instant Necessary for ZVS in the Secondary Bridge [A]
$t_{ZVS,P}$	Minimum Dead-Time Necessary for ZVS in the Primary Bridge [s]
$t_{ZVS,S}$	Minimum Dead-Time Necessary for ZVS in the Secondary Bridge [s]
Q_{C_P}	Charge of Capacitor C_P [C]
Q_{C_S}	Charge of Capacitor C_S [C]
L_M	Magnetizing Inductance [H]
L_{dab}	External/Discrete Inductance [H]
l_1	Transformer Leakage Inductance on the Primary Side [H]
l_2	Transformer Leakage Inductance on the Secondary Side [H]
l_2'	Secondary Side Leakage Inductance Referred to Primary [H]
t_f	Power Switch Current Fall Time [s]
$P_{sw,off}$	Turn Off Switching Loss [W]
$V_{f,igbt}$	Estimated Voltage Drop of Collector-Emitter Channel of IGBT [V]
$R_{ce,igbt}$	Estimated Resistance of Collector-Emitter Channel of IGBT [Ω]
$P_{on,ce}$	Conduction Loss of Collector-Emitter Channel of IGBT [W]
$V_{f,D}$	Estimated Forward Voltage of Diode [V]
R_D	Estimated Resistance of Diode [Ω]
$P_{on,D}$	Conduction Loss of Diode [W]
T_j	Junction Temperature [°C]
T_a	Ambient Temperature [°C]
R_{cd}	Thermal Resistance of Case-to-Heatsink [°C/W]
R_{jc}	Thermal Resistance of Junction-to-Case [°C/W]
R_{da}	Thermal Resistance of Heatsink-to-Ambient [°C/W]
T_{hs}	Heatsink Temperature [°C]
C_{oss}	IGBT Output Capacitance [F]
$\phi_{ZVS,P}$	Minimum Phase-shift Required for ZVS [rad]
$P_{ZVS,P}$	Minimum Power Required for ZVS [W]
$L_{dab,meas}$	External Inductance Measured [H]
L_{meas}	Total Inductance Measured [H]

$\phi_{R,new}$	Adjusted Rated Phase-Shift [rad]
$v_{ab\sim}$	Alternating Component of Voltage v_{ab} [V]
$v_{cd\sim}$	Alternating Component of Voltage v_{cd} [V]
$v_{ab\sim,rms}$	RMS Value of Voltage $v_{ab\sim}$ [V]
$v_{cd\sim,rms}$	RMS Value of Voltage $v_{cd\sim}$ [V]
$v_{ce,P1}$	Collector-Emitter Voltage of Power Switch P_1 [V]
$v_{be,P1}$	Base-Emitter Voltage of Power Switch P_1 [V]
I_S	Average Value of the Input Source Current [A]
i_{Ro}	Load Current [A]
$I_{1,sec}$	Switching Current I_1 Referred to Secondary Side [A]
$I_{2,sec}$	Switching Current I_2 Referred to Secondary Side [A]
I_{Ro}	Average Value of Load Current [A]
ϕ_{int}	Internal Phase-Shift [°]
I_{zp}	Zero Active Power Current [A]
ΔT_{zp}	Zero Active Power Period [s]
$I_{L,pk}$	Peak Value of Inductor Current [A]
P_{ref}	Reference Value for Power Transmitted [W]
ϕ_i	Initial Value of External Phase-shift [°]
ϕ_f	Final Value of External Phase-shift [°]
$\phi_{int,i}$	Initial Value of Internal Phase-shift [°]
$\phi_{int,f}$	Final Value of Internal Phase-shift [°]
$\Delta\phi$	Step Value of External Phase-shift [°]
$\Delta\phi_{int}$	Step Value of Internal Phase-shift [°]
$V_{o,ref}$	Reference Value for Output Voltage [V]
V_{tol}	Tolerance Voltage for mCSPT [V]
T_w	Waiting Period for mCSPT [s]
S_i	Input Apparent Power [VA]
$S_{i,b}$	Base Value of Input Apparent Power [VA]
$\overline{S_i}$	Normalized Input Apparent Power [p.u.]
S_o	Output Apparent Power [VA]
Q	Reactive Power [var]
D	Distortion Power [VA]

N	Non-Active Power [VA]
N_i	Input Non-Active Power [VA]
Q_i	Input Reactive Power [var]
∀	For All
∧	And

CONTENTS

1 INTRODUCTION

Amid environmental concern and rising global temperatures due to human activities (Copernicus, 2025), replacing technology that relies on fossil fuel – coal, oil and natural gas, which contributes to climate change (IPCC, 2021) – with “greener” alternatives is paramount to prevent even higher temperatures and preserve life on the planet (IPCC, 2018).

Electricity generated by coal and natural gas still represents around half of the world’s generation (IEA, 2024a). Even though there has been significant growth recently, renewable energy must be tripled by 2030 to keep on track of the goals defined in the Paris Agreement (IEA, 2023a). In the next years, solar and wind energy are expected to represent most of the new installed capacity of all renewable energies (IEA, 2024b).

In this context, some emerging technologies are promising in society’s quest to attain a cleaner future with renewable energy, such as Electric Vehicles (EV) and Battery Energy Storage Systems (BESS). Although these concepts have already been presented in the past, only now they are financially viable for implementation, especially due to recent advances that allows for cheaper, smaller and lighter batteries.

Solar and wind are better utilized if linked to BESSs, given its intermittent nature: solar energy is only converted during the day and wind energy can only be converted when there is enough wind to turn the turbines. Storing this energy for usage when nothing can be generated or if excess energy is converted is essential. Moreover, BESSs can help ease the grid during high demand peaks (Segaran, 2013). The International Renewable Energy Agency (IRENA) estimates it will be necessary around 359 GW of capacity from BESSs around the world by 2030 to fulfill Paris Agreement’s goals (IRENA, 2023).

EVs use electric motors, meaning there is zero carbon emission when driving (provided that the electricity comes from renewable energies). It is also much more efficient than internal combustion engine cars, which depend on oil. In 2022, global EV sales were slightly more than 10 million. However, to reach carbon emission goals, sales in 2030 should be around 59 million, corresponding to a 67% share of global vehicle sales (IEA, 2024c).

EVs can be viewed as mobile BESSs, meaning the energy stored in the batteries can be used for other applications, like injecting it back to the grid - known as Vehicle to Grid (V2G) - or supply power to an electrical equipment (Safayatullah *et al.*, 2022).

To enable EVs as the main type of transportation, improvements on the grid must be made to deal with the larger power peak demand. Furthermore, fast charging stations of high power must be installed in cities, highways and countryside, to guarantee that EVs can be recharged faster during a long trip, compared to low power recharging of residences, workplaces and commercial buildings that takes hours to fully recharge (Safayatullah *et al.*, 2022; Jung, 2017).

Wind turbines generate electricity in Alternate Current (AC) but must be rectified into Direct Current (DC) to deal with variable frequency caused by the unpredictable nature of the wind. Solar panels generate electricity in DC. In this manner, the use of renewable energy can promote the development of DC transmission and distribution networks, increasing the efficiency in a system where most sources and loads are of DC nature (Ertugrul, 2024).

DC grids facilitate the connection of different sources on the grid, since there is no need for phase/frequency synchronism, although the short circuit detection and extinction gets harder (Dujic, 2023). Moreover, DC grids may use only two conductors (instead of three in a three-phase AC grid), which reduces the amount of copper used in transmission lines, since an increase in its demand is expected (IEA, 2023b, 2023c).

Power Electronics plays a key role in this energy transition. Most of the world’s electricity runs through power converters (Ertugrul, 2024), since each equipment/application has different requirements of voltage and current. Essentially, power converters interface sources and loads to adequate voltage/current levels or type (AC/DC) between them, which is done by controlling the electrical current flow. Thus, making sure loads can be powered properly.

Improving power converters leads to several benefits for society: higher efficiency means less electrical energy loss and smaller batteries needed; reduction in volume, weight and number of components means less materials used; better reliability means less components are damaged and longer converter/equipment availability.

As for the emerging technologies mentioned previously, a DC-DC converter is crucial for enabling their operation. This converter takes a DC voltage from an input source and can step up or step down the voltage level to the output load. Equal input and output voltages are also possible.

Furthermore, these converters can offer galvanic isolation by utilizing medium/high frequency transformers (> 1 kHz), resulting in much lighter and smaller transformers than the low frequency transformer (50/60 Hz), providing safety to users (Zhao *et al.*, 2014; Kenzelmann *et al*., 2015).

For BESSs, a bidirectional DC-DC converter, which allows current to flow in both ways, is used to adequate voltage levels between the system and the grid, as well as allowing charging and discharging of the batteries.

In EVs, DC-DC converters are used to charge the batteries and to provide a DC bus for the traction inverter and other auxiliary loads, like electronic control units and sensors. Low power charging is done by the on-board charger, in which high power density is required. For high power charging (>20 kW), the charger is off-board, meaning it is located outside the vehicle, i.e., in the fast charging station (Safayatullah *et al.*, 2022).

If the charger is unidirectional, it is only possible to supply energy from the grid to the vehicle, known as Grid to Vehicle (G2V), because the current can only flow in one direction. To use the energy stored in the batteries for other purposes, e.g., V2G mode, a bidirectional converter must be used. Galvanic isolation is desired for meeting safety standards, either for on-board or off-board chargers. Storing energy from regenerative breaks also requires a bidirectional converter (Safayatullah *et al.*, 2022).

DC grids require bidirectional DC-DC converters to interface the multiple energy sources (wind, solar, fuel cell), energy storages (batteries, supercapacitors) and loads (Segaran, 2013). Galvanic isolation is also desirable for interconnecting different DC grids.

More Electric Aircrafts (MEA) may have their own DC microgrid. This system is composed of generators, loads and energy storage systems (batteries, supercapacitors). Hence, bidirectionality is essential to manage the power flow. Galvanic isolation is also required by standards, such as the MIL-STD-704F. High

power density is vital for aircrafts (and other EVs), since it has very limited space and weight capacity (Buticchi; Costa; Liserre, 2017).

In this context, the Dual Active Bridge (DAB) is a DC-DC converter that stands out. Initially, it was proposed for aerospace power systems. However, research interest in the converter has skyrocketed because of its main characteristics: bidirectionality, galvanic isolation, modularity, inherent soft switching, high power processing and high power density, making it a suitable choice for the emergent technologies (De Doncker; Divan; Kheraluwala, 1991; Zhao *et al.*, 2014). Thus, it is chosen as the subject for this Master's thesis.

The bigger challenges that need to be overcome for consolidation of the DAB converter are the large reactive power and loss of soft switching when the converter operates with a wide voltage range and under light load, which reduces efficiency (Shao *et al.*, 2019), although this problem is inherent to any converter that operates with soft switching.

1.1 GENERAL GOAL

There are two general goals for this Master's thesis: the first one is to establish an academic reference with a comprehensive and easy to understand analysis that covers all of the important aspects of the DAB converter. The second one is to develop an algorithm using Dual Phase-Shift modulation to minimize the current stress in the transformer and in the power switches for evaluation of the converter efficiency. Also, it should be easy to implement.

1.2 SPECIFIC GOALS

The specific goals established for achieving the general goals are:

- Research the design challenges of the DAB converter considering different applications.
- Analyze the circuit operation of the converter employing the simplest modulation (Single Phase-Shift).

- Verify important aspects such as transformer apparent power, circulating power and soft-switching operation and their impact on the converter operation.
- Establish a mathematical model for the design of the main components of the converter.
- Build and test a prototype to verify if the experimental measurements match the operation described theoretically.
- Analyze the operation of the converter employing the Dual Phase-Shift modulation.
- Investigate the impact of the control variables on the transformer current when the converter operates in a condition when there is a period with no active power being transferred.
- Propose, develop and experimentally test a way to automatically reduce the current stress in the transformer and in the power switches.

1.3 CONTRIBUTIONS

The contribution of this Master's thesis is summarized as follows:

- Proposes a simple and automatic digital algorithm for reducing the current stress in the transformer and power switches for the Dual Phase-Shift modulation.

1.4 THESIS SCOPE

The research and study done in this Master's thesis is limited by the following points:

- The topology of the Dual Active Bridge converter for the literature review and the circuit analysis is the single-phase, voltage fed and non-resonant topology, with the active bridge configuration being a standard full-bridge.

- The theoretical analysis of the converter considers only ideal components. Parasitic components are not considered in any equation derived (except for soft-switching).
- The thesis does not provide analyses and neither equations for designing and building the magnetic components of the converter.
- The algorithm proposed is developed and tested for the specific condition of when the external phase-shift is lower than the internal phase-shift of the Dual Phase-Shift modulation. Moreover, it is supposed to be used as an additional feature for the main control system of the converter, since it needs initial input values. Lastly, the algorithm is supposed to execute when the converter is operating in steady-state, and for the sake of simplifying the tests, it does not detect if the load changes during its execution.

1.5 THESIS STRUCTURE

The next chapters of this thesis have the following content:

Chapter 2 presents a review of many papers read during the study of the DAB converter, mixing the converter's characteristics and state-of-the-art techniques published. It is intended as an overview of various important topics, so the reader can have a glimpse of some aspects regarding the converter's operation in a qualitative manner.

Chapter 3 presents a detailed analysis of the fundamental concepts for the DAB converter, considering Single Phase-Shift modulation. Mathematical expressions for many converter parameters are derived for understanding and aiding the converter design.

Chapter 4 presents the design methodology of a 600 W prototype for experimental validation of the circuit analysis presented in previous chapters. The converter is designed for a 380 V to 380 V voltage conversion. Besides the main equations for designing the converter, the chapter contains the technical specifications of the active bridge PCBs and magnetics used for building the prototype.

Chapter 5 presents the experimental results of measurements done with the prototype designed in the previous chapter. Voltages and current waveforms are presented for confirming the converter operation as described in Chapter 3, as well as tables for comparing theoretical results and experimental measurements. The estimated efficiency of the converter is also compared with the measured efficiency.

Chapter 6 starts with a brief description of the Dual Phase-Shift modulation applied to the DAB converter. After that, an investigation is done for a specific operation condition of the Dual Phase-Shift modulation where there is a period when no active power is transferred between the input and output voltage sources. The results obtained from such investigation inspired the development of an algorithm for minimizing the current stress of the converter when operating in this condition of the Dual Phase-Shift modulation. A comprehensive description of the proposed algorithm is done, with simulation and experimental results for showing the operation of the algorithm and proving that its goal of minimizing current stress is achieved.

Chapter 7 ends the Master's thesis with the final conclusions of the work done with suggestions for future work regarding the algorithm proposed.

2 LITERATURE REVIEW

In this section, the literature is reviewed to get familiar with the converter's fundamental concepts, the challenges of its design and the state-of-the-art techniques shared by other researchers.

The Dual Active Bridge converter was proposed by De Doncker; Divan; Kheraluwala (1991), both single-phase and three-phase topologies, for use in applications that need high power and high power density. In the three-phase version, much higher power can be processed, since currents are better distributed between magnetics, input/output filter capacitors are smaller and output current ripple is reduced (Li *et al.*, 2023; Safayatullah *et al.*, 2022). However, the single-phase version has a simpler design, lower cost and can achieve comparable power capacity by combining other modules.

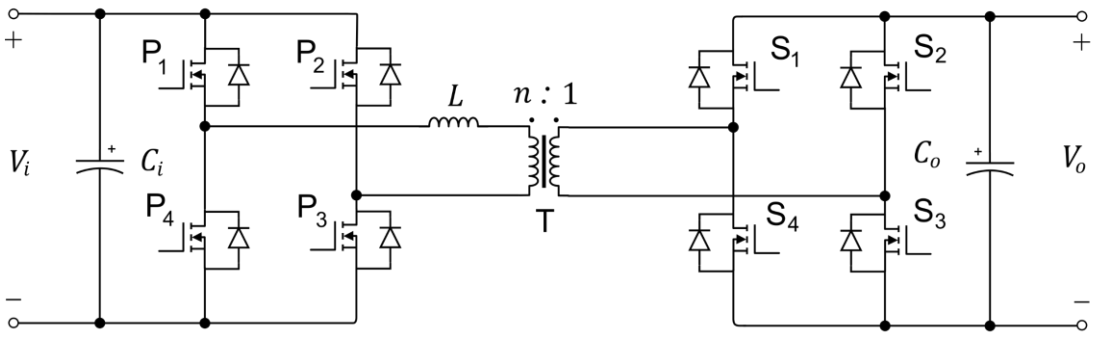
The DAB converter did not receive much attention in its early years after it was proposed in 1991 (Zhao *et al.*, 2014), but has been gaining a lot of interest from the academy since 2015 (Kenzelmann *et al*., 2015 ; Li *et al.*, 2023), due to the development of better semiconductors and desirable characteristics for trending technologies (Zhao *et al.*, 2014). Prototypes reported in the literature have rated power up to 500 kW. Potential applications for the DAB are:

- Renewable Energy (Friedemann; Krismer; Kolar, 2012);
- DC Grids / Smart Grids (Song *et al.*, 2020; Segaran, 2013);
- Electric Vehicles (terrestrial) (Yan *et al.*, 2020);
- MEAs (Buticchi; Costa; Liserre, 2017; Naayagi; Forsyth; Shuttleworth, 2012);
- Solid State Transformers (SST) (Heinig *et al.*, 2022; Xu *et al.*, 2020).

This review covers a wide range of topics important for converter design, like: modulation strategies, optimization, magnetics, modelling, wide bandgap semiconductors and topological modifications.

The scope of this review is limited to single-phase topologies. In this work, the "conventional DAB" is defined as the single-phase topology proposed by De Doncker; Divan; Kheraluwala (1991): composed by H-bridges (full-bridges), voltage-fed and non-resonant. Figure 1 presents the topology.

Figure 1 – Topology diagram for the conventional DAB.



Source: provided by the author, 2024.

Below are some terms' definitions for ease of understanding the concepts of the converter and explanations in this chapter:

- "Voltage conversion ratio" or "Voltage ratio": means the ratio between input and output voltage referred to the same side of the transformer. For example, if both voltages are referred to the primary, then the voltage conversion ratio is $K = nV_o/V_i$, where n is the turns ratio of the transformer, V_i is the input voltage and V_o is the output voltage. Not to be confused with DC-DC conversion;
- Voltage match: when the voltage ratio is unitary (or close to unity);
- ZVS region: group of operating points depending on voltage ratio, phase-shift or power transmitted that enables ZVS operation of the converter;
- Reactive/circulating/backflow power: is defined as the portion of instantaneous power that goes back to the input source and does not contribute to active output power;
- Current stress: peak and RMS values of the inductor current.

2.1 TOPOLOGY OVERVIEW

The conventional DAB has an input and an output capacitor, two active H-bridges separated by a transformer in series with an inductor. The two bridges make it possible to control power flowing in both directions and achieving high

levels of power. The transformer provides galvanic isolation and allows buck-boost operation. The inductor serves as the instantaneous energy storage component (Zhao *et al.*, 2014). The idea is that the leakage inductance of the transformer is used as the inductor, improving the power density of the converter, whereas an external inductor would compromise the power density, reliability and increase costs (but can be used as well). Natural soft switching by Zero Voltage Switching (ZVS) is achieved by using resonance between the parasitic output capacitance of the power switches and the inductor (De Doncker; Divan; Kheraluwala, 1991).

The main converter's losses can be divided between two components: the transformer and the switching devices. In the transformer, there are copper losses and core losses. In the switching devices, there are conduction losses and switching loss (Kim *et al.*, 2011).

Both copper and conduction losses depend on the RMS value of the current. The reactive power is responsible for increasing the RMS value of the current without increasing the active power transmitted (Kim *et al.*, 2011).

The core losses are dependent on the magnetic flux density, which depends on the net voltage-seconds applied, which in turn depends on the peak value of the current. Of course, switching frequency also impacts core losses (Kim *et al.*, 2011).

The switching losses are dependent on the switching frequency, voltage across the power switch and peak value of the current (Kim *et al.*, 2011).

In the last 10 years, there have been over 200 papers proposing topological/hardware modifications for the DAB, such as: different active bridges, transformers, inductors, resonant components, multiport input/output and many others. Both voltage-fed and current-fed topologies are possible (Li *et al.*, 2023).

2.2 MODULATIONS

The modulation strategy chosen for the converter can impact several aspects of its operation. Common optimization goals are: minimum RMS value of current, minimum reactive power, minimum current stress (Kim *et al.*, 2011), ZVS

range, efficiency under light load and transformer DC bias elimination (Li *et al.*, 2023; Corti *et al.*, 2022).

Traditional modulation strategies for the conventional DAB converter are the phase-shifted Pulse Width Modulations (PWM) (Corti *et al.*, 2022). The duty cycle of the driving signals is always fixed in 50%. There are usually two types of phase-shifts:

- External/outer phase-shift: the phase-shift between the output voltages of the primary and secondary bridges. This is done by adding a phase-shift in the PWM's carrier signal of one bridge with respect to the carrier of the other bridge. The leading voltage is the one delivering power.
- Internal/inner phase-shift: the phase-shift between driving signals in a pair of power switches from the bridge. The addition of the inner phase-shift leads to a 3-level voltage waveform in the output of the bridge, allowing to adjust its duty cycle. Sometimes this parameter is defined in terms of the duty cycle from the output voltage waveform of the active bridge.

It is also important to note that, some authors define different references for the phase-shift. Some common choices are: at the start of the active period, at the middle of the active period or at the fundamental component of the voltage. The reference chosen might impact in the form of the equations for the parameters of the converter, which can be confusing. Obviously, all of them should compute the same value.

As the number of phase-shifts (i.e., control variables) increases, the better the converter's performance can be optimized. However, the complexity of modelling and control implementation also increases.

2.2.1 Single Phase-Shift

The simplest modulation strategy is the Single Phase-Shift (SPS), which consists of the external phase-shift only. The waveform of the output voltage from both bridges is 2-level only. This modulation can only control the active power

transmission of the converter and achieves good efficiency rates when the voltage conversion ratio is close to unity (Corti *et al.*, 2022).

Since it cannot control reactive power, which increases when there is no voltage match, the efficiency is reduced because of increased current stress (Corti *et al.*, 2022; Liu; Sun; Liu, 2022).

Dead-time reduces the active power transmitted. This effect can be compensated by adding a value to the phase-shift reference proportional to the deadtime period, resulting in a bigger phase-shift value needed than the ideal case with no deadtime for the same output active power (Bai; Mi, 2008; Segaran, 2013).

The start-up process using SPS is a critical issue for the converter. If the output voltage is already relatively high on start-up, but it is still not the reference value, the phase-shift should be incremented slowly until it reaches the rated value required for that operation point. This way, the peak value of the inductor current during start-up is minimized (Bai; Mi, 2008). However, if the output voltage is zero, the inductor current cannot be limited, whether it is a hard start or soft start, leading to a large inrush current that could damage the converter. Therefore, in this case it is recommended to use another modulation strategy, since other methods to address this issue would be:

a) increase the input voltage from zero;
b) precharge the output capacitor;
c) utilize components that withstand bigger current stress (Bai, Mi, 2008).

Naayagi, Forsyth and Shuttleworth (2012) presented an analysis of the converter during steady-state, providing essential equations for its hardware design and loss estimates, such as RMS value of the inductor current and RMS and average values of the semiconductors' current, considering both buck and boost modes of operation (i.e., bidirectional power flow).

Moreover, the impact of snubber capacitors installed across the switches on the ZVS operation of the converter is studied. Experimental tests with a prototype processing 7 kW show that the results of proposed equations are similar to measured values.

2.2.2 Extended and Dual Phase-Shift

Extended Phase-Shift (EPS) and Dual Phase-Shift (DPS) modulations were introduced to minimize the reactive power and increase the ZVS range when there is no voltage match or under light load. Aside from the external phase-shift, in EPS there is an internal phase-shift in only one of the bridges, whereas in DPS, both bridges have the same value of internal phase-shift applied (Corti *et al.*, 2022). Although better than SPS, DPS still cannot achieve ZVS for all switches under light load (Yan *et al.*, 2020).

DPS modulation in DAB converters was studied initially by Bai and Mi (2008). The definition of reactive power used is the instantaneous power sent back to the input source during its operation, which happens when the inductor current and the input voltage have different polarities. Other papers adopt the same definition for reactive power (Wang *et al.*, 2014; Shao *et al.*, 2019), however, it is important to remember that it does not account for all non-active power in the converter.

The reduction of reactive power also implies on the reduction of the output voltage ripple, since it is directly proportional to reactive power (Bai; Mi, 2008), and the reduction of current stress for the same amount of power transmitted, compared to SPS (Zhao; Song; Liu, 2012).

Furthermore, with DPS modulation, it is possible to soft-start the converter with zero output voltage without the need of additional circuits. The inrush current is significantly lower during the soft-start with DPS, in comparison with SPS modulation (Bai; Mi, 2008).

Experimental tests done by Bai, Nie and Mi (2010) confirmed that DPS can achieve higher efficiency than SPS when there is no voltage match (much less than unity) and under light-load conditions, but SPS can achieve higher efficiency when there is voltage match and under light-load or no voltage match (much higher than unity) and under heavy load conditions. Hence, it is recommended to use SPS during heavy-load and DPS under light-load operation for better efficiency across the power range of the converter.

An in-depth analysis made by Kim *et al.* (2011) provided equations for active power transmission, reactive power and RMS and peak values of the

inductor current for DPS. It also shows ZVS regions for different operation points. Limiting the external phase-shift to 90° reduces the following aspects: reactive power, RMS and peak value of inductor current. The equations provided allow for optimization of the control strategy to minimize these aspects, but only one can be chosen. Simulation and experimental tests with a 3.68 kW prototype show that the DPS modulation minimizing the peak value of the inductor current can result in higher efficiency for the whole power range than with SPS (application considered is an EV Charger).

According to Coelho and Batschauer (2021), comparing different modulation strategies by looking at the RMS value of the transformer current alone is not enough for estimating the best operation point. Neglecting the number of voltage levels applied to the transformer can lead to inaccurate estimates of its apparent power. Experimental results from different operation points using SPS, EPS and DPS are presented for confirmation.

2.2.3 Triple Phase-Shift

Triple Phase-Shift (TPS) modulation has the external phase-shift and two different internal phase-shift for each of the bridges in the converter, meaning three degrees of freedom for control. SPS, EPS and DPS can be seen as special cases from the TPS modulation. Since it is the most complete phase-shift modulation, the converter operating with TPS has the potential to achieve highest efficiency through the whole operation range (Corti *et al.*, 2022). It can achieve ZVS for all switches even under light load, however, switching-off current can increase (Yan *et al.*, 2020).

The Trapezoidal and Triangular Modulation Method proposed by Schibli (2000) shapes the inductor current waveform accordingly, in which the main goal is to reduce switching loss by modulating the current down to zero before turn-off, but it does not happen at every switching event. Trapezoidal Mode minimum power transmitted is the maximum power for Triangular Mode. A few drawbacks of this modulation are: it cannot be used if one of the bridges' output voltages is zero (or close to) or both equal (for triangular mode), unbalanced distribution of

losses (Schibli, 2000) and they could increase the RMS value of the inductor current (Kim *et al.*, 2011).

Krismer and Kolar (2012) presented a TPS modulation scheme optimizing the RMS value of the inductor current, decreasing conduction and copper losses. The converter operation is analyzed considering the fundamental component of the voltages. Closed form solutions are presented for the design. Under light load, the proposed modulation scheme falls into Triangular Current Modulation and under heavy load, into SPS. In medium power however, the operation results in complex equations, increasing control processing costs. Furthermore, the modulation scheme does not consider the ZVS conditions of the converter.

Huang *et al.* (2016) analyzes the TPS modulation considering all harmonic components of the voltages and presents an optimized modulation scheme to achieve minimum current stress. An auxiliar phase-shift is introduced between the fundamental component of the bridges' output voltages, which helps to define the direction of power flow. An optimization algorithm is implemented to deduce closed form solutions of the control variables. Under light load, the modulation scheme can also reduce the RMS value of the inductor current. Moreover, it is verified that the converter can operate with soft switching through the whole power range. The proposed optimization algorithm could be applied considering the minimization of any other parameter.

Table 1 resumes the traditional Phase-Shift (PS) strategies described in a conventional DAB. For this work, the name of the modulations refers to the types of phase-shifts used in it, since many modulation strategies (optimized) have been proposed based in these (as presented in this chapter).

2.2.4 Other Modulations

Many other modulation strategies and optimizations have been proposed based on phase-shift for many applications, which may include other parameters like different duty cycles (asymmetric modulations) and variable switching frequency (He *et al.*, 2023).

For example, Taylor *et al.* (2018) proposed a modulation for on-board EV chargers that allows the DAB to function as a Power Factor Correction (PFC) and

Table 1 – Traditional Phase-Shift modulations comparison.

Modulation	SPS	EPS	DPS	TPS
External PS	Yes	Yes	Yes	Yes
Internal PS	No	Only in one bridge	Equal for both bridges	Different for both bridges
Control Variables	1	2	2	3
Voltage Levels	2	2 and 3	2 and 3	2 and 3
Active Power Control	Yes	Yes	Yes	Yes
Reactive Power and ZVS Control	No	Limited	Good	Best
Complexity	Easy	Medium	Medium	Hard

Source: provided by the author, 2024.

the DC-DC converter for transferring power. Basically, the modulation strategy uses a combination of DPS with variable switching frequency and TPS. When the input voltage (rectified grid voltage) is around its peak, the instantaneous transferred power is higher, in which the DPS modulation achieves higher

efficiency. When the input voltage is lower, TPS becomes the better option, since it can enable ZVS under light load. The use of DPS and TPS modulations allows to shape the input current waveform, achieving close to unity power factor from medium to high power, although the total harmonic distortion of the grid current is around 60% when under low power.

For high power DC grids, the use of Medium and High Voltage (MV and HV) is preferable to decrease losses through the line. In this case, the use of multilevel converters is recommended, because of the lower voltage stress on the power switches. Song *et al.* (2020) proposed an optimized modulation scheme for a DAB converter with a 5L NPC bridge on the high voltage port, which also allows for more degrees of freedom to shape the voltage waveform. Analytical solutions are developed for reducing the current stress, while considering the ZVS constraints. Simulations show that the modulation can achieve higher efficiency in the full power range even when there is no voltage match, in comparison to SPS.

2.3 MODELLING

The simplest way to model a DAB converter is by utilizing the reduced order model, which doesn't consider the dynamics of the inductor current, resulting in a first-order model. This model is accurate enough for designing and implementing a voltage controller (Shao *et al.*, 2022).

An analysis for modelling the converter operating with SPS is done by Santos-Silva (2019), in which transfer functions are derived in both continuous and discrete domain for designing an output voltage controller. The designed controllers are validated using simulations in software and hardware-in-the-loop platforms.

In smart grids, a few requirements for power converters like galvanic isolation, bidirectionality and high performance regulation can be met by using the DAB converter. However, high performance voltage regulation design requires highly precise models of the converter. Segaran (2013) developed a dynamic model of the conventional DAB with SPS modulation considering all the harmonic components of the converter's operation. This way, the proposed

model can predict the switching nature of the converter. The analysis also takes into consideration the deadtime effects on dynamics and the power transmitted. The model can present a very similar behavior of the output voltage as seen in simulations of the converter. However, the inductor current equation of the model does not match the dynamic behavior of the simulation, only the steady state operation is accurate. Furthermore, the model can only predict transients caused by a minor phase-shift step (around 5°). Bigger steps of phase-shift require an adaptation of the model.

2.4 SOFT-SWITCHING

The soft-switching in DAB converter depends on a few parameters: voltage conversion ratio, phase-shift angle, power switch output capacitance and magnitude and polarity of current on the switching instant (Kim *et al.*, 2011).

An analysis considering all harmonic components of the voltages is done by Riedel *et al.* (2017) to determine the ZVS region of the converter with more accuracy. It is found out that a simpler analysis considering only the fundamental component of the voltages leads to a smaller ZVS region than the full harmonic analysis, especially for low phase-shift values, where importance of higher harmonic components matters the most. The authors present expressions for analyzing the impact of various parameters, such as dead-time, parasitic output/snubber capacitors and different transformer impedances.

For SPS, both phase legs in a bridge have the same ZVS boundaries (Riedel *et al.*, 2017). Operation with voltage match results in ZVS for all power switches, guaranteeing higher efficiency (Kim *et al.*, 2011). As the voltage ratio increases or decreases under light load, one of the bridges will lose the ability to achieve ZVS (Guenter *et al.*, 2023).

When internal phase-shifts are applied (i.e., DPS and TPS), each phase leg has its own boundary and the ZVS regions of the converter change completely (Riedel *et al.*, 2017).

If active power is being transmitted to the load during soft-switching, the ZVS region will decrease if operating under light load (Guenter *et al.*, 2023).

Incomplete soft-switching not only leads to more switching losses, but also overvoltage across the switches (Guenter *et al.*, 2023).

The power switch's parasitic output capacitance is one of the main parasitic elements that limit soft-switching (or snubber capacitor, if used), since it slows down the slew rate of the voltages. The magnitude of the inductor current must be large enough to fully discharge this capacitance, before dead-time ends (Guenter *et al.*, 2023; Riedel *et al.*, 2017). If the inductor current crosses zero before the bridge's output voltage transition, a partial hard switch occurs. Dead-time also alters the ZVS regions. (Riedel *et al.*, 2017).

Finally, the ZVS regions are altered when the transformer's primary and secondary leakage inductance are not closely matched, causing an asymmetry between the primary and the secondary bridges. (Riedel *et al.*, 2017).

2.5 VARIABLE VOLTAGE APPLICATIONS

In applications like EVs and BESSs, one of the requirements for the converter is to be able to operate with high efficiency for a wide output/input voltage range through the full power range (Safayatullah *et al.*, 2022). The natural ZVS operation of the DAB converter is essential for that.

The modulation strategy proposed by Yan *et al.* (2020) for EV chargers makes sure the converter is working with ZVS under the whole power range, by integrating SPS, DPS and TPS, assuring smooth transition between them and the charger operation modes. The strategy also considers the dead-time. Experimental tests with a 20 kW SiC-based prototype show the proposed modulation increases the efficiency of the converter under the whole power range, when compared with SPS modulation. The results also show a smooth transition between G2V and V2G operation.

Gill *et al.* (2019) proposes an EV fast charger connected directly to MV grid composed of PFC and DC-DC converters, disposing the need for big and heavy low frequency transformers. The DC-DC stage is a multilevel ISOP (input-series-output-parallel) DAB-based converter. The authors propose a SPS-based modulation strategy with variable input voltage and switching frequency, in order to maintain voltage match and extend the ZVS region on most of the power range.

Experimental results on a 12 kW prototype with 3.3 kV SiC MOSFETs show that the strategy is able to extend the ZVS range under different output voltage and power scenarios.

To deal with a variable input voltage, Bezerra *et al.* (2014) chooses a DAB converter with a 5 level T-type half-bridge for the primary side of the converter, which allows to apply half of the input voltage to the transformer, providing more flexibility. In this work, the authors propose an optimized modulation scheme focused on increasing the efficiency of the converter by minimizing the RMS value of the inductor current. Estimated conduction loss results show that the 5LDAB can achieve higher efficiency than the conventional DAB for input voltages between 500 V and 800 V, whereas the conventional DAB has higher efficiency for input voltages less than 400 V, considering a power range of 7 kW and fixed output voltage of 700 V.

Similarly, Higa *et al.* (2015) proposes the use of a T-type full bridge in the secondary with variable output voltage. Since the voltage applied is cut by half in half bridge mode, reduced iron losses in the magnetic core can be achieved, because magnetic flux density is directly proportional to the voltage (Higa *et al.*, 2015; Qin *et al.*, 2018).

Another way to get a better voltage conversion ratio with variable voltages is by applying a rectangular voltage with a DC component, which can be filtered out by a DC blocking capacitor in series with the inductor. The magnitude of the voltage will be half of the voltage source. Qin *et al.* (2018) proposed a modulation with this idea for a conventional DAB, while analyzing the ZVS regions, which is tested in a 1.5 kW prototype. In the same manner, Xuan *et al.* (2019) used this concept for their modulation strategy, but considering a 5L NPC in both bridges for an EV charger application. In this case, the topology allows for 4 different voltage amplitudes. Experiments on a 3.5 kW prototype resulted in 98% of peak efficiency and 93% under light load.

2.6 MAGNETICS DESIGN

The design of the transformer is also an important subject. Although this Master's thesis does not cover any magnetic design method in detail, this section

presents some insights from other authors in how the design of magnetic components can affect the operation of the DAB converter.

A simpler design method usually considers the magnetizing inductance much larger than the leakage inductance, neglecting its impact on the converter. An analysis made by Yin *et al.* (2021) concluded that the value of the magnetizing inductance impacts on: the shape and peak value of the transformer current, the ZVS region and the power transmission capability of the converter. As it decreases, the peak value of the transformer current increases, the ZVS region widens and the power transmission capability decreases, since more current flows through the magnetizing inductance instead of going to the load.

An analysis made by Vardhan, Odavic and Atallah (2023) provided analytical equations for designing the converter considering the magnetizing inductance. Expressions for the RMS value of the inductor current, switching currents, active power and ZVS regions are provided. It is reported that a non-optimal value for this parameter can lead to an increase in losses and mass of the transformer, depending on the core type, thus lowering the power density of the converter.

Dey *et al.* (2022) presents a transformer design method for DAB, which considers the leakage inductance as the DAB inductor. Equations and winding arrangements are provided for achieving the design goals. Measurements of a prototype confirms that the transformer has the calculated magnetizing and leakage inductances.

The parasitic capacitance of the inductor must be minimized during its design and construction. Otherwise, it can lead to large oscillations in the inductor current, bringing negative impacts to the performance of the converter, such as EMI and higher losses (Guenter *et al.*, 2023).

2.7 TRANSFORMER SATURATION

Transformer saturation is an important topic regarding any power converter that uses a transformer. Some non-idealities such as gate driver delay signals, unmatched turn-on and turn-off times and parasitic resistances can lead to unbalanced volt-seconds applied to the transformer, thus introducing a DC

offset component. Although the winding resistances can mitigate the DC component, this parameter is kept as low as possible to reduce conduction losses. Even if the transformer does not saturate, core losses are increased. Should the transformer saturate, the peak value of the magnetizing current increases, along with conduction losses and switching losses, eventually destroying the converter (Ortiz; Mühlethaler; Kolar, 2011).

A traditional and simple method to avoid a DC component in the transformer is by placing series capacitors in both windings. However, this method can degrade the power density of the converter, since high power operation requires big capacitors that support high currents. Ortiz, Mühlethaler and Kolar (2011) briefly described some existing methods to measure and compensate DC flux density components in transformers.

A method proposed by Ortiz, Mühlethaler and Kolar (2011) consists of an additional magnetic core installed in parallel with the main core. When the inductance of this auxiliary winding decreases, it indicates that the core is starting to saturate. An additional circuit obtains a signal inversely proportional to the inductance by measuring the current in the auxiliary winding. A controller implemented in a DSP uses this signal to estimate the DC component in the flux density of the main core. Finally, the controller adjusts the duty cycle in the PWM to compensate for the DC component. Experimental tests show that the proposed method can effectively avoid DC offsets on the operation of the DAB transformer, ensuring higher efficiency during the operation of the converter.

Chorfi *et al.* (2022) proposed the use of a current sensor for the inductor with a digital controller in a DAB with 3L ANPC bridges, which is a topology suitable for using 650 V GaN transistors in an 800 V EV on-board charger. The controller uses the sensed current to adjust the duty cycle of the primary bridge switches to compensate for the DC current. A 1.5 kW GaN-based prototype with DPS modulation used in experiments confirms the effectiveness of the proposed technique, by keeping the offset current smaller than 20 mA.

Assadi *et al.* (2018) developed a saturation prevention algorithm that relies on the measured output current of the converter. The method is intended for use in conventional DAB-based EV chargers, in which the output of the converter is connected to a battery. Basically, the algorithm calculates the slope of the current

waveform in the battery. When this value rises above a predefined threshold, it is assumed that the core is saturating. The algorithm is implemented in a FPGA. Experimental tests with a 6.6 kW SiC-based prototype and 125 kHz of switching frequency show that the algorithm can detect the divergence between the sampled current points, caused by a DC offset in the transformer current, which increases the slope. When it crosses the threshold, the algorithm adjusts the PWM duty cycle to counter the DC offset, preventing the transformer from entering the saturation region.

Liu; Sun; Liu (2022) improves a modulation strategy focused on minimizing the RMS value of the inductor current, adding the function to suppress DC offsets that can occur during a change in the operation point of the converter, i.e., when power increases or decreases. The proposed modulation allows the current to quickly reach steady-state.

2.8 HARDWARE OPTIMIZATION

Airborne Wind Turbine generators require bidirectional DC-DC converters for transferring the power to the grid as well as powering up the motors required to fly the kites. Galvanic isolation between the kite and the ground station is required for safety. Since the generators operate in the air, power converters need to be as light as possible. Friedemann; Krismer; Kolar (2012) chooses a DAB topology composed of a full-bridge for the LV side and a 3L NPC for MV side for this application. The system uses 4 DC-DC converters of 25 kW, and each of them uses 4 DAB cells of 6.25 kW connected in an input-parallel-output-series connection. After estimating losses of the converter and designing optimal transformer and heatsink in respect to minimum weight, the researchers achieved a power-to-weight ratio of 4.4 kW/kg with a maximum efficiency of 97%, meaning each DAB cell weights approximately 1.42 kg for a rated power of 6.25 kW.

2.9 HIGH POWER PROTOTYPES

To give an idea of how much power a DAB converter can process, in the next paragraphs a few prototypes reported in the literature so far are described.

Table 2 sums up the information for a single DAB cell prototype provided by the papers. Note that this list is not limited to the conventional DAB topology.

Kheraluwala *et al.* (1992) built a 50 kW prototype, operating with 50 kHz of switching frequency, input voltage of 200 V and output voltage of 1600 V. At the time, there wasn't much availability of power switches rated at the desired output voltage. Therefore, the secondary bridge of the DAB prototype consists of two half-bridges in series, to reduce the voltage stress on the switches. Overall weight power density is estimated to be 0.24 kg/kW. An efficiency of 87.2% is achieved when the converter operates with voltage match.

Liang *et al.* (2019) proposes a 350 kW EV fast charger connected in MV. The system is composed of three modules for each phase, consisting of a PFC stage and the DC-DC isolated stage. The DC-DC converter is a DAB composed of an ANPC on the MV side (12 kV) and a full-bridge on the LV side (800 V), using 10 kV SiC MOSFETs on the MV bridge and 1.2 kV SiC MOSFETs, with 25 kHz of switching frequency. TPS modulation is chosen. Loss estimates and simulations are done to verify the viability of the converter, showing the system could reach 98% efficiency.

SSTs are a promising technology to be applied in smart grids and MV grids. The DAB converter is one of the building blocks for SSTs. Xu *et al.* (2020) designs and tests a 200 kW and 1.3 kV SiC-based DAB cell prototype for power switch evaluation. The goal is to use this cell in a 1 MW SST in MV grids. The peak efficiency obtained is 99.53% and the power density is 1.6 MW/m³. Guo *et al.* (2023) presents the transformer and external inductors designs, with a developed prototype of 222 kW and 15 kHz. The SST system is then built and successfully tested.

Heinig *et al.* (2022) experimentally tests two DAB cells rated at 550 kW: one with Si IGBT devices at 2.5 kHz and the other with SiC MOSFETs at 4 kHz, to evaluate efficiency and the switching devices behavior. The test was made for an operation point of 1600 V in the MV side and 800 V in the LV side, with 360 kW of power being transmitted. The SiC-based DAB cells achieved higher efficiency. The cells are meant to be used in an ISOP system of 4 cells, reaching 2 MW of rated power. With the results of the experiment, it is expected that the SiC DAB-based SST could reach 99% efficiency.

Table 2 – High power DAB prototypes reported in the literature.

Reference	Rated Power	Switch Technology	Application	Power Density	Peak Efficiency
(Gill *et al.*, 2019)	12 kW	SiC	EV Fast Charger	x	x
(Yan *et al.*, 2020)	20 kW	SiC	EV Fast Charger	3 kW/L	98%
(Naayagi; Forsyth; Shuttleworth, 2012)	20 kW	Si	Aerospace	x	90%
(Kheraluwala *et al.*, 1992)	50 kW	Si	x	0.24 kg/kW	87%
(Liang *et al.*, 2019)	117 kW	SiC	EV Fast Charger	x	98%
(Xu *et al.*, 2020)	200 kW	SiC	SST	x	x
(Heinig *et al.*, 2022)	550 kW	Si and SiC	SST	x	x

Source: provided by the author, 2024.

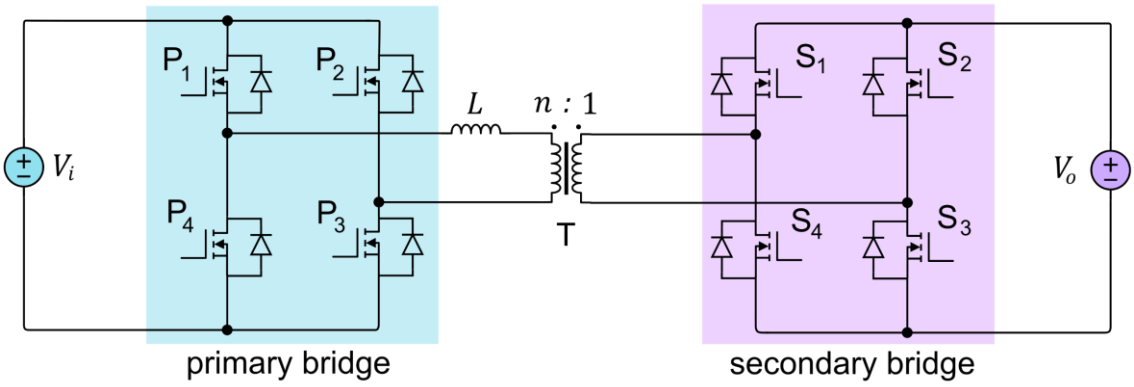
3 SINGLE PHASE-SHIFT MODULATION

In this section, the fundamental concepts and mathematical analysis of the conventional DAB converter employing SPS modulation are presented. Some parameters were also derived by Santos and Martins (2014) and Kirsten (2014), resulting in similar equations.

In the analysis, it is considered that the left bridge is the primary bridge of the converter, meanwhile the right bridge is the secondary bridge, as shows Figure 2. Because of the bidirectional nature of the converter, it is defined that:

- Positive power flow ($P > 0$ and $\phi > 0$) is considered power transferred from left to right;
- Negative power flow ($P < 0$ and $\phi < 0$) is power transferred from right to left.

Figure 2 – Definitions used for the DAB converter topology.



Source: provided by the author, 2024.

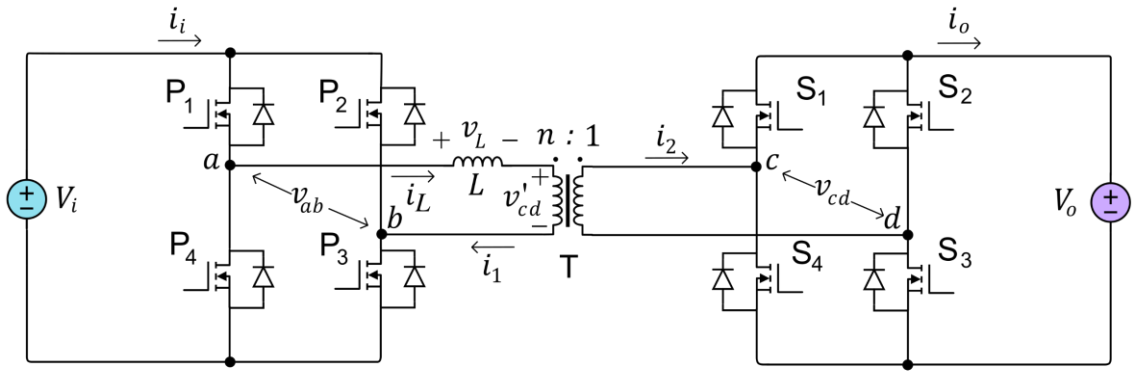
For ease of understanding, the following assumptions are done to demonstrate and analyze the steady state operation of the converter:

- All components are ideal and there are no losses;
- Magnetizing inductance of the transformer and dead-time of power switches are not considered;
- Positive power flow;
- Buck mode, i.e., $V_i > nV_o$;

- The phase angle of the primary bridge output voltage is zero, and the secondary bridge's is ϕ;
- $i_L(0) < 0$ and $i_L(t_1) > 0$, where $t_1 > 0$.

Figure 3 shows the definitions of the voltages and currents on the topology. V_i is the input voltage, $n = N_1/N_2$ is the transformer's turns ratio, V_o is the output voltage, v_{ab} is the output voltage of the primary bridge, v_L is the inductor voltage referred to the primary of the transformer, v_{cd} is the output voltage of the secondary bridge, $v'_{cd} = nv_{cd}$ is the output voltage of the secondary bridge referred to the primary of the transformer, i_i is the input current, i_L is the inductor current in the primary side of the transformer, i_1 is the transformer current in the primary side, $i_2 = ni_1$ is the transformer current in the secondary side and i_o is the output current.

Figure 3 – Voltages and currents defined for analyzing the DAB.



Source: provided by the author, 2024.

3.1 TOPOLOGICAL STAGES

This section describes each stage of the converter in a switching period T_s, with time values given by Table 3. Instants t_a and t_b are the moments where the inductor current crosses zero and are chosen arbitrarily for the sake of a simple analysis, since this parameter depends on other parameters of the converter such as L, V_i and V_o.

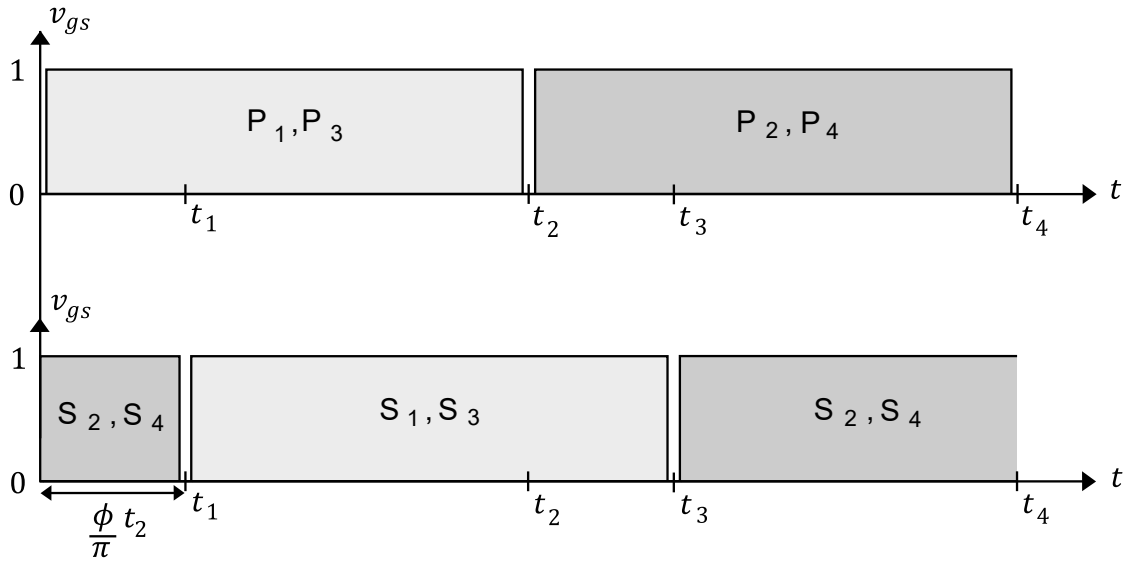
Figure 4 presents the driving signals of the power switches in the DAB converter employing SPS modulation, considering the assumptions done.

Table 3 – Instant time values for $\phi > 0$.

Time	Value
t_1	$\frac{\phi}{\pi}\frac{T_s}{2}$
t_2	$\frac{T_s}{2}$
t_3	$\frac{T_s}{2}\left(1+\frac{\phi}{\pi}\right)$
t_4	T_s

Source: provided by the author, 2024.

Figure 4 – Gate signals of the power switches in SPS modulation.

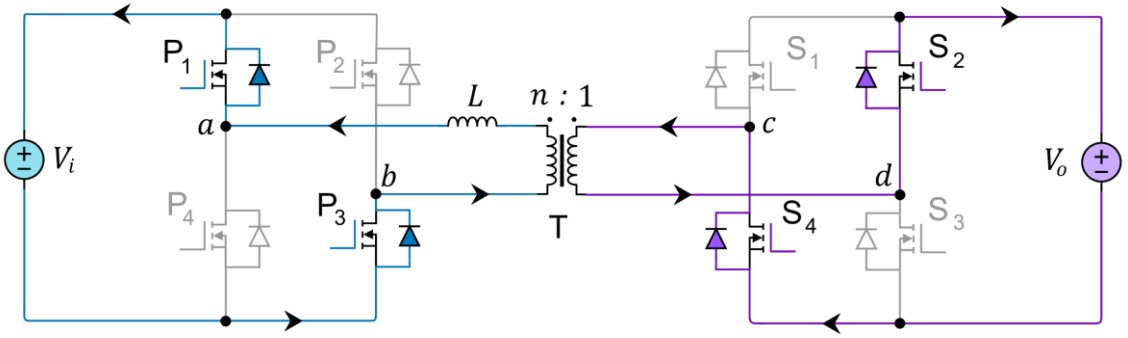


Source: provided by the author, 2024.

a) Time interval: $0 < t < t_a$

The polarity of the initial inductor current value ($i_L(0)$) is defined as being negative. The switches P_1, P_3, S_2 and S_4 are turned on, therefore, the current in the primary bridge flows through the antiparallel diode of P_1 and P_3, and in the secondary bridge, through the antiparallel diode of S_2 and S_4. Figure 5 illustrates this stage. This results in a positive voltage across $v_{ab} = +V_i$ and a negative voltage across $v_{cd} = -V_o$. Since the voltage across the inductor (v_L) is the difference between v_{ab} and v'_{cd}, the current in the inductor starts to rise linearly.

Figure 5 – Stage 1 of a DAB converter operating in SPS.

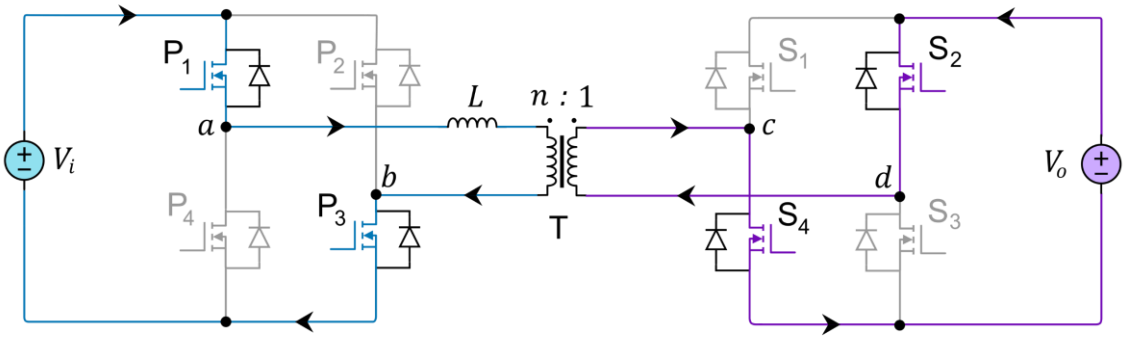


Source: provided by the author, 2024.

b) Time interval: $t_a < t < t_1$

After the instant t_a, the inductor current becomes positive, meaning that the current now flows through the switches in both bridges, as shows Figure 6.

Figure 6 – Stage 2 of a DAB converter operating in SPS.

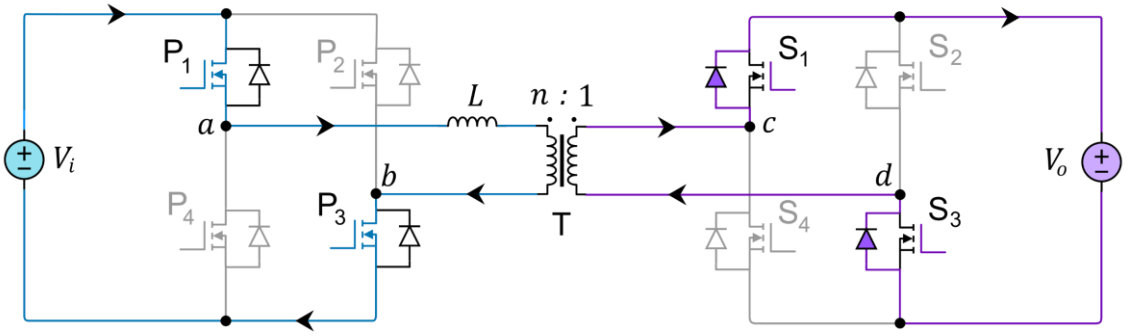


Source: provided by the author, 2024.

c) Time interval: $t_1 < t < t_2$

At this stage, the switches S_1 and S_3 are now turned on, resulting in a positive voltage applied at the output of the secondary bridge, $v_{cd} = +V_o$. Since the current is still positive, the current in the secondary bridge flows through the diode of S_1 and S_3, as can be seen in Figure 7. The slope of the current in the inductor decreases because the voltage applied across the inductor was reduced, but it's still positive.

Figure 7 – Stage 3 of a DAB converter operating in SPS.

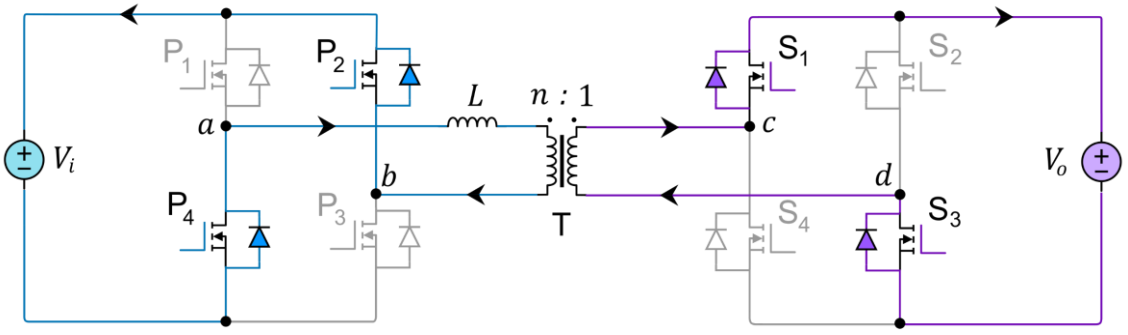


Source: provided by the author, 2024.

d) Time interval: $t_2 < t < t_b$

After half the switching period, the switches P_2 and P_4 are commanded to turn on, causing the output voltage of the primary bridge to become negative, $v_{ab} = -V_i$. Since the current is positive, the diodes of P_2 and P_4 are conducting at this stage, shown in Figure 8. The slope of the inductor current gets negative, linearly decreasing the current over time, until it reaches zero at t_b.

Figure 8 – Stage 4 of a DAB converter operating in SPS.

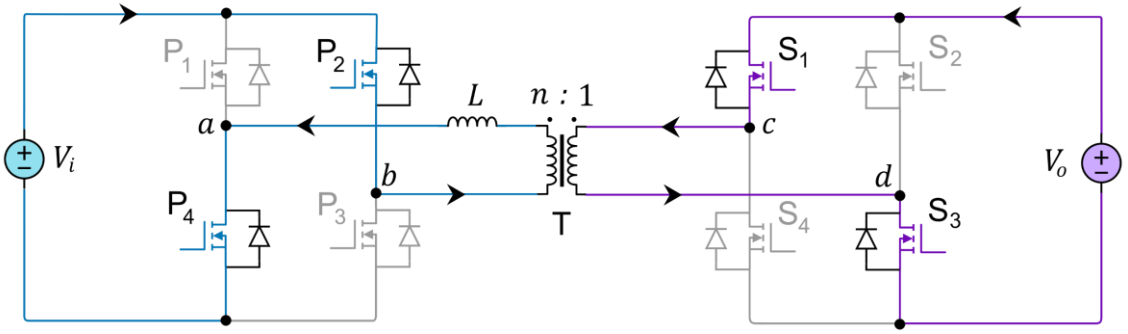


Source: provided by the author, 2024.

e) Time interval: $t_b < t < t_3$

After t_b, the inductor current becomes negative, causing the switches P_2, P_4, S_1 and S_3 to conduct, as seen in Figure 9.

Figure 9 – Stage 5 of a DAB converter operating in SPS.

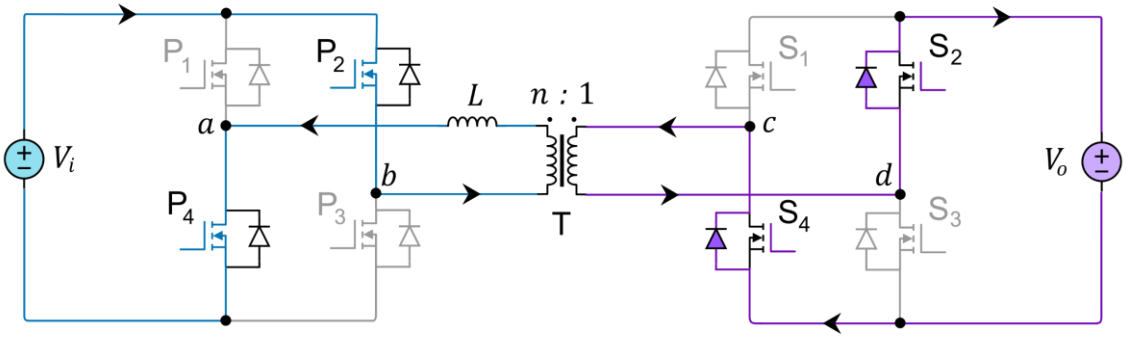


Source: provided by the author, 2024.

f) Time interval: $t_3 < t < t_4$

The switches S2 and S4 are turned on, but its diodes are conducting, since the inductor current is still negative, as can be seen in Figure 10, resulting in $v_{cd} = -V_o$. The slope magnitude of the inductor current decreases, because the magnitude of the voltage applied across the inductor was reduced.

Figure 10 – Stage 6 of a DAB converter operating in SPS.



Source: provided by the author, 2024.

3.2 MAIN WAVEFORMS

Figure 11 presents the main voltages and current waveforms of the operation described in the previous section. These waveforms are for the condition that $i_L(t_1) > 0$. For the Buck mode, $i_L(0)$ will always be negative but there are also two other possible initial conditions for $i_L(t_1)$:

- $i_L(t_1) = 0$
- $i_L(t_1) < 0$

Other possibilities of operation in the AC-link are:

- Boost mode ($V_i < nV_o$);
- Voltage Match mode ($V_i = nV_o$).

Figure 12 shows the waveform of the inductor current in the two modes for comparison. Note that the shape of the inductor current is different for each mode.

For the Boost mode, it (Figure 12) considers $i_L(0) > 0 \wedge i_L(t_1) > 0$. There are also two other possible conditions that changes the shape of the current:

- $i_L(0) = 0 \wedge i_L(t_1) > 0$;
- $i_L(0) < 0 \wedge i_L(t_1) > 0$.

For an application with fixed V_i and V_o, the parameter n is chosen such that the converter always operates in Voltage Match mode, making the most of the topology. In this mode:

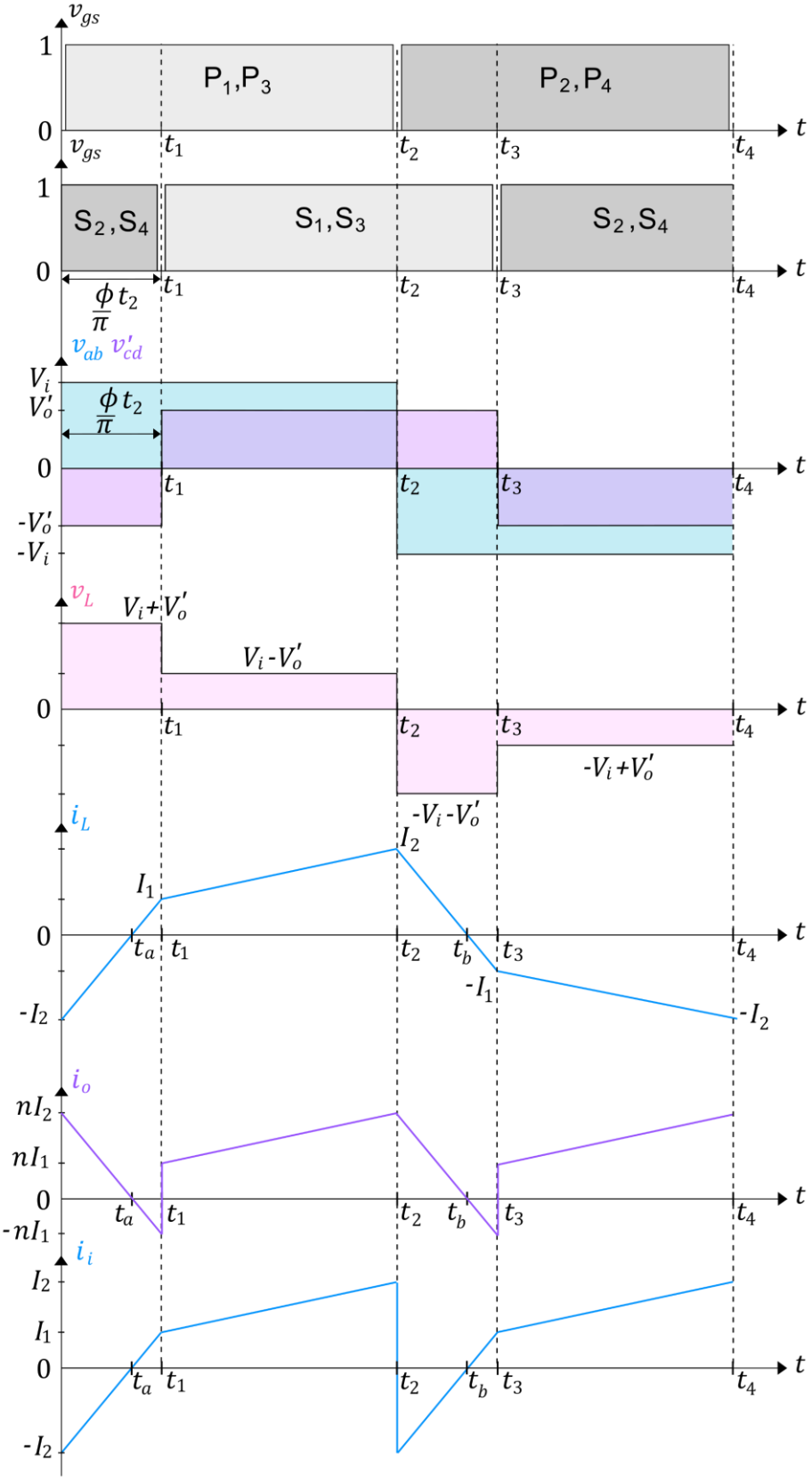
- $I_1 = I_2$
- $i_L(0) < 0 \wedge i_L(t_1) > 0$, always.

Obviously, the transition of power flow direction will change the mode the converter operates if it is not in Voltage Match mode.

It is important to highlight that these modes are referring to the voltages being applied to the terminals of the inductance L, and not the input and output voltage of the converter itself. Although it might seem confusing at first, it will become clearer how they can be helpful for the design of the converter as the analysis gets further.

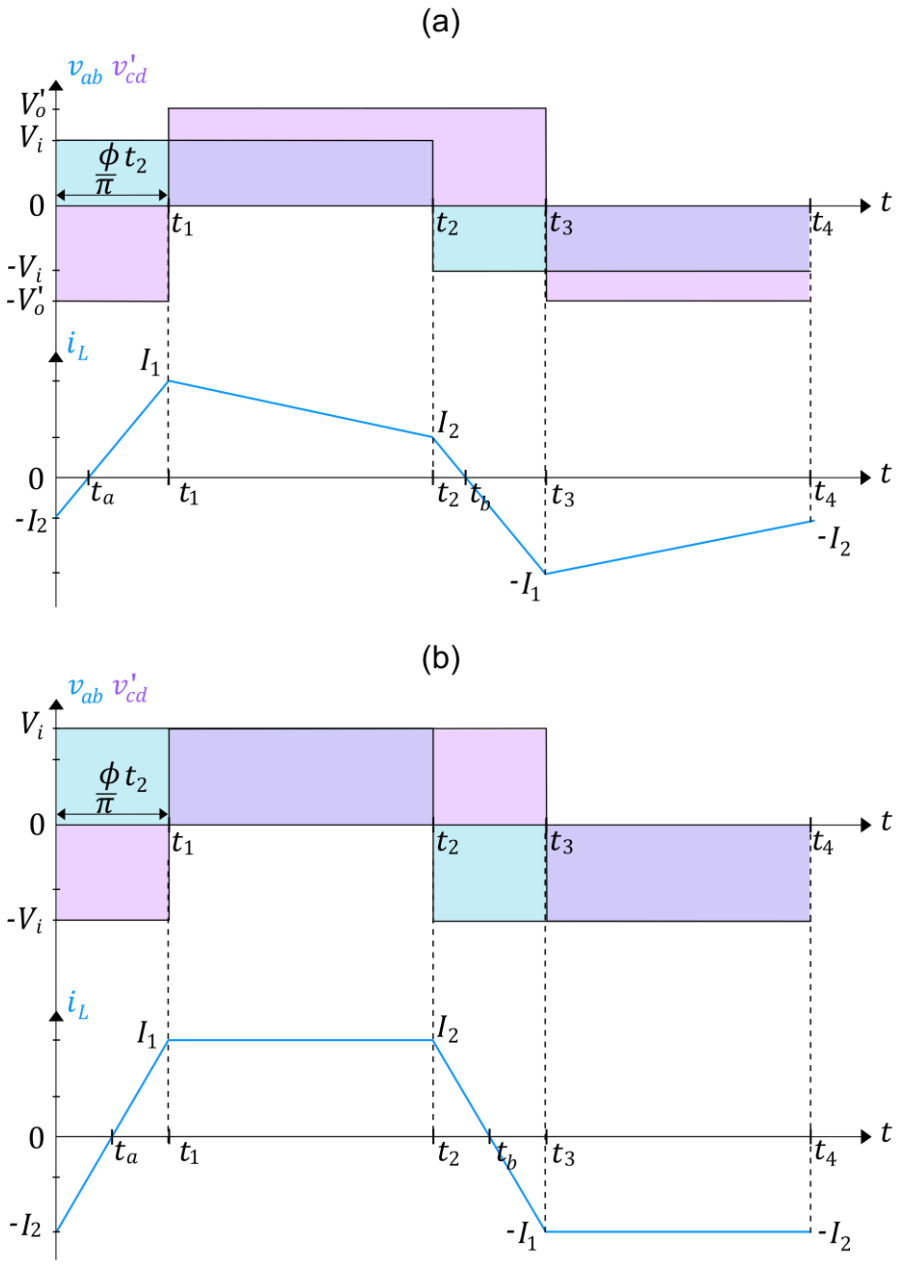
The equations derived in the following sections are suitable for the three modes: Buck, Boost and Voltage Match, operating either with positive or negative power flow, unless stated otherwise.

Figure 11 – Main voltages and currents waveforms of the DAB converter operating in buck mode with SPS modulation.



Source: provided by the author, 2024.

Figure 12 – Inductor current for other modes of operation. (a) Boost mode and (b) Voltage Match mode.



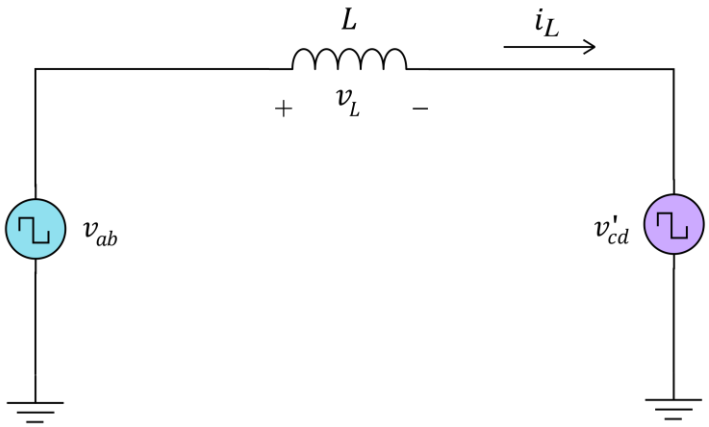
Source: provided by the author, 2024.

3.3 MATHEMATICAL ANALYSIS

The operation described earlier allows for a simpler representation of the DAB converter, which is shown in Figure 13. Basically, the equivalent circuit consists of two rectangular-wave voltage sources that are phase-shifted from each other by ϕ and an inductor, responsible for transferring the power between

both sources. Since there are no losses considered, the input power P_i is equal to the output power P_o.

Figure 13 – Equivalent circuit for power transfer in the lossless DAB converter.



Source: provided by the author, 2024.

3.3.1 Power Transmission

The most important aspect of the DAB is its active power transmission P, which will be designated simply as power transmission. This parameter is defined by equation (3.1). Since the converter operates in a symmetric manner, only half of the switching period is necessary for the calculation. It is important to remind that, since the converter has no losses, the input and output power are the same.

$$P = \frac{1}{T_s/2}\int_0^{T_s/2} v_{ab}(t) i_L(t) dt \tag{3.1}$$

To derive an expression for P, the expressions for the voltage $v_{ab}(t)$ ($v'_{cd}(t)$ could also be used) and current $i_L(t)$ must be found. By looking at Figure 11, it can be concluded that the voltage $v_{ab}(t)$ is defined by expression (3.2).

$$v_{ab}(t) = \begin{cases} +V_i & \forall \ \ 0 < t \leq T_s/2 \\ -V_i & \forall \ \ T_s/2 < t \leq T_s \end{cases} \tag{3.2}$$

Furthermore, $v'_{cd}(t)$ can be defined by expression (3.3), where $V'_o = nV_o$.

$$v'_{cd}(t) = \begin{cases} -V'_o & \forall \ \ 0 < t \leq \dfrac{\phi}{\pi}\dfrac{T_s}{2} \\ +V'_o & \forall \ \ \dfrac{\phi}{\pi}\dfrac{T_s}{2} < t \leq \dfrac{T_s}{2}\left(1+\dfrac{\phi}{\pi}\right) \\ -V'_o & \forall \ \ \dfrac{T_s}{2}\left(1+\dfrac{\phi}{\pi}\right) < t \leq T_s \end{cases} \tag{3.3}$$

. The current $i_L(t)$ can be found by using equation (3.4).

$$v_L(t) = L\frac{di_L}{dt} \rightarrow i_L(t) = \frac{1}{L}\int_0^t \left(v_{ab}(t) - v'_{cd}(t)\right)dt \tag{3.4}$$

Applying equations (3.2) and (3.3) in (3.4), the resulting inductor current is shown in equation (3.5).

$$i_L(t) = \begin{cases} \dfrac{1}{L}(V_i + V'_o)\,t - I_2 & \forall \ \ 0 < t \leq t_1 \\ \dfrac{1}{L}(V_i - V'_o)\,(t - t_1) + I_1 & \forall \ \ t_1 < t \leq t_2 \\ \dfrac{1}{L}(-V_i - V'_o)\,(t - t_2) + I_2 & \forall \ \ t_2 < t \leq t_3 \\ \dfrac{1}{L}(-V_i + V'_o)\,(t - t_3) - I_1 & \forall \ \ t_3 < t \leq t_4 \end{cases} \tag{3.5}$$

I_1 and I_2 are the inductor current values when the converter's state is switched, thus are called "switching currents" in this thesis. Figure 14 highlights the switching currents for the studied case. The other possible cases are (considering $\phi > 0$):

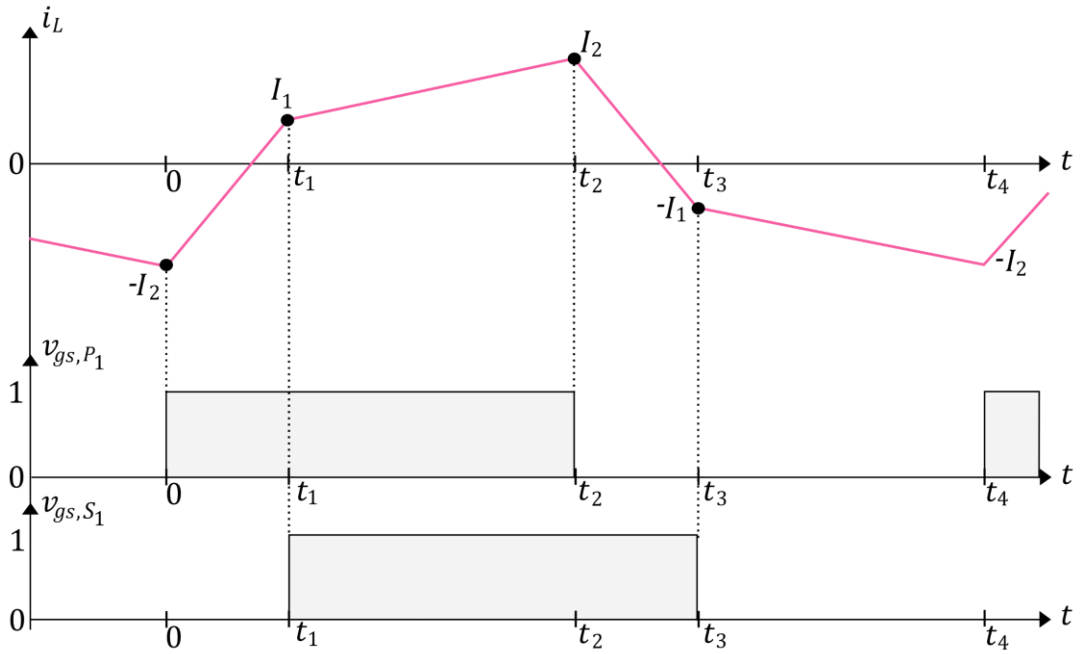
a) If $V_i > V'_o$ (buck mode):
   - $i_L(0) < 0$ and $i_L(t_1) < 0$ for light load operation (lower ϕ);
   - $i_L(0) < 0$ and $i_L(t_1) = 0$;
   - $i_L(0) < 0$ and $i_L(t_1) > 0$ for heavy load operation (higher ϕ);

b) If $V_i = V'_o$ (voltage match mode):
   - $i_L(0) < 0$ and $i_L(t_1) > 0$ for all $0 < \phi \leq 90$;

c) If $V_i < V'_o$ (boost mode):
   - $i_L(0) > 0$ and $i_L(t_1) > 0$ for light load operation (lower ϕ);

- $i_L(0) = 0$ and $i_L(t_1) > 0$;
- $i_L(0) < 0$ and $i_L(t_1) > 0$ for heavy load operation (higher ϕ);

Figure 14 – Inductor current waveform highlighting the switching currents.



Source: provided by the author, 2024.

From Figure 14, it can be seen that $i_L(0) = -I_2$, $i_L(t_1) = I_1$, $i_L(t_2) = I_2$, $i_L(t_3) = -I_1$ and $i_L(t_4) = i_L(0)$. Therefore, using the equation (3.5) in the intervals $(0,t_1)$ and (t_1,t_2), the linear system shown in equation (3.6) is obtained.

$$\begin{cases} i_L(t_1) = I_1 = \dfrac{1}{L}(V_i + V_o')\, t_1 - I_2 \\ i_L(t_2) = I_2 = \dfrac{1}{L}(V_i - V_o')\,(t_2 - t_1) + I_1 \end{cases} \tag{3.6}$$

Solving this system results in the expressions (3.7) and (3.8) for the switching currents I_1 and I_2, respectively.

$$I_1 = \frac{1}{4Lf_s}\left(2V_i\frac{|\phi|}{\pi} - V_i + V_o'\right) \tag{3.7}$$

$$I_2 = \frac{1}{4Lf_s}\left(2V_o'\frac{|\phi|}{\pi} + V_i - V_o'\right) \tag{3.8}$$

Notice that, I_2 is also the peak value of the inductor current when the converter is in buck mode. If the converter is in boost mode, I_1 is the peak value of the inductor current. With the equations for $v_{ab}(t)$ and $i_L(t)$, the power transmission can now be derived. By applying equations (3.2) and (3.5) in (3.1):

$$P = \frac{2}{T_s}\left[\int_0^{t_1} V_i\left(\frac{1}{L}(V_i + V_o')\,t - I_2\right)dt + \int_{t_1}^{t_2} V_i\left(\frac{1}{L}(V_i - V_o')(t - t_1) + I_1\right)dt\right] \tag{3.9}$$

Solving the integration in (3.9) results in the power transmission for the DAB operating with SPS modulation, shown in expression (3.10).

$$P = \frac{nV_iV_o}{2Lf_s}\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.10}$$

It can be seen in equation (3.10) that the power transmitted in the DAB converter depends on various parameters. Usually, some parameters are fixed in a power converter, such as the inductance L, switching frequency f_s and transformer's turns ratio n. The input voltage V_i and output voltage V_o may vary depending on the application.

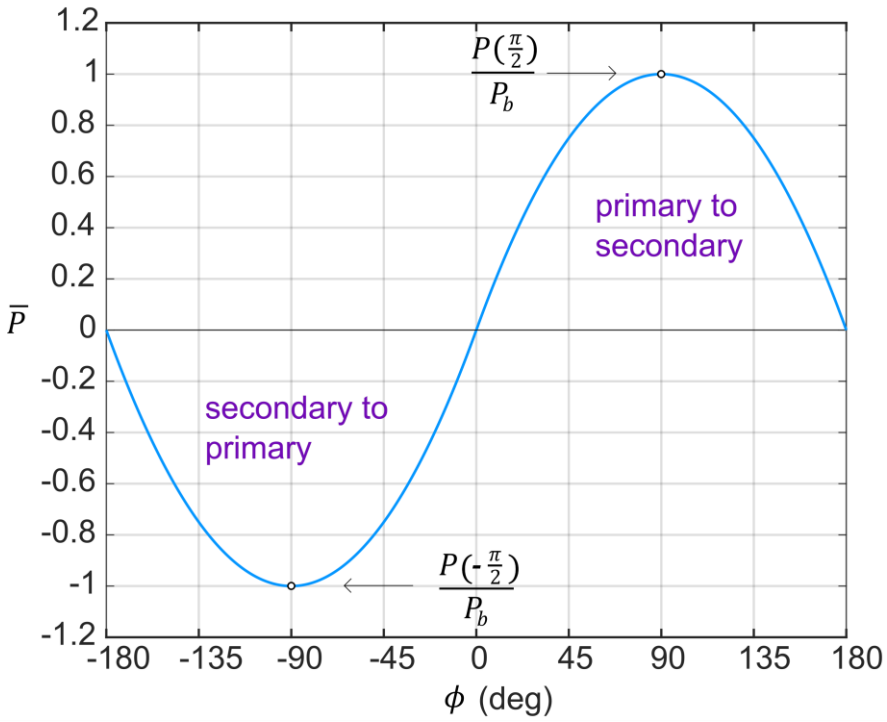
Considering fixed V_i and V_o, the phase-shift ϕ is the only variable for controlling the amount of active power transmitted. The direction of the power flow in the converter is defined by the sign of ϕ.

Defining P_b as the base value for the power transmitted by the converter as shown in equation (3.11), the normalized power transmission $\bar{P}$ can be obtained as equation (3.12). Figure 15 shows the plot of $\bar{P}$ versus ϕ (in degrees, for better visualization) ranging from $-\pi$ to π.

$$P_b = \frac{nV_iV_o}{8Lf_s} \tag{3.11}$$

$$\bar{P} = \frac{P}{P_b} = 4\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.12}$$

Figure 15 – Power Transmission versus Phase-Shift plot of DAB converter using SPS modulation.



Source: provided by the author, 2024.

From Figure 15, it can be noted that for both positive and negative power flow, the magnitude of the power transmission curve reaches its peak at $|\phi| = \pi/2$ (or 90°), which is equal to P_b. For every other value of power transmitted, there are two possible values of ϕ resulting in the same value of power transmitted. For ϕ equal to $-\pi$, 0 and π, the power transmission is theoretically zero.

For a given power transfer P, equation (3.10) can be rearranged as (3.13) to calculate the necessary phase-shift, as long as $0 < |P| \leq P_b$.

The function $sgn(x)$ is equal to 1, if $x > 0$; equal to 0, if $x = 0$; or equal to -1, if $x < 0$. For the case when $P = 0$, the phase-shift can assume either one of these values: $\phi = 0$, $\phi = \pi$ or $\phi = -\pi$.

$$\phi = sgn(P)\,\frac{\pi}{2}\left(1 \pm \sqrt{1 - \frac{8Lf_s|P|}{nV_iV_o}}\right) \tag{3.13}$$

3.3.2 Inductor Current

It can be seen in equation (3.4) that the shape of the inductor current depends on the voltages applied on its terminals, when L and n are constant. The average value of the inductor current is zero. The RMS value of the inductor current $I_{L,rms}$ is given by equation (3.14)

$$I_{L,rms} = \sqrt{\frac{2}{T_s}\int_0^{T_s/2} i_L^2(t)\, dt} \tag{3.14}$$

Applying equation (3.5) with the proper intervals, equation (3.14) becomes equation (3.15).

$$I_{L,rms} = \sqrt{\frac{2}{T_s}\left[\int_0^{t_1}\left(\frac{1}{L}(V_i + V_o')t - I_2\right)^2 dt + \int_{t_1}^{t_2}\left(\frac{1}{L}(V_i - V_o')(t - t_1) + I_1\right)^2 dt\right]} \tag{3.15}$$

Solving the integral in equation (3.15) results in the expression (3.16) for the RMS value of the inductor current.

$$I_{L,rms} = \frac{1}{2Lf_s}\sqrt{-\frac{2}{3}V_i V_o'\left(\frac{|\phi|}{\pi}\right)^3 + V_i V_o'\left(\frac{|\phi|}{\pi}\right)^2 + \left(\frac{V_i^2}{12} - \frac{V_i V_o'}{6} + \frac{{V_o'}^2}{12}\right)} \tag{3.16}$$

The current $I_{L,rms}$ can be normalized. Rearranging equation (3.16) into (3.17):

$$I_{L,rms}^2 = \frac{1}{48}\frac{1}{L^2 f_s^2}\left[-8V_i V_o'\left(\frac{|\phi|}{\pi}\right)^3 + 12V_i V_o'\left(\frac{|\phi|}{\pi}\right)^2 + (V_i - V_o')^2\right] \tag{3.17}$$

By assuming V_i and n constant and substituting the voltage conversion ratio $K = V_o'/V_i$ into (3.17), equation (3.18) is obtained.

$$I_{L,rms}^2 = \frac{1}{48}\frac{1}{L^2 f_s^2} V_i^2 \left[-8K\left(\frac{|\phi|}{\pi}\right)^3 + 12K\left(\frac{|\phi|}{\pi}\right)^2 + (1-K)^2\right] \quad (3.18)$$

A base value for the RMS value of the inductor current $I_{L,b}$ can be defined with equation (3.19), the normalized RMS value of the inductor current $\overline{I_L}$ can be found with equation (3.20), resulting in expression (3.21).

$$I_{L,b} = \frac{V_i}{4Lf_s} \quad (3.19)$$

$$\overline{I_L^2} = \frac{I_{L,rms}^2}{I_{L,b}^2} \quad (3.20)$$

$$\overline{I_L} = \sqrt{\frac{1}{3}\left[-8K\left(\frac{|\phi|}{\pi}\right)^3 + 12K\left(\frac{|\phi|}{\pi}\right)^2 + (1-K)^2\right]} \quad (3.21)$$

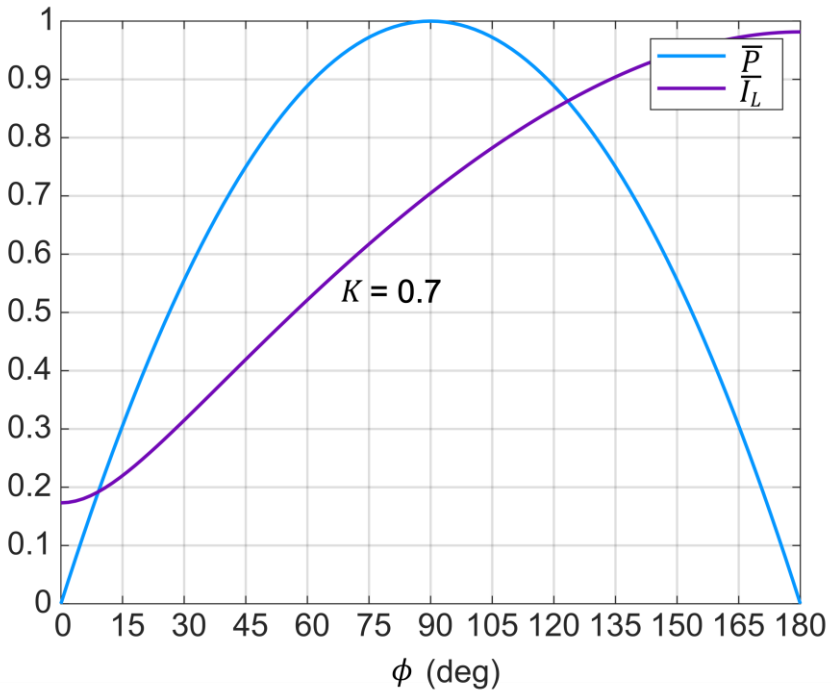
Figure 16 presents the plot of $\overline{I_L}$ and $\bar{P}$ versus $\phi \in [0, \pi]$, since negative values of ϕ results in the same curve but with negative values in the y-axis. The plot shows that the RMS value of the inductor current only gets larger with the increase of the phase-shift. Therefore, for practical implementation, it is recommended that ϕ is limited to $\left[-\frac{\pi}{2}, \frac{\pi}{2}\right]$ for higher efficiency and less stress in the components, since values of $\left[-\pi, -\frac{\pi}{2}\right]$ and $\left[\frac{\pi}{2}, \pi\right]$ will result in the same power transmission but with increased losses.

The value of K indicates which mode the AC-link is operating (reminder that $K = nV_o/V_i$). The possibilities are: $K < 1$ (buck mode), $K = 1$ (voltage match) and $K > 1$ (boost mode).

Substituting K in equation (3.11), the base value of the power transmission becomes equation (3.22). Thus, it should be kept in mind that as K (i.e., V_o) varies, the maximum power transmitted also varies. Figure 17 presents the normalized current $\overline{I_L}$ versus ϕ for different values of K.

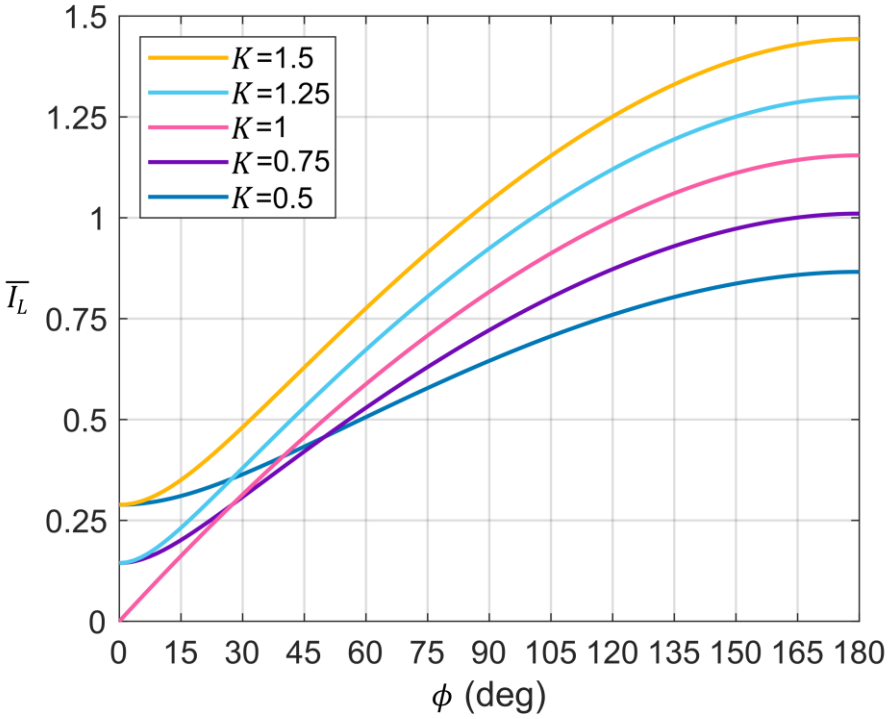
$$P_b = \frac{nV_iV_o}{8Lf_s} = \frac{V_i^2}{8Lf_s}K \quad (3.22)$$

Figure 16 – Normalized RMS value of i_L versus ϕ plot.



Source: provided by the author, 2024.

Figure 17 – Normalized RMS value of i_L versus ϕ plot for different values of K.



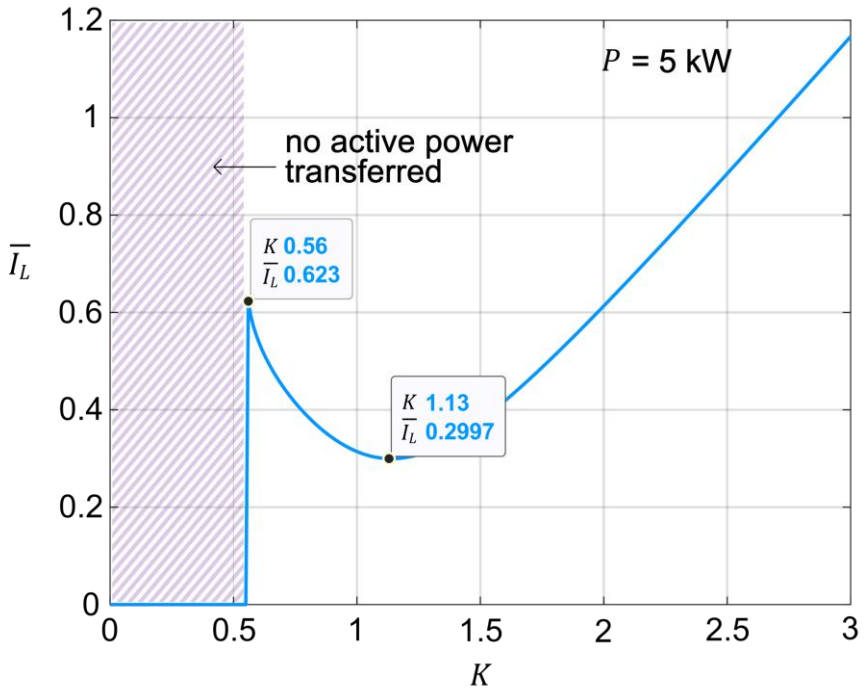
Source: provided by the author, 2024.

It can be seen in Figure 17 that when $K = 1$, the current $I_{L,rms}$ is lower at light-load (i.e., lower ϕ) than for $K \neq 1$. Furthermore, for $K \neq 1$, there is always current circulating in the inductor, even when there is no active power being transferred to the load (i.e., $\phi = 0$). This means that there is only non-active power being processed by the converter, which results in losses. Obviously, higher values of $I_{L,rms}$ are expected as ϕ increases when $K > 1$, since P_b will be larger.

Figure 18 presents the current $\overline{I_L}$ versus K for a numerical simulation with fixed P = 5 kW. For the chosen converter parameters, the converter is not able to transfer power when $K < 0.56$. From the plotted curve, it can be noted that the current $I_{L,rms}$ has a minimum value when $K = 1.13$. For every other value of K, $I_{L,rms}$ will increase, even if the output power remains the same, decreasing efficiency.

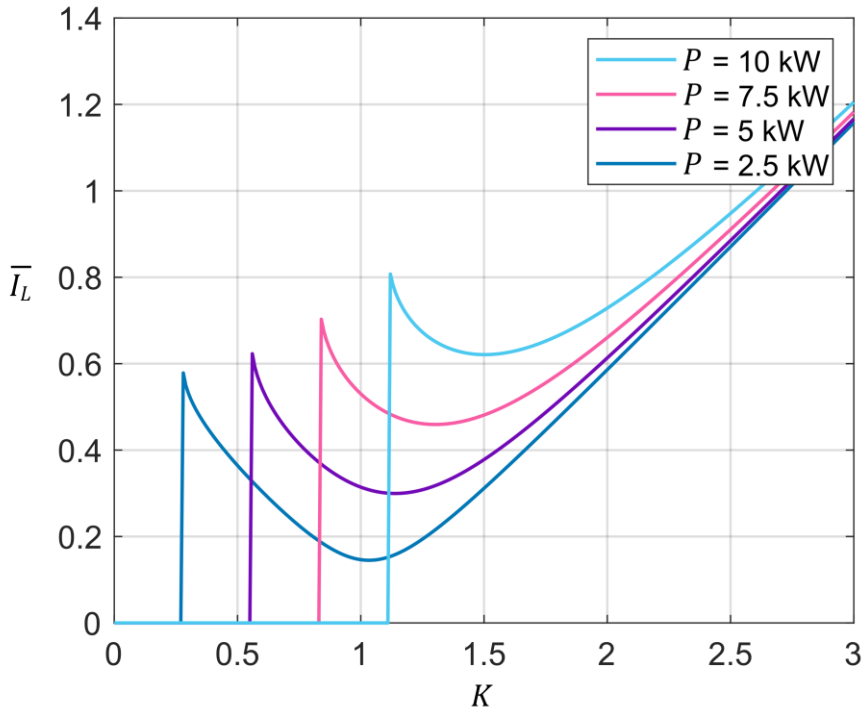
Figure 19 shows that the minimum value of $I_{L,rms}$ is reached with different values of K for different power levels.

Figure 18 – Plot of $\overline{I_L}$ versus K for $P = 5\ kW$. Parameters of the converter are: $V_i = 100\ V, n = 1, L = 13.88\ \mu H$ and $f_s = 10\ kHz$.



Source: provided by the author, 2024.

Figure 19 – Plot of $\overline{I_L}$ versus K for different values of P. Parameters of the converter are: $V_i = 100\ V, n = 1, L = 13.88\ \mu H$ and $f_s = 10\ kHz$.



Source: provided by the author, 2024.

3.3.3 Input and Output Currents

The average value of the input current I_i of the converter seen by the input voltage source is given by equation (3.23).

$$I_i = \frac{P_i}{V_i} = \frac{P}{V_i} \rightarrow I_i = \frac{nV_o}{2Lf_s}\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.23}$$

The first half of the input current waveform is the same as the inductor current waveform, as seen in Figure 11. Therefore, the RMS value of the input current $I_{i,rms}$ is equal to $I_{L,rms}$.

$$I_{i,rms} = \sqrt{\frac{2}{T_s}\int_0^{T_s/2} i_i^2(t)\,dt} = I_{L,rms} \tag{3.24}$$

The RMS value of the secondary current $I_{2,rms}$ is given by equation (3.25)

$$I_{2,rms} = \sqrt{\frac{2}{T_s}\int_0^{T_s/2} n^2 i_L^2(t)\, dt} = nI_{L,rms} \tag{3.25}$$

In the same manner, the RMS value of the output current $I_{o,rms}$ seen by the output capacitor is equal to $I_{2,rms}$.

$$I_{o,rms} = \sqrt{\frac{2}{T_s}\int_0^{T_s/2} i_o^2(t)\, dt} = I_{2,rms} \tag{3.26}$$

The average value of the output current I_o is given by equation (3.27).

$$I_o = \frac{P_o}{V_o} = \frac{P}{V_o} \quad \rightarrow \quad I_o = \frac{nV_i}{2Lf_s}\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.27}$$

3.3.4 Circulating Power

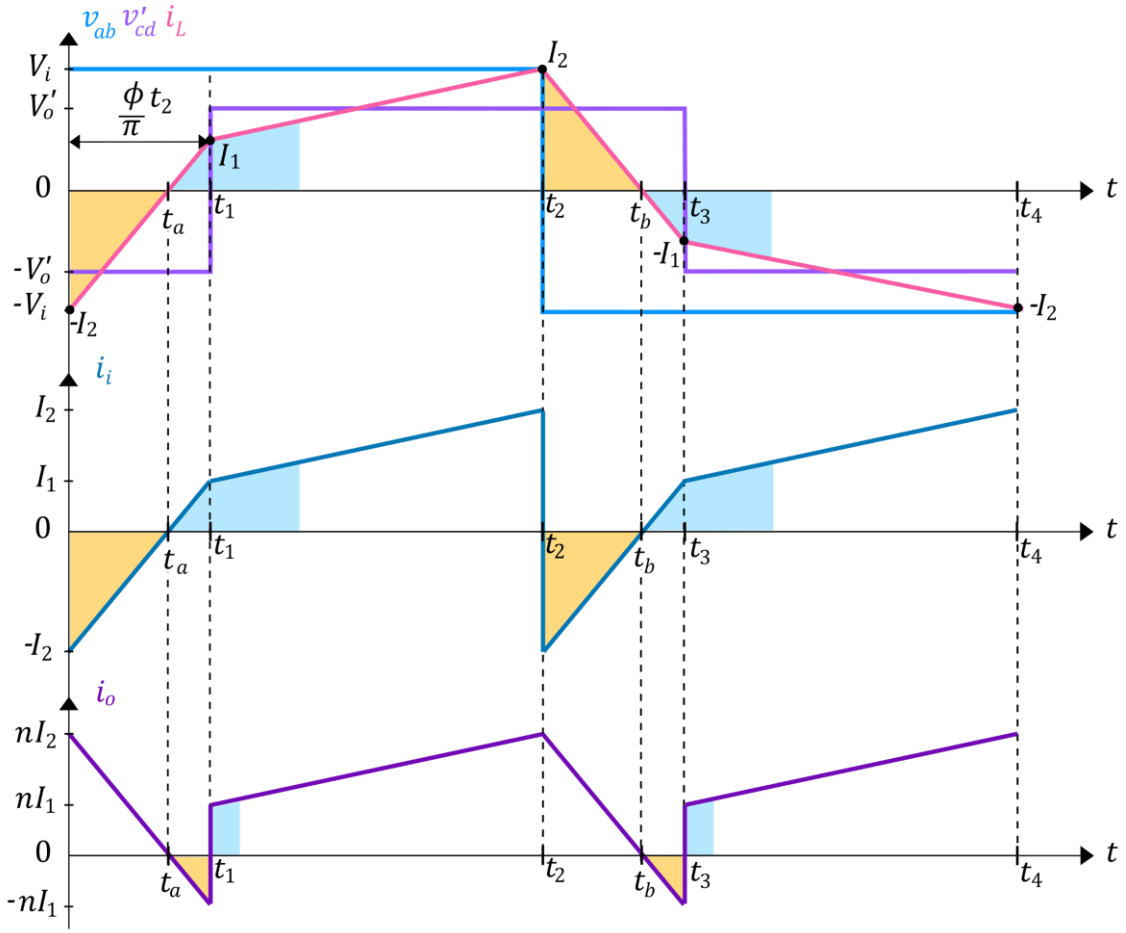
Bai and Mi (2008) defined the portion of instantaneous power that is flowing back to the input source as “reactive power”, which happens when the polarity of $i_L(t)$ is different from $v_{ab}(t)$. In this Master’s thesis, the term “circulating power” will be used to identify this phenomenon. The analysis done in this section is valid for $\phi > 0$.

In Figure 20, the generation of circulating power Q_c is illustrated, considering buck mode. From 0 to t_a and from t_2 to t_b, i_L has different polarity than $v_{ab}(t)$. The orange shaded area is the resulting circulating power.

To maintain the desired active power transmission, the converter has to compensate for this circulating power, which is the blue shaded area. According to Bai and Mi (2008), this portion of power does not contribute to the power transmitted to the load, it only increases conduction losses because of larger $I_{L,rms}$.

It can also be seen that during the circulating power generation, the input current is negative, which means that power is being sent back to the input source. According to the definitions made in Figure 3: $i_i(t) < 0$ means the current is entering the source V_i and $i_o(t) < 0$ means the current is leaving source V_o.

Figure 20 – Circulating power generation, waveforms for $i_L(0) < 0$ and $i_L(t_1) > 0$, for buck mode.



Source: provided by the author, 2024.

Analyzing Figure 20, the following points can be concluded:

- When $sgn(i_L(t)) \neq sgn(v_{ab}(t))$, part of the energy stored in the inductor is sent back to the input source, and the other part is delivered to the output source (load), since $i_i(t) < 0$ and $i_o(t) > 0$.
- When $sgn(i_L(t)) \neq sgn(v'_{cd}(t))$, the output source sends energy back, i.e., when $i_o(t) < 0$. At the same time, the input source is also

delivering energy. Since none of the voltage sources are consuming power, this energy simply “circulates” through the inductor.

For the buck and voltage match modes, the current $i_L(0)$ is always negative. Equation (3.28) defines the circulating power.

$$Q_c = 2\frac{V_i}{T_s}\int_{t_2}^{t_b} i_L(t)dt \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.28}$$

The instant t_a can be calculated with equation (3.29).

$$t_a = \frac{1}{4f_s}\frac{\left(V_i + V_o'\left(2\frac{\phi}{\pi} - 1\right)\right)}{(V_i + V_o')} \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.29}$$

Since $t_b - t_2 = t_a$, equation (3.28) can be rewritten as equation (3.30)

$$Q_c = 2\frac{V_i}{T_s}\int_0^{t_a}\left(\frac{(-V_i - V_o')}{L}t + I_2\right)dt \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.30}$$

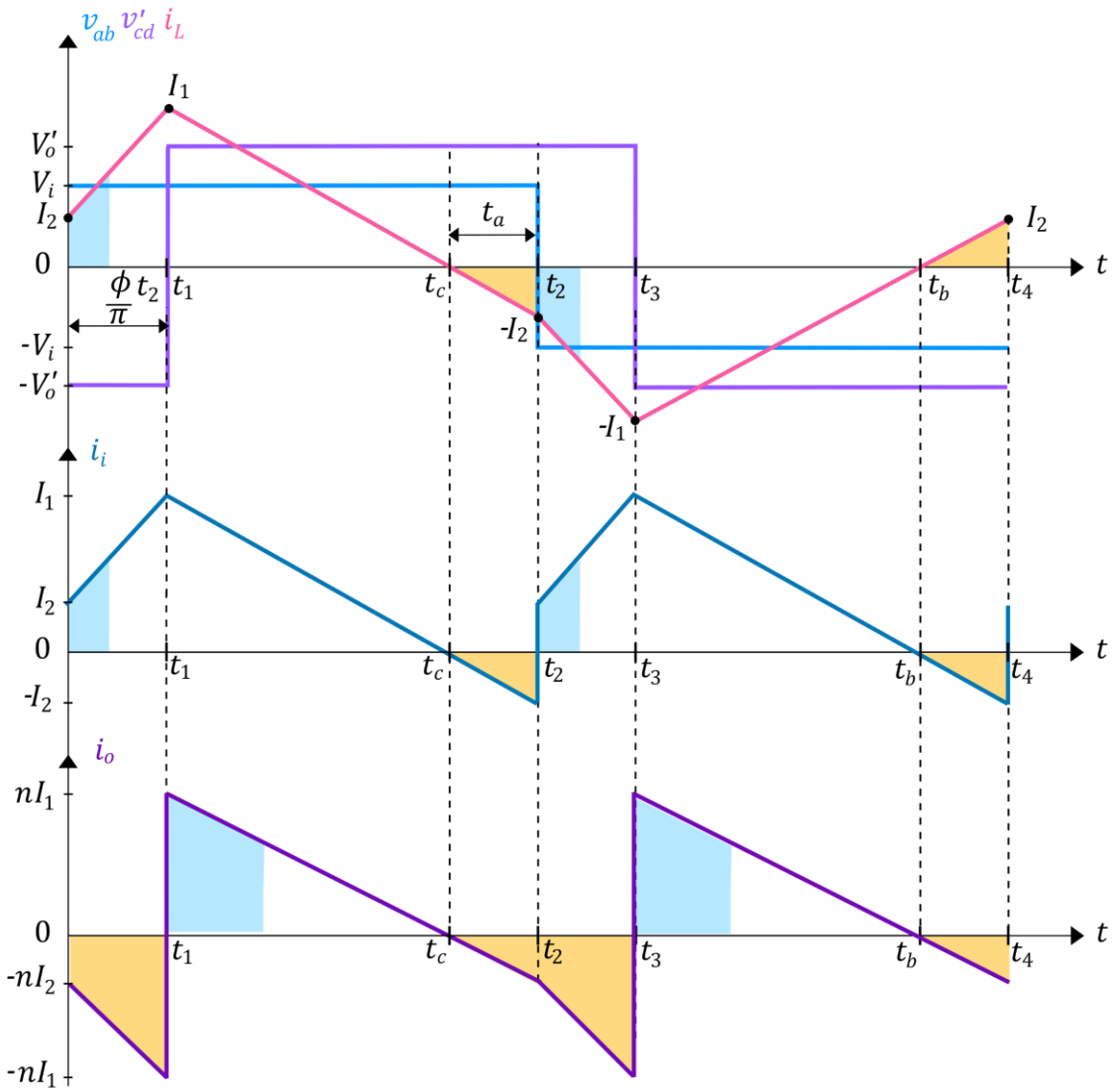
Substituting equation (3.29) in (3.30), the expression (3.31) is deduced, which can be used to compute the circulating power when $i_L(0) < 0$ and $i_L(t_1) > 0$. In this case, Q_c is positive, which can be understood as inductive circulating power since the current is lagging the voltage.

$$Q_c = \frac{V_i}{16Lf_s}\frac{\left(V_i + V_o'\left(2\frac{\phi}{\pi} - 1\right)\right)^2}{(V_i + V_o')} \quad \forall \quad i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.31}$$

For the boost mode, there are three possibilities for the initial current value $i_L(0)$: $-I_2$, 0 or I_2. When $i_L(0) < 0$, equations (3.28), (3.29), (3.30) and (3.31) are valid. If $i_L(0) = 0$, then $t_a = 0$ and thus, $Q_c = 0$. Figure 21 illustrates the case when $i_L(0) > 0$. It can be seen that:

- When both $i_i(t)$ and $i_o(t)$ are negative (intervals (t_c, t_2) and (t_b, t_4)), the input source is receiving energy from the output source;
- The output source keeps sending energy back at the periods $(0, t_1)$ and (t_2, t_3). This energy simply circulates through the inductor, since the input source is not consuming active power.

Figure 21 – Circulating power generation, waveforms for $i_L(0) > 0$ and $i_L(t_1) > 0$, in boost mode.



Source: provided by the author, 2024.

Equation (3.32) defines the circulating power for this case.

$$Q_c = 2\frac{V_i}{T_s}\int_{t_c}^{t_2} i_L(t)dt \;\; \forall \;\; i_L(0) > 0 \;\wedge\; i_L(t_1) > 0 \tag{3.32}$$

For $i_L(0) > 0$, the period t_a can be calculated with equation (3.33). Equation (3.32) can be written as equation (3.34).

$$t_a = \frac{1}{4f_s}\frac{\left(V_o'\left(1 - 2\frac{\phi}{\pi}\right) - V_i\right)}{(V_i - V_o')} \;\; \forall \;\; i_L(0) > 0 \;\wedge\; i_L(t_1) > 0 \tag{3.33}$$

$$Q_c = 2\frac{V_i}{T_s}\int_0^{t_a} \frac{(V_i - V_o')}{L} t \; dt \;\; \forall \;\; i_L(0) > 0 \;\wedge\; i_L(t_1) > 0 \tag{3.34}$$

Finally, solving the integral in equation (3.34) results in the expression (3.35), which can be used to calculate the circulating power when $i_L(0) > 0$ and $i_L(t_1) > 0$. In this case, Q_c is negative, meaning it is capacitive circulating power since the current is leading the voltage.

$$Q_c = \frac{V_i}{16Lf_s}\frac{\left(V_o'\left(1 - 2\frac{\phi}{\pi}\right) - V_i\right)^2}{(V_i - V_o')} \;\; \forall \;\; i_L(0) > 0 \;\wedge\; i_L(t_1) > 0 \tag{3.35}$$

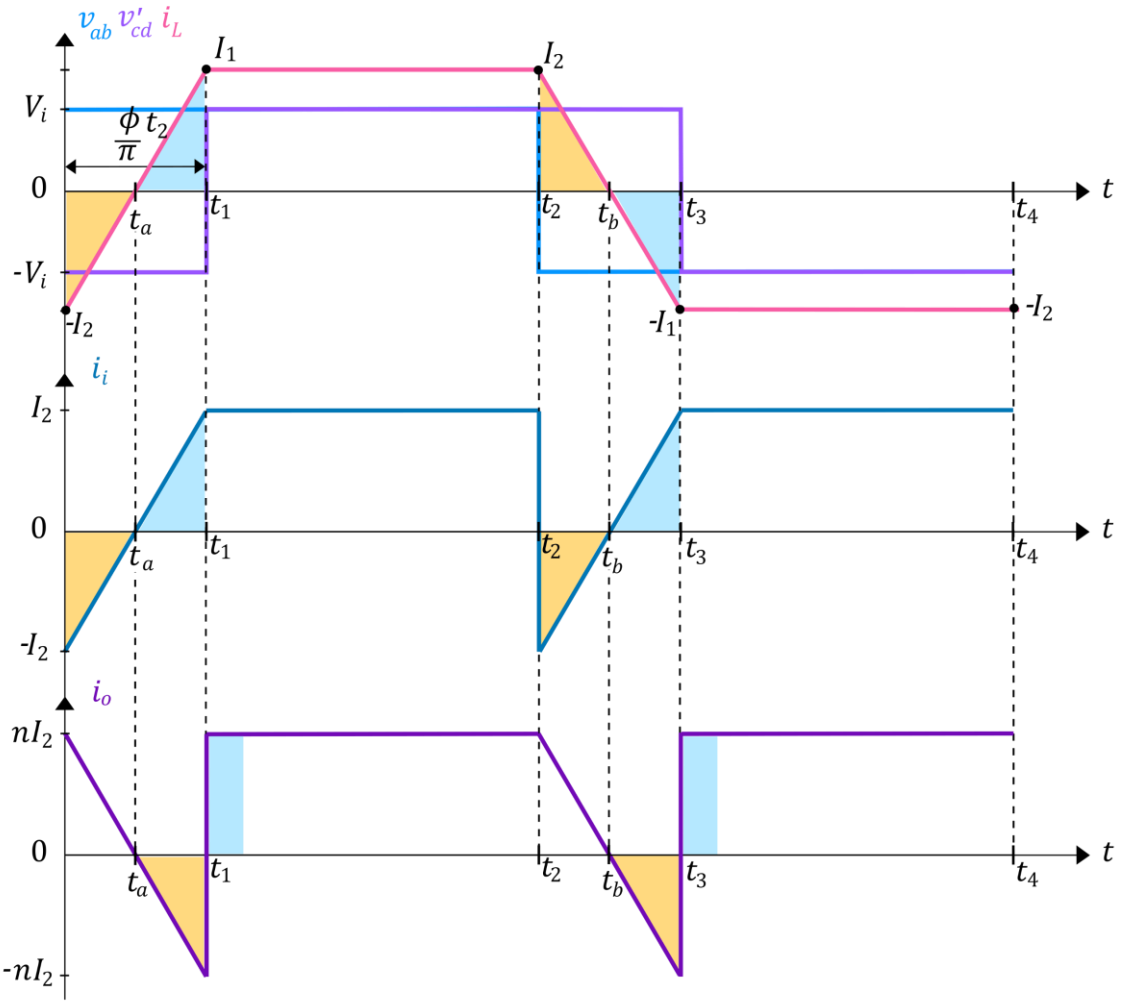
Figure 22 illustrates the case for the voltage match mode. A couple of conclusions can be drawn:

- Both input and output sources receive energy from the inductor during the periods $(0, t_a)$ and (t_2, t_b), since $i_i(t) < 0$ and $i_o(t) > 0$;
- The output source sends energy back to the inductor during periods (t_a, t_1) and (t_b, t_3), since $i_o(t) < (0)$, but the input source does not consume any active power, since $i_i(t) > 0$;
- The circulating power can be calculated with equation (3.31).

It is important to note that, the equations deduced for Q_c are not valid for the case when both $i_L(0)$ and $i_L(t_1)$ are negative, which can occur when ϕ is small enough. In this case, the expression for the circulating power is more

complex to derive, because the inductor current has two different states before it reaches zero. The result is shown in equation (3.36).

Figure 22 – Circulating power generation for voltage match mode.



Source: provided by the author, 2024.

$$Q_c = \frac{1}{16Lf_s}\frac{V_i}{(-V_i + V_o')}\left(\left(4{V_o'}^2 - 8V_iV_o'\right)\left(\frac{\phi}{\pi}\right)^2 + 4\left(V_iV_o' - {V_o'}^2\right)\left(\frac{\phi}{\pi}\right) - (V_i - V_o')^2\right) \quad (3.36)$$

$$\forall\ i_L(0) < 0 \ \wedge\ i_L(t_1) < 0$$

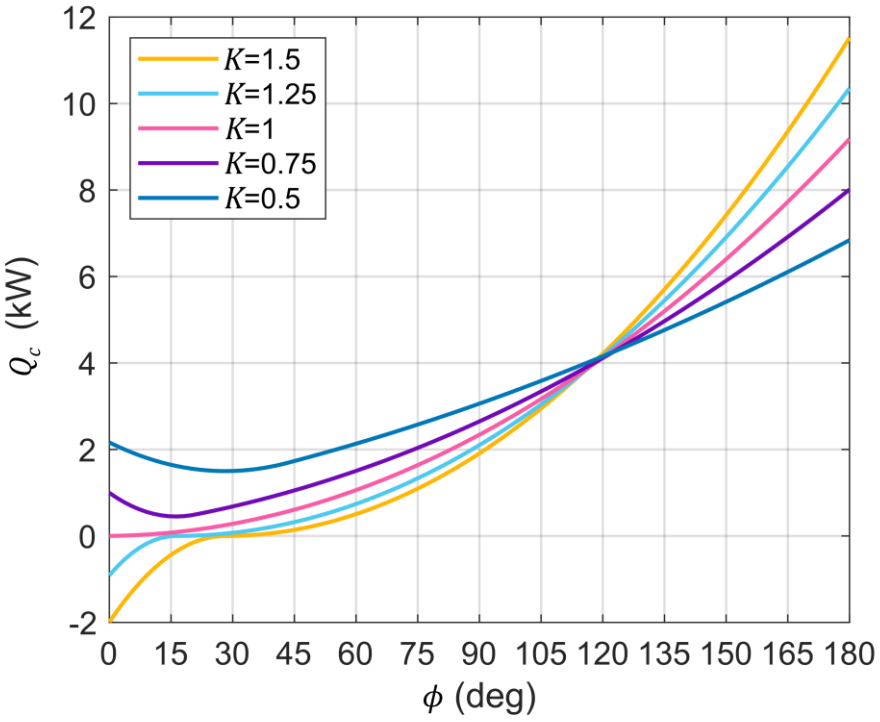
It can be seen in equations (3.31) and (3.35) that the only situation when $Q_c = 0$ is when $V_i = V_o'\left(1 - 2\frac{\phi}{\pi}\right)$, which results in $i_L(t_1) = 0$. Equation (3.36) is more difficult to analyze. It can be concluded that SPS modulation cannot control circulating power.

Figure 23 presents the plot of $Q_c \, x \, \phi$ for some values of K. For the simulated case, it can be seen that during buck mode, the converter always has inductive circulating power.

When $V_o' = V_i$, there is no circulating power for $\phi = 0$.

In boost mode, there is capacitive circulating power for $\phi < \pi/6 \, rad$. For $\phi \approx \pi/12 \, rad$ and $\phi \approx \pi/6 \, rad$, there is no circulating power when $K = 1.25$ and $K = 1.5$, respectively, since $I_2 = 0$. For $\phi > \pi/6 \, rad$, the converter always operates with inductive circulating power.

Figure 23 – Circulating power plot versus phase-shift, for different values of K. Parameters of the converter are: $V_i = 100 \, V, n = 1, L = 13.88 \, \mu H$ and $f_s = 10 \, kHz$.



Source: provided by the author, 2024.

3.3.5 Transformer VA Rating

Considering L as the leakeage inductance of the transformer, the transformer VA rating, or apparent power of the transformer S_T, is given by equation (3.37) (De Doncker; Divan; Kheraluwala, 1991). The RMS value of a

rectangular-shaped waveform with 50% duty cycle and zero average value is equal to its amplitude, resulting in equation (3.38).

$$S_T = \frac{1}{2}\left(V_{ab,rms} I_{L,rms} + V_{cd,rms} I_{2,rms}\right) \tag{3.37}$$

$$S_T = \frac{1}{2}\left(V_i I_{L,rms} + V_o n I_{L,rms}\right) = \frac{1}{2} I_{L,rms}(V_i + V_o') \tag{3.38}$$

Substituting equation (3.16) in (3.38) results in equation (3.39):

$$S_T = \frac{(V_i + V_o')}{4 L f_s} \sqrt{-\frac{2}{3} V_i V_o' \left(\frac{|\phi|}{\pi}\right)^3 + V_i V_o' \left(\frac{|\phi|}{\pi}\right)^2 + \left(\frac{V_i^2}{12} - \frac{V_i V_o'}{6} + \frac{V_o'^{\,2}}{12}\right)} \tag{3.39}$$

The non-active power of the transformer N_T, defined by equation (3.40), results in a big expression and is difficult to be derived. Figure 24 presents the plot of S_T, N_T and P as a function of ϕ. N_T is plotted by numerical simulation, as presented in equation (3.40).

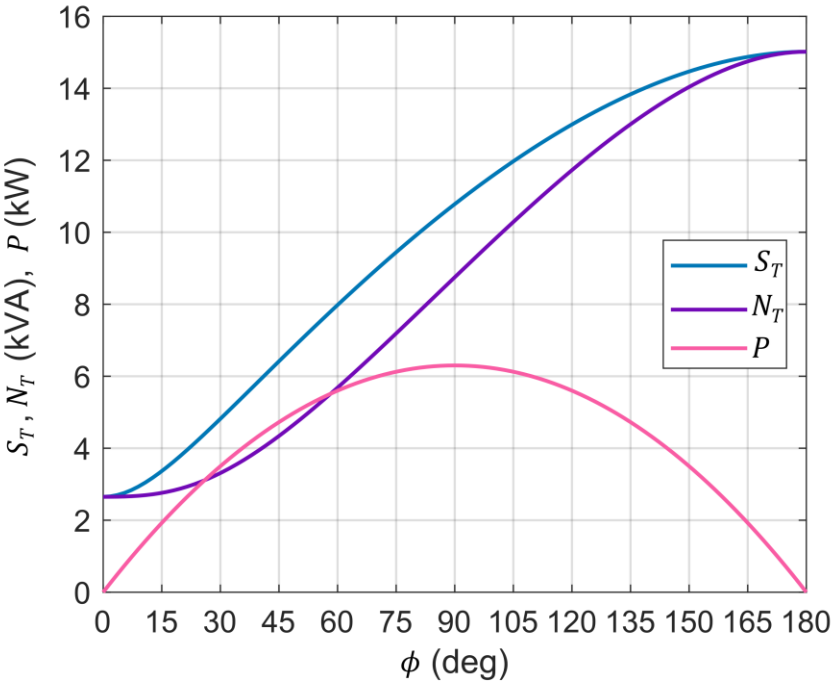
$$N_T = \sqrt{S_T^2 - P^2} = \sqrt{Q_T^2 + D_T^2} \tag{3.40}$$

It can be seen in Figure 24 that, for the simulated case ($K = 0.7$), most of the power flowing in the transformer throughout the phase-shift range is non-active power. Only a small interval of ϕ results in more active power than non-active power being transferred. This shows that most of the apparent power in the transformer only generates losses when $K \neq 1$.

De Doncker, Divan, Kheraluwala (1991) presented the transformer VA rating $S_{T,f}$ by considering only the fundamental component of $v_{ab}(t)$ and $v_{cd}(t)$, allowing mathematical operations with phasors which are easier to manipulate. The expression is presented in equation (3.41), plotted in Figure 25.

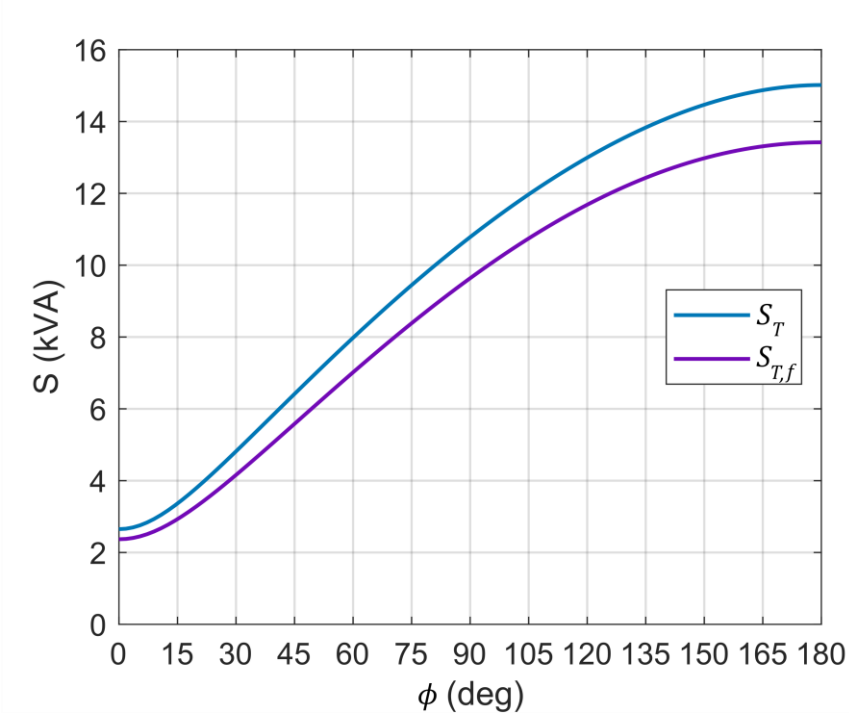
$$S_{T,f} = \left(\frac{2\sqrt{2}}{\pi} V_i\right)^2 \frac{(1+K)}{4\pi f_s L} \sqrt{K^2 - 2K\,cos(\phi) + 1} \tag{3.41}$$

Figure 24 - Power plot of the transformer as function of ϕ, for $V_o = 70\ V$ $(K = 0.7)$. $V_i = 100\ V, n = 1, L = 13.88\ \mu H$ and $f_s = 10\ kHz$.



Source: provided by the author, 2024.

Figure 25 – Comparison of Transformer VA rating equations, for $K = 0.7$. $V_i = 100\ V, n = 1, L = 13.88\ \mu H$ and $f_s = 10\ kHz$.

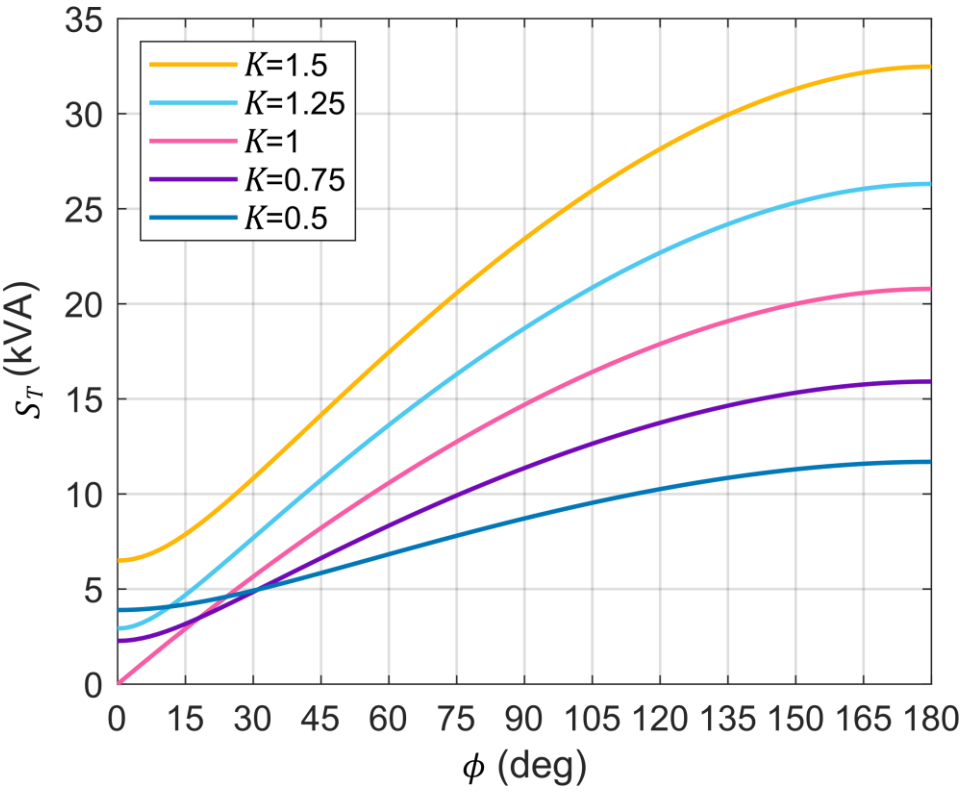


Source: provided by the author, 2024.

It can be seen in Figure 25 that in the simulated case, S_T is slightly higher than $S_{T,f}$ for all of the phase-shift range. The difference is expected, since the derivation of $S_{T,f}$ does not takes into account all of the harmonic components existing in the voltages because of the switching nature of the converter. Therefore, S_T should be used when an accurate estimative is necessary.

Figure 26 presents the power S_T as a function of ϕ for different values of K. When no active power is being transferred (i.e., $\phi = 0$), the only case when there is no power circulating in the transformer is when $V_i = nV_o$ ($K = 1$), which is also the case that results in the smaller non-active power at lower ϕ values. This is expected, since it was already demonstrated in Figure 17 when the behavior of $I_{L,rms}$ was presented.

Figure 26 – Transformer power rating S_T as function of ϕ, for different values of K. Parameters of the converter are: $V_i = 100\ V, n = 1, L = 13.88\ \mu H$ and $f_s = 10\ kHz$.



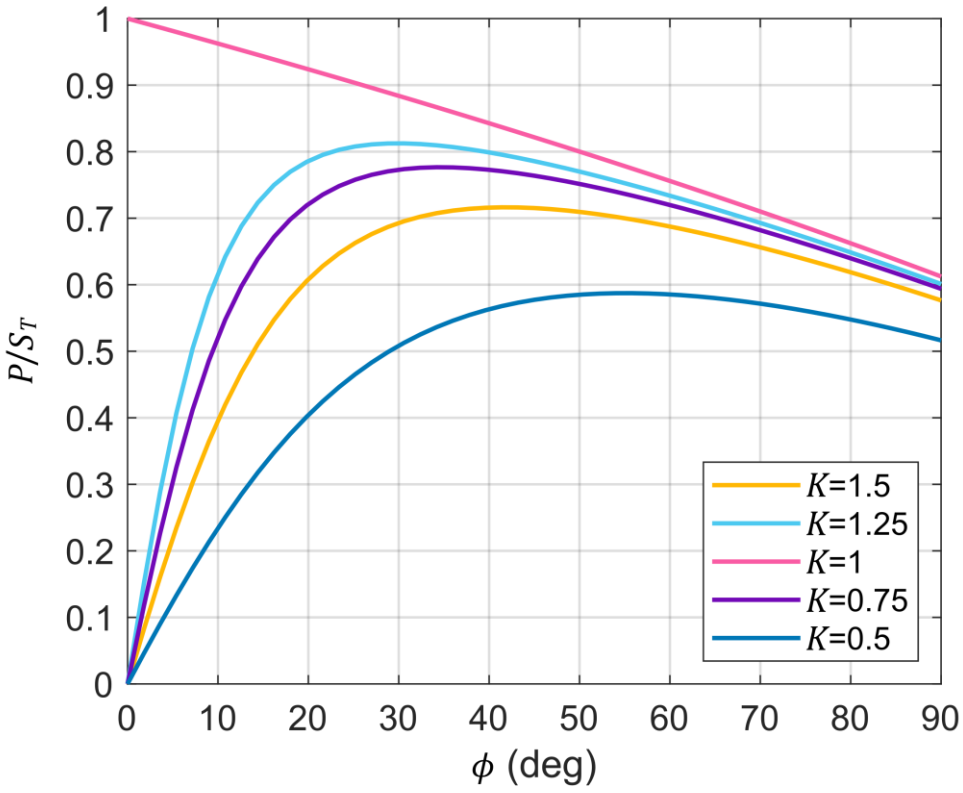
Source: provided by the author, 2024.

For $\phi = 0$, if $V_i = nV_o$, the inductor voltage V_L is zero, which is why the non-active power N_T is also zero. When $V_i \neq nV_o$, $V_L \neq 0$ and therefore, non-active power circulates through the transformer.

The transformer utilization factor, defined as P/S_T (De Doncker; Divan; Kheraluwala, 1991), is a useful figure of merit to determine how much of the apparent power in the transformer actually is active power being transferred to the load. Figure 27 shows the P/S_T as function of ϕ, limited from 0 (no active power) to $\pi/2$ (maximum active power), for different values of K.

It can be observed in Figure 27 that the case with the best transformer utilization factor is when $K = 1$ (i.e., $V_i = nV_o$). Any other value for K results in worse transformer utilization for all of the phase-shift range.

Figure 27 – Transformer utilization factor as function of ϕ for different values of K. Parameters of the converter are: $V_i = 100\ V, n = 1, L = 13.88\ \mu H$, and $f_s = 10\ kHz$.



Source: provided by the author, 2024.

3.3.6 Semiconductors Stresses

For designing the converter, the blocking voltage, the average and RMS values of the current flowing through the semiconductors must be known.

To derive the expressions for the current, a power switch will be divided into two components: a unidirectional switch and a diode in antiparallel. In a MOSFET, a unidirectional switch would be the drain-source channel, while the antiparallel diode would be the intrinsic body-diode. Therefore, both components' stresses must be taken into account to design the power switch.

According to the waveforms of Figure 11 obtained earlier in the converter analysis, Figure 28 presents the current waveforms through the semiconductors in the primary and secondary bridge. Time instants are given by Table 3.

It can be observed in Figure 28 that, due to the symmetric operation of the DAB converter, each semiconductor pair (odd or even numbers) have the same current waveform, although at different intervals. Therefore, only one expression for each semiconductor is necessary to calculate the average of the current. This is defined through equations (3.42) to (3.45), where: I_P is the average value of the current in the switches of the primary bridge, I_{DP} is the average value of the current in the diodes of the primary bridge, I_S is the average value of the current in the switches of the secondary bridge and I_{DS} is the average value of the current in the diodes of the secondary bridge

$$I_{P_1} = I_{P_2} = I_{P_3} = I_{P_4} = I_P \tag{3.42}$$

$$I_{DP_1} = I_{DP_2} = I_{DP_3} = I_{DP_4} = I_{DP} \tag{3.43}$$

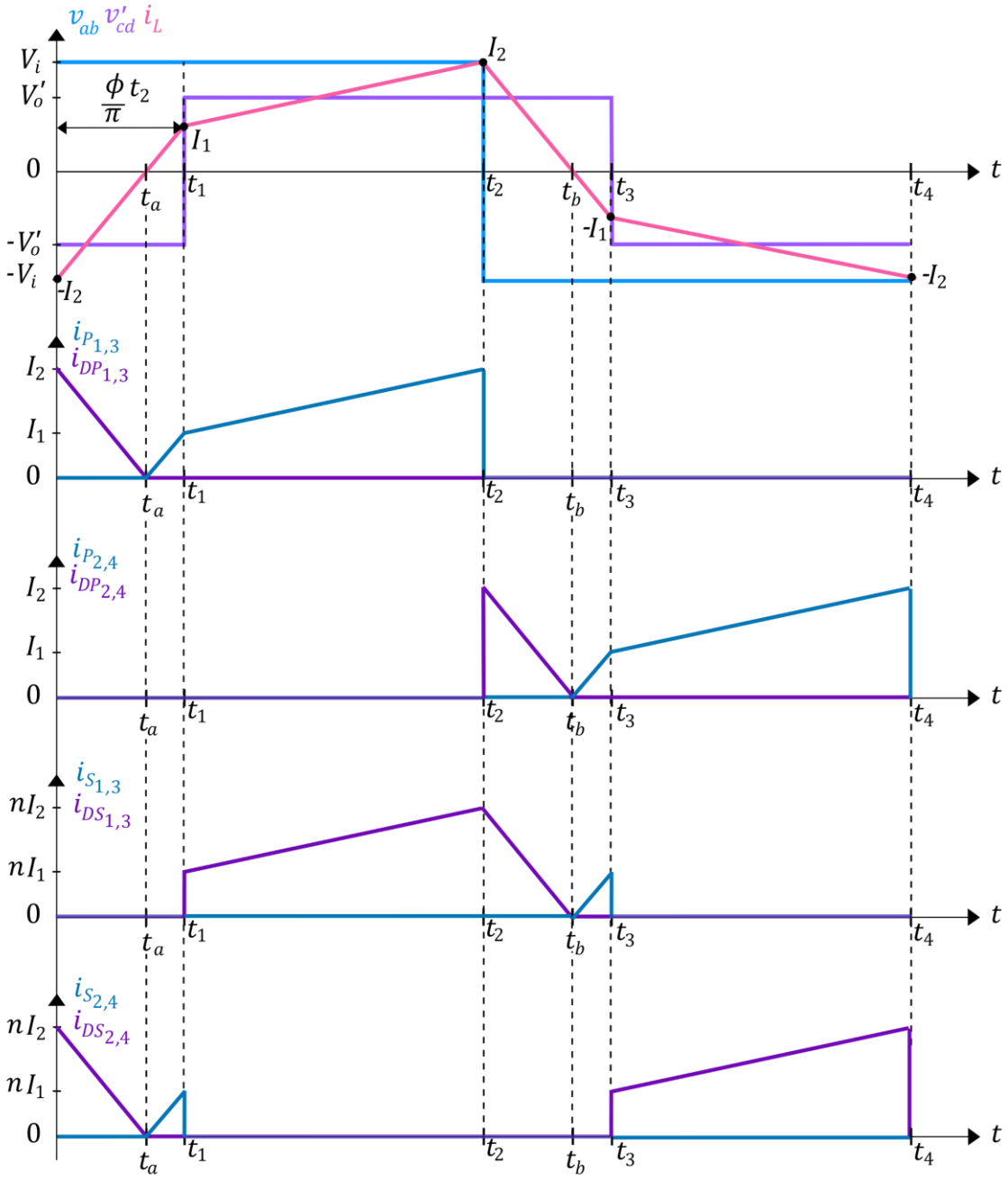
$$I_{S_1} = I_{S_2} = I_{S_3} = I_{S_4} = I_S \tag{3.44}$$

$$I_{DS_1} = I_{DS_2} = I_{DS_3} = I_{DS_4} = I_{DS} \tag{3.45}$$

The currents I_P and I_{DP} can be computed by using equation (3.46) and (3.47), respectively. Time instant t_a can be calculated with equation (3.29).

$$I_P = \frac{1}{T_s}\left[\int_0^{(t_1-t_a)} \frac{(V_i + V_o')}{L}\, t\, dt + \int_{t_1}^{t_2} \left(\frac{(V_i - V_o')}{L}(t - t_1) + I_1\right)\, dt\right] \tag{3.46}$$

Figure 28 – Current waveforms in the semiconductors for buck mode, $i_L(0) < 0$ and $i_L(t_1) > 0$, for buck mode.



Source: provided by the author, 2024.

$$I_{DP} = \frac{1}{T_s}\int_0^{t_a}\left(-\frac{(V_i + V_o')}{L}t + I_2\right)dt \tag{3.47}$$

The currents I_S and I_{DS} can be computed by using equation (3.48) and (3.49), respectively. Time instant t_a can be calculated with equation (3.29).

$$I_S = \frac{1}{T_s}\int_0^{(t_1-t_a)} n\frac{(V_i + V_o')}{L}\, t\, dt \tag{3.48}$$

$$I_{DS} = \frac{1}{T_s}\left[\int_0^{t_a}\left(-n\frac{(V_i + V_o')}{L}t + nI_2\right) dt + \int_{t_1}^{t_2}\left(n\frac{(V_i - V_o')}{L}(t - t_1) + nI_1\right)\ dt\right] \tag{3.49}$$

The considerations done for the average value of the current can also be done to the RMS value of the current in the semiconductors. Equations (3.50) and (3.51) defines the RMS value of the current in the switches ($I_{P,rms}$) and in the diodes ($I_{DP,rms}$) of the primary bridge, respectively. Equations (3.52) and (3.53) defines the RMS value of the current in the switches ($I_{S,rms}$) and in the diodes ($I_{SP,rms}$) of the secondary bridge, respectively.

$$I_{P,rms} = \sqrt{\frac{1}{T_s}\left[\int_0^{(t_1-t_a)}\left(\frac{(V_i + V_o')}{L}t\right)^2 dt + \int_{t_1}^{t_2}\left(\frac{(V_i - V_o')}{L}(t - t_1) + I_1\right)^2\ dt\right]} \tag{3.50}$$

$$I_{DP,rms} = \sqrt{\frac{1}{T_s}\int_0^{t_a}\left(-\frac{(V_i + V_o')}{L}t + I_2\right)^2 dt} \tag{3.51}$$

$$I_{S,rms} = \sqrt{\frac{1}{T_s}\int_0^{(t_1-t_a)}\left(n\frac{(V_i + V_o')}{L}t\right)^2\ dt} \tag{3.52}$$

$$I_{DS,rms} = \sqrt{\frac{1}{T_s}\left[\int_0^{t_a}\left(-n\frac{(V_i + V_o')}{L}t + nI_2\right)^2 dt + \int_{t_1}^{t_2}\left(n\frac{(V_i - V_o')}{L}(t - t_1) + nI_1\right)^2 dt\right]} \tag{3.53}$$

Solving the equations (3.46) through (3.53) can lead to the analytical expressions for the average and RMS values of the current in the semiconductors. Due to the length those derived expressions have, they are shown in Appendix A, section A.2, from equation (A.10) to (A.17), for better readability of this chapter. The equations presented are valid for the condition that $i_L(0) < 0$ and $i_L(t_1) > 0$. New equations must be derived for the other

operating conditions, i.e., $i_L(0) < 0$ and $i_L(t_1) < 0$ or $i_L(0) > 0$ and $i_L(t_1) > 0$, also contemplated in Appendix A, section A.2

Considering the power switch as a single component, i.e., a bidirectional switch, the full RMS value of the current can be easily calculated, due to the fact that the current flowing through the switch is the same as the inductor current during half of T_S (Krismer, 2010). Equation (3.54) can be used to calculate the RMS value of the current in a power switch in the primary bridge, meanwhile equation (3.55) can be used for a power switch in the secondary bridge. $I_{L,rms}$ was defined in equation (3.16). However, estimating losses with these equations ignores the fact that the drain-source channel and the intrinsic body diode in the power switch (in the MOSFET case) have different resistances.

$$I_{QP,rms} = \frac{I_{L,rms}}{\sqrt{2}} \tag{3.54}$$

$$I_{QS,rms} = \frac{nI_{L,rms}}{\sqrt{2}} \tag{3.55}$$

As for the voltage stress, the switches and diodes in the primary bridge must be able to withstand V_i. In the same manner, the switches and diodes in the secondary bridge must be able to withstand V_o. If non-idealities such as parasitic inductances from the pins of the power switch are added to the circuit, oscillations in the voltage during the turn-off of the switch may occurs, resulting in overvoltage spikes (Krismer, 2010).

3.3.7 Passive Components Computation

The passive components of the DAB converter as can be seen in Figure 1 consist of:

- inductor L (which can be the leakage inductance of the transformer or not);
- the transformer T;
- the input capacitor C_i;
- the output capacitor C_o.

DAB inductance

The inductance L can be calculated by isolating the term in expression (3.10), which results in equation (3.56). It is suggested for the design that P_R is the rated power desired for the converter and ϕ_R the maximum phase-shift value.

$$L = \frac{nV_iV_o}{2P_Rf_s}\frac{|\phi_R|}{\pi}\left(1 - \frac{|\phi_R|}{\pi}\right) \tag{3.56}$$

If L is considered as a discrete inductor, the leakage inductance of the transformer will have to be considered into equation (3.56) to calculate the effective DAB inductance, since it will impact on the power transfer capability and other aspects of the converter. It must be designed to withstand the maximum inductor current, which will be either I_1 or I_2 (depending on which mode the converter is operating), derived in section 3.3.1, and the current $I_{L,rms}$, derived in section 3.3.2. The magnetic core design of the discrete inductor is not covered in this thesis.

Transformer

The transformer turns ratio n should be initially selected according to the voltage conversion ratio K. As seen earlier, when $K = 1$, the converter operates with lower $I_{L,rms}$ (and also lower switching losses due to soft-switching, which is seen later in this chapter).

If V_i and/or V_o varies during the converter operation, an iterative process or optimization design method should be applied in order to estimate the value of n that results in the highest efficiency across the voltage/power range of the converter.

In case the majority of the inductance L belongs to one side of the transformer, e.g., primary side, only the voltage $v_{cd}(t)$ is responsible for generating the flux density in the transformer.

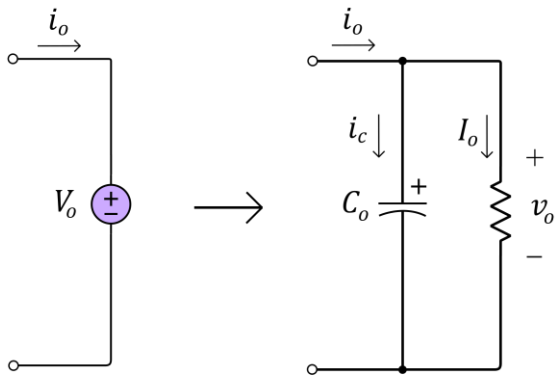
The transformer magnetic core design is not covered in this thesis.

Capacitors

The capacitors C_i and C_o are designed according to the input source and the load, respectively. The input capacitor C_i design will not be covered, assuming it to be part of the input voltage source.

For a purely resistive load, the expression for C_o can be found by using equation (3.57), where $i_c(t)$ is the capacitor current. The voltage across C_o is equal to the output voltage $v_o(t)$. The equivalent circuit is shown in Figure 29. The current in the capacitor is the alternating portion of the current $i_o(t)$ shown in Figure 30, which is defined by equation (3.58). Time instants t_1, t_2, t_3 and t_4 are defined in Table 3. Equation (3.58) is valid for buck mode. Equations (3.59) through (3.61) are valid for $i_L(0) < 0$ and $i_L(t_1) > 0$.

Figure 29 – Equivalent output circuit stage for a resistive load.



Source: provided by the author, 2024.

$$v_c(t) = \frac{1}{C}\int_0^t i_c(t)dt \tag{3.57}$$

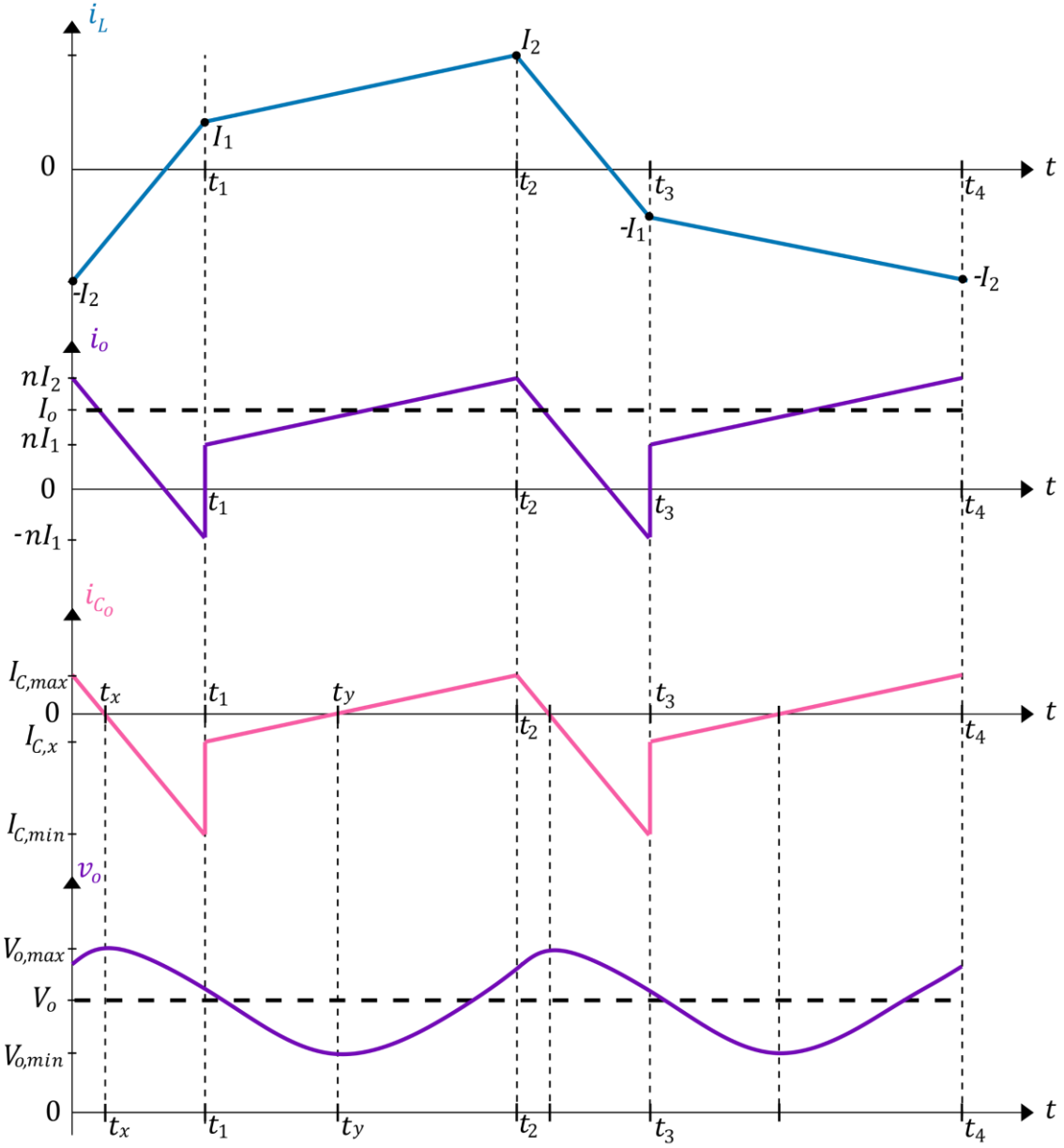
$$i_{C_o}(t) = i_o(t) - I_o = \begin{cases} -\dfrac{n(V_i + V_o')}{L}t + I_{c,max} \ \forall \ 0 < t \leq t_1 \\ \dfrac{n(V_i - V_o')}{L}(t - t_1) + I_{c,x} \ \forall \ t_1 < t \leq t_2 \end{cases} \tag{3.58}$$

$$I_{C,max} = \frac{n}{4Lf_s}\left[2V_i\left(\frac{|\phi|}{\pi}\right)^2 + (2V_o' - 2V_i)\frac{|\phi|}{\pi} + (V_i - V_o')\right] \tag{3.59}$$

$$I_{C,x} = \frac{n}{4Lf_s}\left[2V_i\left(\frac{|\phi|}{\pi}\right)^2 + (-V_i + V_o')\right] \tag{3.60}$$

$$I_{C,min} = \frac{n}{4Lf_s}\left[2V_i\left(\frac{|\phi|}{\pi}\right)^2 + -4V_i\frac{|\phi|}{\pi} + (V_i - V_o')\right] \quad (3.61)$$

Figure 30 – Capacitor C_o current and voltage waveforms for buck mode, $i_L(0) < 0$, $i_L(t_1) > 0$ and $\phi > 0$.



Source: provided by the author, 2024.

By looking at Figure 30, the output ripple voltage ΔV_o is defined by equation (3.62). The integral limits in equation (3.62), t_x and t_y are defined in equations (3.63) and (3.64), respectively.

$$V_{o,max} - V_{o,min} = \Delta V_o = \frac{1}{C_o}\int_{t_x}^{t_y} i_{C_o}(t)dt \tag{3.62}$$

$$t_x = \frac{L}{n(V_i + V_o')} I_{C,max} \tag{3.63}$$

$$t_y = \frac{L}{n(V_i - V_o')}\left(-I_{C,x}\right) + t_1 \quad \forall \quad I_{C,x} < 0 \tag{3.64}$$

Since there is a discontinuity in the interval $[t_x, t_y]$, the integral in equation (3.62) is divided into two, as can be seen in equation (3.65). Solving these integrals and rearranging the terms, an expression for C_o can be found. The derived expression for the computation of C_o as function of the desired ΔV_o can be seen in Appendix A, section A.3, as equation (A.34)

$$\begin{aligned}\Delta V_o = \frac{1}{C_o}\Bigg(&\int_{t_x}^{t_1}\left(-\frac{n(V_i + V_o')}{L}t + I_{C,max}\right)dt \\ &+ \int_{t_1}^{t_y}\left(\frac{n(V_i - V_o')}{L}(t - t_1) + I_{C,x}\right)dt\Bigg)\end{aligned} \tag{3.65}$$

Since the converter was analyzed considering a DC voltage source as the load (i.e., a very big capacitance), a big voltage ripple will cause a difference in the average value of the output voltage for the phase-shift ϕ calculated by equation (3.13).

In this case, small adjustments need to be made in ϕ, which will be automatically compensated if the converter operates with any controller having an integral action term, such as a PI or PID controller. To obtain a closer value to the mathematical model, a voltage ripple $\Delta V_o \leq 0{,}05 V_o$ should be chosen, although a bigger capacitance C_o will be needed.

Another cause for the increase of larger ΔV_o than desired is the circulating power, described in section 3.3.4. In SPS modulation, the only way to eliminate the circulating power is meeting the condition $V_i = V_o'\left(1 - 2\frac{|\phi|}{\pi}\right)$. To reduce the circulating power, another modulation strategy should be used, such as DPS modulation.

The RMS value of the current flowing through C_o can be calculated using the equation (3.66). The expression derived from equation (3.66) can be seen in Appendix A, section A.3, as equation (A.36).

The equations shown earlier (except for (A.36)) are valid for the conditions of $V_i > nV_o$, $i_L(0) < 0$ and $i_L(t_1) > 0$.

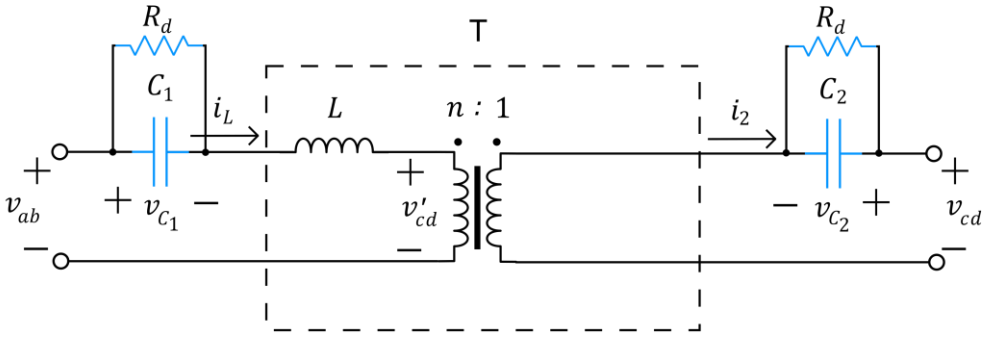
$$
\begin{aligned}
I_{C_o,rms} &= \sqrt{\frac{2}{T_s}\int_0^{t_2} i_{C_o}^2(t)dt} \\
&= \left\{\frac{2}{T_s}\left[\int_0^{t_1}\left(-\frac{n(V_i+V_o')}{L}t + I_{C,max}\right)^2 dt\right.\right. \\
&\left.\left. + \int_0^{t_2-t_1}\left(\frac{n(V_i-V_o')}{L}t + I_{C,x}\right)^2 dt\right]\right\}^{1/2}
\end{aligned}
\tag{3.66}
$$

DC Blocking Capacitors

For practical implementation, in case there is no control scheme to avoid/mitigate transformer saturation, it is recommended the use of DC blocking capacitors in series with both primary and secondary sides of the transformer. Figure 31 shows the circuit diagram. Damping resistor R_d can be calculated with equation (4.13)

To calculate the required capacitance, the resonant frequency f_{LC} of the capacitors with the inductor can be used, shown in equation (3.67) (Schibli, 2000).

Figure 31 – Diagram of transformer with series DC blocking capacitors.



Source: provided by the author, 2024.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \ll f_s \tag{3.67}$$

The chosen frequency f_{LC} must be much smaller than the switching frequency f_s (at least 5 times smaller). Rearranging equation (3.67) results in equation (3.68).

$$C = \frac{1}{4\pi^2 f_{LC}^2 L} \tag{3.68}$$

Equation (3.68) shows the total capacitance needed to block the DC components in the transformer. The capacitance needed in each side of the transformer is given in equation (3.69).

$$C_1 = C_2 = 2C \tag{3.69}$$

The maximum voltage across the capacitor must also be known. Figure 32 shows the waveforms of the inductor current and the capacitor voltage C_1 considering $\phi = \pi/2$. The time instants values can be seen in Table 3 (except for t_a and t_b). The voltage ripple in C_1 can be defined using equation (3.70)

$$V_{max} - V_{min} = \Delta V_c = \frac{1}{C_1}\int_{t_a}^{t_b} i_{C_1}(t)\,dt = \frac{1}{C_1}\int_{t_a}^{t_b} i_L(t)\,dt \tag{3.70}$$

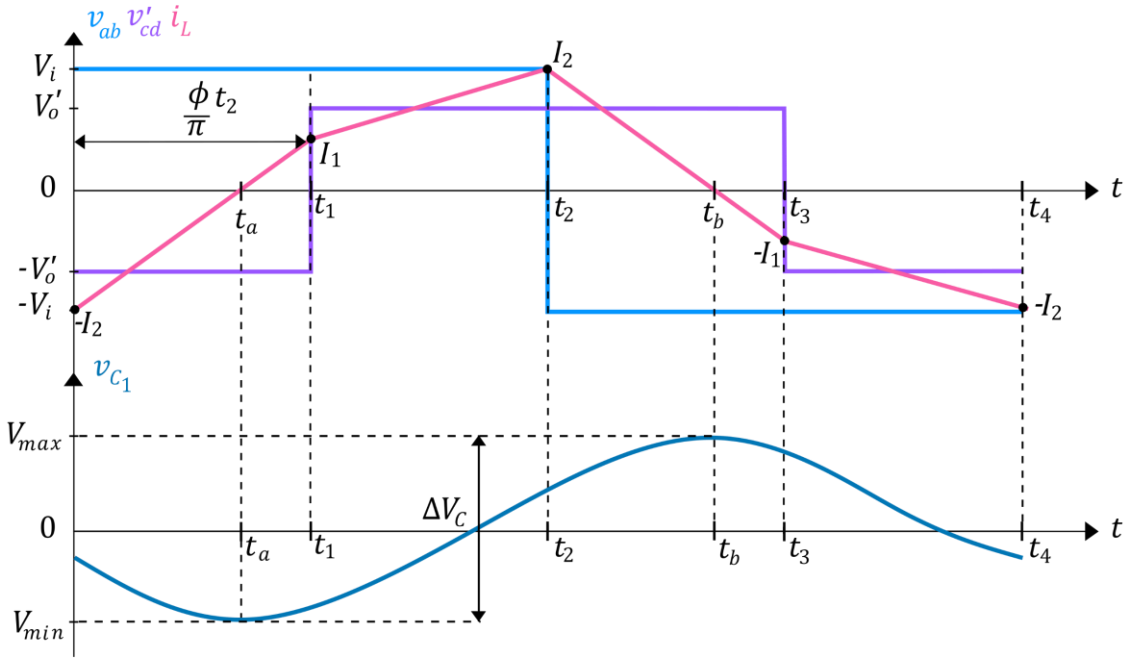
According to the voltage waveform in Figure 32 and using the appropriate intervals of equation (3.5), equation (3.70) becomes equation (3.71).

$$\begin{aligned}\Delta V_c = \frac{1}{C_1}\Bigg[&\int_{t_a}^{t_1}\left(\frac{(V_i + V_o')}{L}t - I_2\right)dt + \int_{t_1}^{t_2}\left(\frac{(V_i - V_o')}{L}(t - t_1) - I_1\right)dt \\ &+ \int_{t_2}^{t_b}\left(\frac{-(V_i + V_o')}{L}(t - t_2) + I_2\right)dt\Bigg] \\ &\forall\, i_L(0) < 0 \;\wedge\; i_L(t_1) > 0\end{aligned} \tag{3.71}$$

$$t_a = I_2 \frac{L}{(V_i + V_o')} \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.72}$$

$$t_b = t_a + t_2 \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.73}$$

Figure 32 – Voltage and current waveforms in DC blocking series capacitor C_1.



Source: provided by the author, 2024.

By solving the integral of equation (3.71), the expression for ΔV_c can be derived, resulting in equation (3.74).

$$\Delta V_c = \frac{1}{C_1} \frac{1}{32 L f_s^2} \frac{1}{(V_i + V_o')} \left[-8 V_i V_o' \left(\frac{|\phi|}{\pi} \right)^2 + 16 V_i V_o' \frac{|\phi|}{\pi} + 2(V_i - V_o')^2 \right] \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.74}$$

Therefore, the maximum voltage across the DC blocking capacitor C_1 is

$$V_{max,C_1} = \frac{\Delta V_c}{2} \quad \forall \; i_L(0) < 0 \; \wedge \; i_L(t_1) > 0 \tag{3.75}$$

Since $C_1 = C_2$ and $i_2(t) = n i_L(t)$, the voltage V_{max} for the capacitor C_2 can be found by using equation (3.76).

$$V_{max,C_2} = \frac{n\Delta V_c}{2} \;\; \forall \;\; i_L(0) < 0 \;\wedge\; i_L(t_1) > 0 \tag{3.76}$$

The equation valid for other cases ($i_L(0) < 0$ and $i_L(t_1) < 0$ or $i_L(0) > 0$ and $i_L(t_1) > 0$) can be derived by using equation (3.70) with the appropriate alterations in the inductor current waveform and the integral limits t_a and t_b.

3.3.8 Dead-time Effect

Despite being necessary to avoid the occurrence of short-circuit in a phase-leg, the dead-time negatively affects the performance of all power converters. In DAB converters, the dead-time can lead to a change of the effective phase-shift, and therefore, the power transferred is altered.

During this period, both power switches in a phase-leg are commanded to turn-off. Since the current can't flow through the power switch anymore, it flows through the antiparallel diodes. When this happens, there is no control over the output voltage of a bridge, meaning that it only depends on which direction the current is flowing. According to Segaran (2013), there are three possible scenarios:

- If $i_L(t)$ is negative during the start of dead-time, it does not impact on the output voltage of the bridge, and the phase-shift does not change;
- If $i_L(t)$ is positive during the start of dead-time, but becomes negative at some point before the dead-time ends, the polarity of the output voltage of the bridge alternates while still in dead-time period, but a partial phase-shift error occurs;
- If $i_L(t)$ is positive during the start of dead-time and does not cross zero until the end of the dead-time period, the polarity of the output voltage of the bridge only alternates at the end, meaning a full phase-shift error is caused by the dead-time.

This phase-shift error can be compensated by adding a phase-shift angle ϕ_{dt} to the ideal phase-shift angle ϕ value, according to the current operating conditions of the converter. The adjusted phase-shift ϕ_a is shown in equation (3.77).

$$\phi_a = \phi + \phi_{dt} \tag{3.77}$$

The analysis of the error depends not only on the inductor current's amplitude and polarity, but also the voltages V_i, V_o and which bridge is the leading bridge. A more complete analysis is done by Segaran (2013), which also provides the equations to calculate ϕ_{dt} for compensating the phase-shift error caused by the dead-time.

According to Bai and Mi (2008), the full dead-time period T_{dt} can be converted to a phase-shift angle ϕ_{db}, which is given by equation (3.78).

$$\phi_{db} = T_{dt} \cdot 2\pi \cdot f_s \tag{3.78}$$

As a final note, the dead-time period cannot be bigger than the period t_1 (time resulted from the phase-shift operation). Otherwise, the converter won't operate properly.

3.3.9 Soft-switching Operation

Soft-switching is a technique used for reducing switching losses. The two main types are: passive or active. The passive type utilizes components such as inductors and capacitors, which can be added or already be a part of the converter, whereas the active type are additional circuits with switches.

The technique consists of ensuring the voltage across the switch or the current through the channel is zero before the switch receives a signal command (turn-on or turn-off). Thus, they are classified as Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS).

The DAB converter has natural passive-type ZVS because of the inductor in series with the transformer and antiparallel diodes with the switches, which are already part of its topology, as seen in Figure 1.

To explain the requirements for ZVS, first it is considered an ideal power switch that has no output capacitance. The current must be flowing through the antiparallel diode before the turn-on command is given, ensuring the voltage over the switch is clamped to zero before turn-on. This operating condition was used in the study case illustrated in sections 3.1 and 3.2. In Figure 28, it can be seen that the switches in both bridges achieve ZVS during turn-on, because the antiparallel diodes are conducting current when a switching event happens. However, it should be noted that during turn-off, the current flowing through the switches is not zero, resulting in a hard switch. Therefore, despite no switching loss occurs during turn-on, there is still some energy dissipated during turn-off.

Analyzing the converter in Figure 1 and the inductor current waveforms for $\phi > 0$, it can be concluded that there are two conditions for enabling ZVS operation:

a) For the primary bridge: $i_L(0) < 0$;
b) For the secondary bridge: $i_L(t_1) > 0$.

Since $|i_L(0)| = |I_2|$, by analyzing equation (3.7), the condition for ZVS in the primary bridge can be found, leading to expressions (3.81).

$$I_2 = \frac{V_i}{4Lf_s}\left(2K\frac{|\phi|}{\pi} + 1 - K\right) \tag{3.79}$$

$$\bar{I_2} = \frac{4Lf_s}{V_i} I_2 = 2K\frac{|\phi|}{\pi} + 1 - K \tag{3.80}$$

$$\bar{I_2} \geq 0 \rightarrow \ 2K\frac{|\phi|}{\pi} + 1 - K \geq 0 \tag{3.81}$$

For the secondary bridge, since $|i_L(t_1)| = |I_1|$, analyzing equation (3.8) can lead to the expression (3.84).

$$I_1 = \frac{V_i}{4Lf_s}\left(2\frac{|\phi|}{\pi} - 1 + K\right) \tag{3.82}$$

$$\overline{I_1} = \frac{4Lf_s}{V_i} I_1 = 2\frac{|\phi|}{\pi} - 1 + K \tag{3.83}$$

$$\overline{I_1} \geq 0 \rightarrow 2\frac{|\phi|}{\pi} - 1 + K \geq 0 \tag{3.84}$$

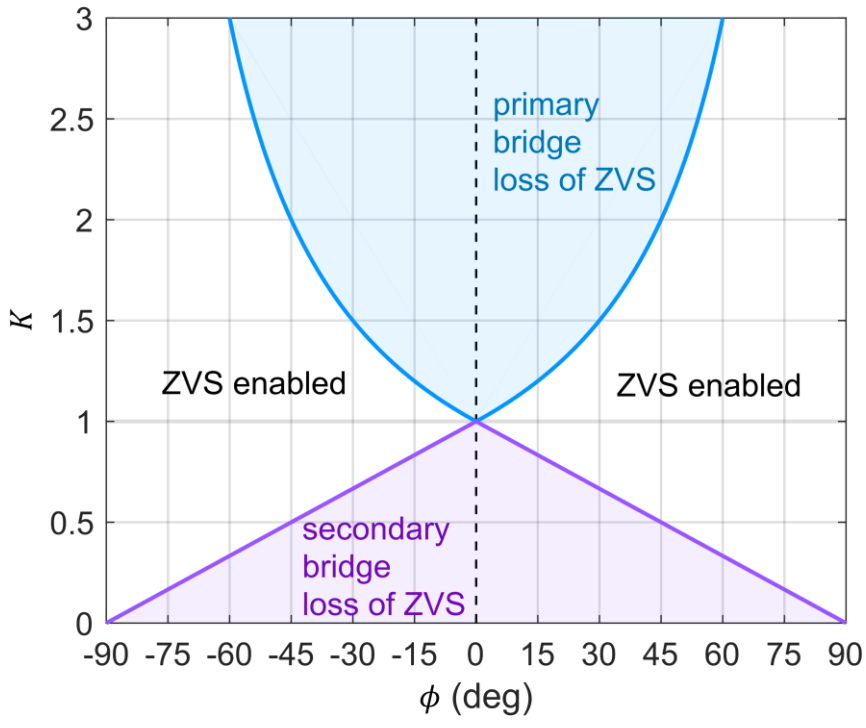
From expressions (3.81) and (3.84), the boundary values of the voltage conversion ratio K as function of ϕ can be derived as equations (3.85) and (3.86), respectively.

$$2K_{PB}\frac{|\phi|}{\pi} + 1 - K_{PB} = 0 \;\rightarrow\; K_{PB} = \frac{1}{1 - 2\frac{|\phi|}{\pi}} \tag{3.85}$$

$$2\frac{|\phi|}{\pi} - 1 + K_{SB} = 0 \;\rightarrow\; K_{SB} = 1 - 2\frac{|\phi|}{\pi} \tag{3.86}$$

Plotted in Figure 33, equations (3.85) and (3.86) define the ZVS regions.

Figure 33 – Plot of K versus ϕ with ZVS regions considering ideal switches.



Source: provided by the author, 2024.

Because of the symmetric characteristic of the converter, the curves for the negative phase-shift interval are just the mirrored versions of equations (3.85) and (3.86). It can be noted that for $K = 1$, soft-switching happens in both bridges for all the range of ϕ.

On the other hand, when $K \neq 1$, as ϕ decreases one of the bridges will lose ZVS operation, meaning one of the conditions a) or b) will not be respected anymore. If $K > 1$ when ϕ decreases, current $i_L(0)$ will become positive at a certain ϕ value, disabling ZVS for the primary bridge. If $K < 1$ when ϕ decreases, current $i_L(t_1)$ will become negative at a certain ϕ value, disabling ZVS for the secondary bridge.

Another analysis can be done by looking at the normalized transmitted power of the converter. Substituting equations (3.85) and (3.86) into (3.88), boundary equations (3.89) and (3.90) can be derived, which are plotted in Figure 34 with the transmitted power for different values of K.

$$P_b = \frac{V_i^2}{8Lf_s} \tag{3.84}$$

$$\bar{P} = \frac{P}{P_b} = 4K\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.88}$$

$$\bar{P}_{PB} = 4\frac{1}{\left(1 - 2\frac{|\phi|}{\pi}\right)}\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.89}$$

$$\bar{P}_{SB} = 4\left(1 - 2\frac{|\phi|}{\pi}\right)\frac{\phi}{\pi}\left(1 - \frac{|\phi|}{\pi}\right) \tag{3.90}$$

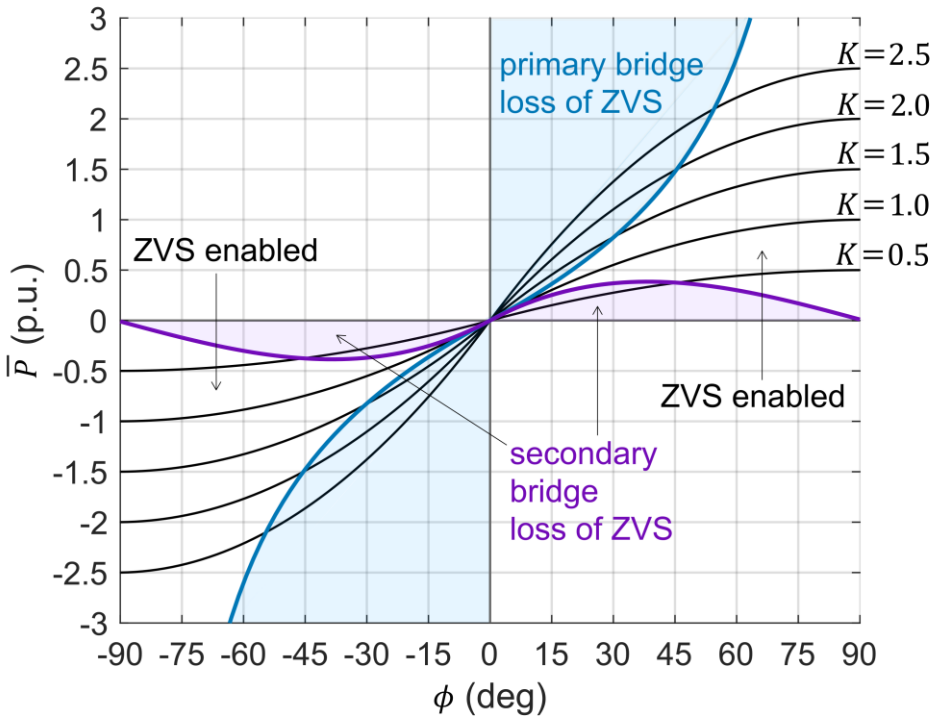
From the perspective of Figure 34, it can be concluded that as the load gets lighter (i.e., the power transmitted decreases) when $K \neq 1$, the switching currents (I_1 or I_2) will change polarity at certain point (seen in section 3.3.1) depending on the value of K, causing one of the bridges to lose ZVS. For $K = 1$, ZVS is achieved in both bridges for the whole power range, since I_1 and I_2 polarities never change.

Taking the analysis a step further, the influence of the power switches' output capacitance (or an external capacitance placed in parallel with the transistor) changes the constraints for enabling ZVS, because now the magnitude

of the inductor current at the switching instant needs to be large enough to charge/discharge the capacitors. The following analysis is also done for $\phi > 0$, but similar analysis can be done for $\phi < 0$.

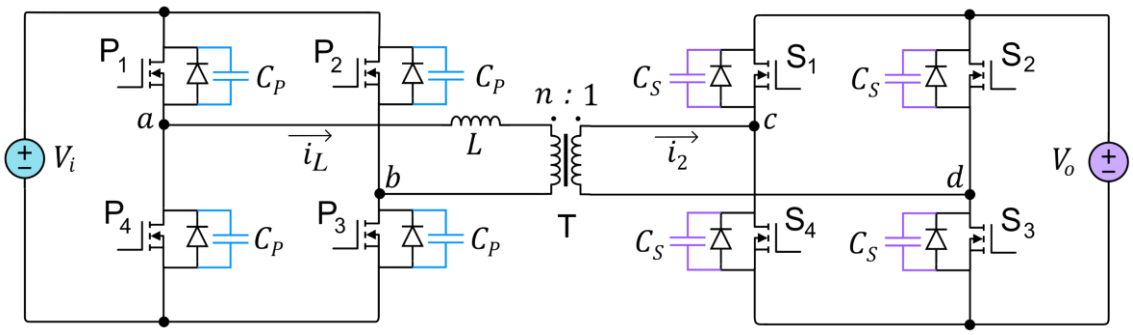
Figure 35 illustrates the switches with the output capacitance in the converter. For this analysis, it is considered that every switch in a bridge has the same output capacitance.

Figure 34 - Plot of P versus ϕ with ZVS regions considering ideal switches.



Source: provided by the author, 2024.

Figure 35 – DAB converter diagram with the switches' output capacitances.



Source: provided by the author, 2024.

The minimum value of current required for ZVS (I_{ZVS}) can be found by using the energy stored in the DAB inductor L and the effective output capacitance C, presented in expression (3.91), where V_Q is the voltage over the switch and m is the number of switches to be turned-on.

$$\frac{1}{2}L|i_L|^2 \geq m\frac{1}{2}CV_Q^2 \tag{3.91}$$

For the primary bridge, substituting $m = 2$, $C = C_P$ and $V_Q = V_i$ in (3.91), the minimum inductor current $I_{ZVS,P}$ required to enable ZVS can be calculated with equation (3.93).

$$\frac{1}{2}LI_{ZVS,P} = 2\frac{1}{2}C_PV_i^2 \tag{3.92}$$

$$I_{ZVS,P} = V_i\sqrt{\frac{2C_P}{L}} \tag{3.93}$$

For the secondary bridge, substituting $m = 2$, $C = C_S$ and $V_Q = V_o$ in (3.91), the minimum inductor current $I_{ZVS,S}$ required to enable ZVS can be calculated with equation (3.95).

$$\frac{1}{2}LI_{ZVS,S} = 2\frac{1}{2}C_SV_o^2 \tag{3.94}$$

$$I_{ZVS,S} = V_o\sqrt{\frac{2C_S}{L}} \tag{3.95}$$

The regions of ZVS operation considering the output capacitance for the primary bridge can be found by substituting $|i_L| = I_2$, $m = 2$, $C = C_P$ and $V_Q = V_i$ in (3.91), resulting in expression (3.97).

$$\frac{1}{2}LI_2^2 \geq 2\frac{1}{2}C_PV_i^2 \tag{3.96}$$

$$K_{PB} \leq \frac{1 - 4f_s\sqrt{2LC_P}}{1 - 2\frac{|\phi|}{\pi}} \tag{3.97}$$

For the secondary bridge, considering the inductor L referred to the secondary of the transformer, by substituting $|i_L| = nI_1$, $m = 2$, $C = C_S$ and $V_Q = V_o$ in (3.91), expression (3.99) can be found.

$$\frac{1}{2}\frac{L}{n^2}(nI_1)^2 \geq 2\frac{1}{2}C_S V_o^2 \tag{3.98}$$

$$K_{SB} \geq \frac{1 - 2\frac{|\phi|}{\pi}}{1 - \frac{4f_s\sqrt{2LC_S}}{n}} \tag{3.99}$$

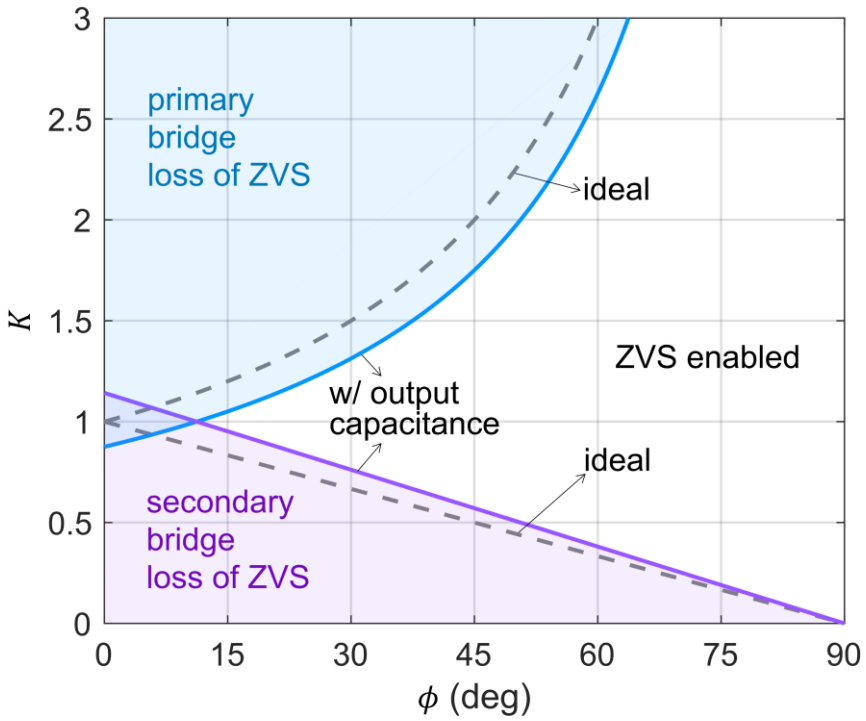
Figure 36 plots K_{PB} and K_{SB} considering the cases with ideal power switch and with output capacitance, as function of $\phi \in [0, \pi/2]$. It is assumed that for each value of ϕ, the dead-time period is long enough for the capacitances fully charge/discharge and for the converter to operate properly.

It can be noted in Figure 36 that as the output capacitance increases, the region allowing ZVS operation gets narrower. Consequently, even when $K = 1$, the converter will not be able to operate with soft-switching when operating with a smaller ϕ (i.e., under light load). Which is expected, since as the output capacitance increases, the minimum value of current required to charge/discharge the capacitors also increase, as can be noted by analyzing equations (3.93) and (3.95). In other words, when the converter operates at a lower power, it does not have enough energy stored in the inductor to charge/discharge the capacitors before the turn-on of the switches.

For the appropriate operation of the soft-switching, the charge and discharge of the switches' output capacitances has to happen during the dead-time period of the switching commands. Therefore, the minimum dead-time period must be known.

Equation (3.100) can be used to calculate the minimum dead-time period for the switches in the primary bridge, where Q_{C_P} is the charge stored in the capacitance C_P, while equation (3.101) can be used for the switches in the

Figure 36 - Plot of K versus ϕ with ZVS regions considering the switches' output capacitance. Parameters: $L = 13.88\,\mu H$, $n = 1$, $f_s = 10\,kHz$ and $C_P = C_S = 350\,nF$.



Source: provided by the author, 2024.

secondary bridge, where Q_{C_S} is the charge stored in the capacitance C_S. Basically, equations (3.100) and (3.101) calculate the period in which the capacitors charge/discharge, considering the minimum value of the inductor current necessary for ZVS. The higher the inductor current at the switching moment, the faster the capacitors are charged/discharged, thus requiring a shorter dead-time period.

$$t_{ZVS,P} = \frac{mQ_{C_P}}{I_{ZVS,P}} = \frac{2C_P V_i}{I_{ZVS,P}} \tag{3.100}$$

$$t_{ZVS,S} = \frac{mQ_{C_S}}{I_{ZVS,S}} = \frac{2C_S V_o}{I_{ZVS,S}} \tag{3.101}$$

Obviously, the same dead-time period has to be applied to both the primary and secondary bridges. Thus, the minimum dead-time period to be

applied must be the larger period calculated between equations (3.100) and (3.101).

To conclude, the capacitances C_p and C_s must be small enough not only for higher efficiency, but also to allow proper operation of the converter. The equations derived in this chapter does not take into account the resonance between the output capacitances and the inductance L. If the output capacitances and the dead-time are big enough, the resonance between the components can distort the shape of the voltages v_{ab} and/or v_{cd}, as well as the current i_L. In this case, the equations presented in this chapter are not valid anymore.

3.3.10 Final Remarks

The addition of non-ideal characteristics in the components, such as: on-resistances, parasitic capacitances, parasitic lead inductances, resistance of inductor/transformer windings, inductance and resistance of PCB traces and temperature, changes the equivalent circuit model of the DAB, resulting in different voltage and current waveforms than the ones presented in this chapter. Obviously, new equations should be derived for accounting these parameters.

For a DAB converter operating with $K \approx 1$, the conduction losses of the components are dominant through most of the power range, thus the provided equations in this chapter might be enough to estimate the efficiency of the converter. For $K \neq 1$, the converter will lose ZVS in one of the bridges much earlier, meaning the switching losses will be significant. Thus, other methods for calculating this loss with accuracy should be used (Krismer, 2010).

For DAB converters that operates in buck or boost mode, the efficiency of the converter can change depending on the direction of power flow (Krismer, 2010).

The equations presented in this chapter are suitable for studying the converter and an initial design, but a more accurate model should be used in a product design. The purpose of this chapter is simply to introduce the reader to the fundamental operation of the DAB converter. Incorporating non-ideal components to the model results in complex equations, and it is out of the scope

of this Master's thesis. A comprehensive analysis of the accurate loss model for the DAB can be seen in (Krismer, 2010).

In summary, although SPS modulation is the simplest modulation for DAB converters and has disadvantages when operating under light load or $K \neq 1$, understanding its fundamental concepts is important and helps to understand the development of more complex modulations. Moreover, when the converter operates with heavy load or K close to unity, SPS modulation might achieve higher efficiency, compared to the other traditional modulations (Bai; Nie; Mi, 2010).

4 PROTOTYPE DESIGN

In this chapter, the methodology for designing a DAB converter prototype is presented, which includes: requirements, passive components computation and efficiency estimates.

4.1 REQUIREMENTS

Before designing the DAB prototype, initial requirements must be established. The active bridges for the converter already existed for another project and was designed and built by Castellain (2024). They are being reused for building the DAB prototype to save time. Despite that, the design methodology of the converter is shown in the next section for didactic purposes. The requirements chosen for the DAB prototype considers the hardware limits from the active bridges.

One of the proposed applications for the DAB converter are DC grids. Sometimes, the interconnection between two different DC grids with the same voltage is needed. An isolated and bidirectional DC-DC power converter is necessary for interfacing them. Since both grids have the same voltage, the transformer's turns ratio can be equal to 1.

Power transmission in DC grids is usually done in the order of kVs. However, due to laboratory and available equipment constraints, experiments must be done at a lower voltage. One of the proposed voltage bus levels for a DC microgrid is 380 V (Jithin et al., 2023; Dragicevic et al., 2016).

The rated power, switching frequency and rated phase-shift (for SPS modulation) values are chosen based on three constraints:

1. Available magnetic core for the transformer operating with a temperature of 80 °C at rated power (for lower losses);
2. Safe margin between phase-shift period and dead time necessary for the power switches, ensuring normal operation of the converter;
3. Big enough ZVS region for dismissing switching loss through most of the power range of the converter.

Many design iterations were done to define the values for these parameters, in order to build a transformer with the highest rated power possible. Table 4 sums up the parameters of the converter prototype.

Table 4 – Converter parameters for the DAB prototype.

Parameter	Value
Rated Power (P_R)	600 W
Input Voltage (V_i)	380 V
Output Voltage (V_o)	380 V
Transformer Turns Ratio (n)	1
Switching Frequency (f_s)	20 kHz
Rated Phase-Shift (ϕ_R)	18°

Source: provided by the author, 2025.

The design of the active bridges is the same for both the primary and secondary bridges. The converter circuit contains the power switches, gate driver circuits, sensors and an auxiliary power supply. Although they can be considered over-engineered regarding the requirements of the DAB converter, the boards are more than adequate for prototyping purposes. Table 5 shows the main specifications of the board's power stage and Figure 37 shows a picture of one board.

Table 5 – Specifications of Primary and Secondary Bridges for the prototype.

Component	Value
Power Switches	IGBT APT15GT60BRDQ1
DC-Link Capacitor	942 μF - 400 V
Voltage Sensor (Secondary Bridge only)	LEM LV 20-P

Source: provided by the author, 2025.

Figure 37 – Picture of the Active Bridge board used for the prototype.

Source: provided by Castellain (2024).

Table 6 shows the main specifications of the power switches. The IGBT used already has a built-in antiparallel diode. The dead time chosen for the power switches is 300 ns. Nonetheless, it is important to add that the optocoupler (HCPL3120) utilized in the gate driver circuits also adds a signal delay, therefore, the measured dead time of the power switches will bigger.

Table 6 – Main parameters of the IGBT APT15GT60BRDQ1.

Parameter	Value
Max Continuous Collector Current	20 A (@ Case Temperature = 110 °C)
Blocking Voltage	600 V
Output Capacitance	84 pF
Turn-on Delay Time	6 ns
Current Rise Time	8 ns
Turn-off Delay Time	125 ns
Current Fall Time	100 ns

Source: (Microchip, 2008).

4.2 DESIGN METHODOLOGY

The converter is designed considering full power, i.e., when $\phi = \phi_R$. The voltage conversion ratio of the converter is given by equation (4.1).

$$K = \frac{V_o'}{V_i} = \frac{nV_o}{V_i} = \frac{1 \cdot 380}{380} = 1 \tag{4.1}$$

The first component to be computed is the required leakage inductance from the transformer. By using equation (3.56) and given the parameters from Table 4, the inductance L can be computed as shows equation (4.2).

$$\begin{aligned} L &= \frac{nV_iV_o}{2P_Rf_s}\frac{|\phi_R|}{\pi}\left(1-\frac{|\phi_R|}{\pi}\right) \\ &= \frac{1 \cdot 380 \cdot 380}{2 \cdot 600 \cdot 20 \times 10^3}\frac{\left|\frac{18}{180}\right|}{\pi}\left(1-\frac{\left|\frac{18}{180}\right|}{\pi}\right) \\ &= 541.5\ \mu H \end{aligned} \tag{4.2}$$

Using equation (3.16), the RMS value of the transformer current at rated power can be calculated with equation (4.3).

$$\begin{aligned} I_{L,rms} &= \frac{1}{2Lf_s}\sqrt{-\frac{2}{3}V_iV_o'\left(\frac{|\phi_R|}{\pi}\right)^3 + V_iV_o'\left(\frac{|\phi_R|}{\pi}\right)^2 + \left(\frac{V_i^2}{12}-\frac{V_iV_o'}{6}+\frac{{V_o'}^2}{12}\right)} \\ &= \frac{1}{2 \cdot 541.5 \times 10^{-6} \cdot 20 \times 10^3}\left(-\frac{2}{3}380^2\left(\frac{|18/180|}{\pi}\right)^3\right. \\ &\qquad \left. + 380^2\left(\frac{|18/180|}{\pi}\right)^2 + \left(\frac{380^2}{12}-\frac{380^2}{6}+\frac{380^2}{12}\right)\right)^{1/2} \\ &= 1.69\ A \end{aligned} \tag{4.3}$$

Since $K = 1$, the converter operates in Voltage Match mode. Therefore, the switching currents I_1 and I_2 are the same and hence, they are the peak value of the transformer current. Using equation (3.7), they can be calculated as shows expression (4.4).

$$I_1 = I_2 = \frac{1}{4Lf_s}\left(2V_i\frac{|\phi_R|}{\pi} - V_i + V_o'\right)$$
$$= \frac{1}{4 \cdot 541.5 \times 10^{-6} \cdot 20 \times 10^3}\left(2 \cdot 380\frac{\left|\frac{18}{180}\right|}{\pi} - 380 + 380\right) \quad (4.4)$$
$$= 1.75\ A$$

The input current can be calculated with equation (3.23), as shown in equation (4.5).

$$I_i = \frac{nV_o}{2Lf_s}\frac{\phi_R}{\pi}\left(1 - \frac{|\phi_R|}{\pi}\right)$$
$$= \frac{1 \cdot 380}{2 \cdot 541.5 \times 10^{-6} \cdot 20 \times 10^3}\frac{\frac{18}{180}}{\pi}\left(1 - \frac{\left|\frac{18}{180}\right|}{\pi}\right) \quad (4.5)$$
$$= 1.58\ A$$

The output current can be calculated with equation (3.27), as shown in equation (4.6).

$$I_o = \frac{nV_i}{2Lf_s}\frac{\phi_R}{\pi}\left(1 - \frac{|\phi_R|}{\pi}\right)$$
$$= \frac{1 \cdot 380}{2 \cdot 541.5 \times 10^{-6} \cdot 20 \times 10^3}\frac{\frac{18}{180}}{\pi}\left(1 - \frac{\left|\frac{18}{180}\right|}{\pi}\right) \quad (4.6)$$
$$= 1.58\ A$$

4.2.1 Transformer

A ferrite magnetic core made by Thornton is used for building the transformer. Its main geometric properties can be seen in Table 7.

Table 7 – Thornton ferrite core used for transformer.

Property	Value
Core Type	E
Model	NEE-55/28/21
Core Area	354 mm²
Window Area	250 mm²
Volume	42.5 cm³

Source: (Thornton, 2025).

The transformer was designed using the Areas Product Method. The methodology followed can be seen in (Oliveira, 2001) and will not be replicated here. Based on the converter parameters from Table 4, the transformer is built resulting in the parameters from Table 8. The ambient temperature considered is 40 °C.

Table 8 – Transformer construction parameters.

Parameter	Value
Round Wire Gauge	20 AWG
Primary Number of Turns N_P	99
Secondary Number of Turns N_S	99
Core Temperature at Rated Power	81.5 °C

Source: provided by the author, 2025.

Measurements of the transformer with the LCR Meter MS5308 from Politerm can be seen in Table 9.

Table 9 – Measurements from built transformer with LCR Meter (at 10 kHz frequency).

Parameter	Value
Primary L_m	25.87 mH
Secondary L_m	25.91 mH
Primary Leakage Inductance (l_1)	38.16 μH
Secondary Leakage Inductance (l_2)	38.18 μH
Primary Winding Resistance	0.5 Ω
Secondary Winding Resistance	0.5 Ω

Source: provided by the author, 2025.

4.2.2 Additional Inductor

As can be seen in Table 9, the total leakage inductance of the built transformer is not enough for the calculated value of 541.5 μH, as shown in equation (4.2). Therefore, an additional inductor L_{dab} is built to achieve the required value. The necessary inductance is given by equation (4.7).

$$\begin{aligned} L_{dab} &= L - l_1 - \left(\frac{N_P}{N_S}\right)^2 l_2 \\ &= 541.5 \times 10^{-6} - 38.16 \times 10^{-6} - \left(\frac{99}{99}\right)^2 (38.18 \times 10^{-6}) \\ &= 465.16\ \mu H \end{aligned} \tag{4.7}$$

The design method for the inductor can also be seen in (Oliveira, 2001). The inductor was built with a NEE-30/15/07 core, also from Thornton. Table 10 sums up the main specifications of the inductor built (Thornton, 2025). Measurements were made with the same LCR Meter at 10 kHz. The ambient

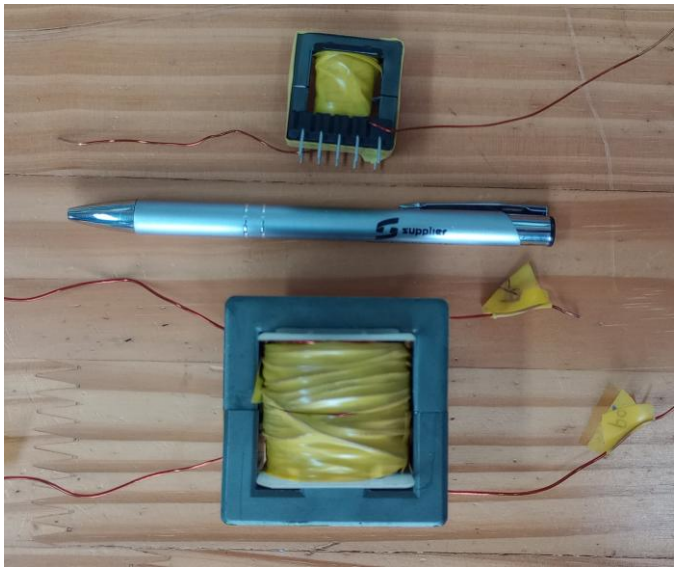
temperature considered is 40 °C. Figure 38 shows a picture of both the transformer and inductor built.

Table 10 – Additional inductor specifications.

Property	Value
Core Type	E
Model	NEE-30/15/07
Core Area	60 mm²
Window Area	80 mm²
Volume	4 cm³
Round Wire Gauge	23 AWG
Number of Turns	60
Total Air Gap Calculated	0.0051 mm
Temperature @ P_r	80.4 °C
Measured Inductance	463 μH
Measured Resistance	232 mΩ

Source: provided by the author, 2025.

Figure 38 – Picture of the inductor (above pen) and transformer (below pen) built for the prototype.



Source: provided by the author, 2025.

4.2.3 DC Blocking Capacitors

The resonant frequency between the capacitors and the total inductance is given by equation (4.8). It is chosen to suit the available capacitors and is close to $f_s/5$.

$$f_{LC} = \frac{f_s}{4.7} = \frac{20 \times 10^3}{4.7} = 4.25\ kHz \tag{4.8}$$

The total capacitance necessary is given by expression (4.9)

$$C_d = \frac{1}{4\pi^2 f_{LC}^2 L} = \frac{1}{4\pi^2 \cdot 4255^2 \cdot 541.5 \times 10^{-6}} = 2.58\ \mu F \tag{4.9}$$

Therefore, the necessary capacitance at each side of the transformer is given by equation (4.10).

$$C_1 = C_2 = 2 \cdot C_d = 5.17\ \mu F \tag{4.10}$$

By using a parallel combination of two 2.2 μF and one 0.68 μF capacitors, the equivalent capacitance at each side of the transformer becomes 5.08 μF. The capacitors are rated for 400 V, in order to withstand the full input/output voltage in case of failure.

Using equation (3.74), the total voltage oscillation of the capacitors can be calculated as shows expression (4.11). Thus, the maximum voltage over the capacitors is given by equation (4.12), which is valid for capacitors in both sides of the bridges, since $n = 1$.

$$\Delta V_c = 8.2\ V \tag{4.11}$$

$$V_{max} = \frac{\Delta V_c}{2} = 4.1\ V \tag{4.12}$$

A damping resistor is placed in parallel with the DC blocking capacitors.

Considering the full input voltage and a dissipated power of 0.1% of P_R, the value of the resistance is calculated with equation (4.13).

$$R_d = \frac{V_i^2}{0.001 P_R} = \frac{380^2}{0.001 \cdot 600} \approx 270\ k\Omega \tag{4.13}$$

4.2.4 Output Capacitor

Since the active boards already have built-in DC link capacitors (Table 5), the output voltage ripple and the RMS value of the capacitor current can be calculated with equations (A.35) and (A.36), respectively, considering a resistive load.

$$\Delta V_o = 5.36\ mV \tag{4.14}$$

$$I_{C,rms} = 616.1\ mA \tag{4.15}$$

4.2.5 Semiconductors Stresses

Using equations (A.10) through (A.17), the current stress in the semiconductors can be calculated. The results are shown in Table 11.

Table 11 – Semiconductors current stresses for the prototype.

Parameter	Value
I_P	0.81 A
$I_{P,rms}$	1.19 A
I_{DP}	0.02 A
$I_{DP,rms}$	0.16 A
I_S	0.02 A
$I_{S,rms}$	0.16 A
I_{DS}	0.81 A
$I_{DS,rms}$	1.19 A

Source: provided by the author, 2025.

The voltage stress that the semiconductors must be able to withstand is

equal to V_i for the primary bridge and equal to V_o for the secondary bridge.

According to Table 6, the IGBT in the active bridges can safely withstand both the voltage and current stresses, seen in Table 11.

The boards already have a heatsink mounted for the IGBTs. The thermal resistance of the heatsink is 1.2 °C/W.

According to Figure 28, which shows current waveforms for buck mode operation but can be adapted to voltage match mode by considering all currents constant during the intervals (t_1,t_2) and (t_3,t_4), the current flowing in the diodes always falls to zero, hence, diode turn off losses can be neglected. Insufficient data in the datasheet and practical challenges for experimental tests prevents diode turn on loss computation, thus it is also neglected.

At rated power, the converter operates within the ZVS operation region, meaning the power switches do not have any turn on loss. Therefore, the only switching losses to be considered is the turn off of the power switches.

The turn off switching loss can be calculated with equation (4.16), where t_f is the current fall time of the IGBT.

$$P_{sw,off} = \frac{1}{2} V_i I_1 t_f f_s = \frac{1}{2} \cdot 380 \cdot 1.75 \cdot 100 \times 10^{-9} \cdot 20 \times 10^3 = 666\, mW \qquad (4.16)$$

The conduction loss in the collector-emitter channel of an IGBT can be modeled using a DC voltage source in series with a resistor, and can be calculated with equation (4.17), where $V_{f,igbt}$ and $R_{ce,igbt}$ are estimated using data available in the datasheet of the component. Equations (4.18) and (4.19) calculates the conduction loss of the power switches in the primary and secondary bridge, respectively.

$$P_{on,ce} = V_{f,ce} I_{avg} + R_{ce} I_{rms}^2 = 0.76 I_{avg} + 0.07 I_{rms}^2 \qquad (4.17)$$

$$P_{on,ceP} = 0.76 I_P + 0.07 I_{P,rms}^2 = 0.76 \cdot 0.81 + 0.07 \cdot 1.19^2 = 724\, mW \qquad (4.18)$$

$$P_{on,ceS} = 0.76 I_S + 0.07 I_{S,rms}^2 = 0.76 \cdot 0.02 + 0.07 \cdot 0.16^2 = 18.7\, mW \qquad (4.19)$$

The conduction loss in the diodes can be calculated similarly, as shows equation (4.20). $V_{f,D}$ and R_D are also estimated using data available in the

datasheet of the component. Equations (4.21) and (4.22) calculates the conduction loss of the power switches in the primary and secondary bridge, respectively.

$$\begin{aligned} P_{on,D} &= V_{f,D} I_{avg} + R_D I_{rms}^2 \\ &= 0.37 I_{avg} + 0.09 I_{rms}^2 \end{aligned} \tag{4.20}$$

$$\begin{aligned} P_{on,DP} &= 0.37 I_{DP} + 0.09 I_{DP,rms}^2 \\ &= 0.37 \cdot 0.02 + 0.09 \cdot 0.16^2 \\ &= 10.5\ mW \end{aligned} \tag{4.21}$$

$$\begin{aligned} P_{on,DS} &= 0.37 I_{DS} + 0.09 I_{DS,rms}^2 \\ &= 0.37 \cdot 0.81 + 0.09 \cdot 1.19^2 \\ &= 431\ mW \end{aligned} \tag{4.22}$$

Finally, the junction temperature (T_j) of the power switches can be calculated. The ambient temperature (T_a) considered is 40 °C. The thermal resistance of thermal paste (R_{cd}) utilized is 0.68 °C/W. The junction-to-case temperature of the collector-emitter channel ($R_{jc,ce}$) is 0.68 °C/W, whereas the junction-to-case temperature of antiparallel diode ($R_{jc,D}$) is 1.35 °C/W (Microchip, 2008). R_{da} is the heatsink's thermal resistance.

The mathematical model used for the calculation of the thermal stress of the semiconductors and the heatsink temperature in the following paragraphs is given by Moraes (2021). This model considers that the same heatsink is used for every semiconductor.

Equation (4.23) shows the result for the heatsink temperature of the primary bridge ($T_{hs,P}$), and equations (4.24) and (4.25) shows the result for the junction temperature of the collector-emitter channel ($T_{j,ceP}$) and diode ($T_{j,DP}$) of the primary bridge, respectively.

In the same manner, equation (4.26) shows the result for the heatsink temperature of the secondary bridge ($T_{hs,S}$), and equations (4.27) and (4.28) shows the result for the junction temperature of the collector-emitter channel ($T_{j,ceS}$) and diode ($T_{j,DS}$) of the secondary bridge, respectively.

$$T_{hs,P} = 4 \cdot \left(P_{on,ce,P} + P_{sw,off} + P_{on,DP}\right)R_{da} + T_a$$
$$= 4 \cdot (0.72 + 0.666 + 0.0105) \cdot 1.2 + 40 \quad (4.23)$$
$$= 46.73\ °C$$

$$T_{j,ceP} = T_{hs,P} + \left(R_{jc,ce} + R_{cd}\right)\left(P_{on,ce,P} + P_{sw,off}\right)$$
$$= 46.73 + (0.68 + 0.68)(0.72 + 0.666) \quad (4.24)$$
$$= 48.62\ °C$$

$$T_{j,DP} = T_{hs,P} + \left(R_{jc,D} + R_{cd}\right)\left(P_{on,DP}\right)$$
$$= 46.73 + (1.35 + 0.68) \cdot 0.0105 \quad (4.25)$$
$$= 46.75\ °C$$

$$T_{hs,S} = \left(P_{on,ce,S} + P_{sw,off} + P_{on,DS}\right)R_{da} + T_a$$
$$= (0.0187 + 0.666 + 0.431) \cdot 1.2 + 40 \quad (4.26)$$
$$= 45.36\ °C$$

$$T_{j,ceS} = T_{hs,S} + \left(R_{jc,ce} + R_{cd}\right)\left(P_{on,ce,S} + P_{sw,off}\right)$$
$$= 45.36 + (0.68 + 0.68)(0.0187 + 0.666) \quad (4.27)$$
$$= 46.29\ °C$$

$$T_{j,DS} = T_{hs,S} + \left(R_{jc,D} + R_{cd}\right)\left(P_{on,DS}\right)$$
$$= 45.36 + (1.35 + 0.68) \cdot 0.431 \quad (4.28)$$
$$= 46.23\ °C$$

The junction temperature of the semiconductors calculated in equations (4.24), (4.25), (4.27) and (4.28) are much lower than the maximum junction temperature of 150 °C informed by the device's datasheet (Microchip, 2008). Therefore, the power switches can safely operate in the proposed converter.

4.2.6 Soft-Switching Limits

According to Table 6, the output capacitance of the IGBT used is $C_{oss} = 84\ pF$. Using equations from section 3.3.9, the phase-shift and power threshold in which the converter will lose the ZVS capability can be calculated.

First, the minimum switching current required for ZVS in the primary bridge is calculated through equation (4.29).

$$I_{ZVS,P} = V_i\sqrt{\frac{2C_P}{L}} = 380\sqrt{\frac{2\cdot 84\times 10^{-12}}{541.5\times 10^{-6}}} = 212\ mA \tag{4.29}$$

By rearranging equation (3.8) into equation (4.30), the phase-shift value in which $I_2 = I_{ZVS,P}$ can be found.

$$\begin{aligned}\phi_{ZVS,P} &= \frac{I_{ZVS,P}\cdot 4\cdot L\cdot f_s - V_i + V_o'}{2\cdot V_o'}\cdot 180° \\ &= \frac{0.212\cdot 4\cdot 541.5\times 10^{-6}\cdot 20\times 10^{3} - 380 + 380}{2\cdot 380}\cdot 180° \\ &= 2.17\ °\end{aligned} \tag{4.30}$$

Finally, using equation (3.10), the power threshold at which the converter will lose ZVS is given by equation (4.31).

$$\begin{aligned}P_{ZVS,P} &= \frac{nV_iV_o}{2Lf_s}\frac{\frac{\phi_{ZVS,P}}{180}}{\pi}\left(1-\frac{\left|\frac{\phi_{ZVS,P}}{180}\right|}{\pi}\right) \\ &= \frac{1\cdot 380\cdot 380}{2\cdot 541.94\times 10^{-6}\cdot 20\times 10^{3}}\frac{\frac{2.17}{180}}{\pi}\left(1-\frac{\left|\frac{2.17}{180}\right|}{\pi}\right) \\ &= 79.46\ W\end{aligned} \tag{4.31}$$

Since $n = 1$ and $K = 1$, the analysis is valid for both the primary and secondary bridge, i.e., both bridges will lose ZVS when $P < 80\ W$.

When the converter operates at the limit of the ZVS region, i.e., $\phi = \phi_{ZVS,P}$, the required time for the charging of the capacitances is given by equation (4.32).

$$t_{ZVS,P} = \frac{2\cdot V_i\cdot C_P}{I_{ZVS,P}} = \frac{2\cdot 380\cdot 84\times 10^{-12}}{0.212} = 301.6\ ns \tag{4.32}$$

As will be shown in the next chapter, the operation point used in the experiments with the lowest power transfer uses $\phi = 5.51°$, which results in a switching current of $I_2 = 537\,mA$. Equation (4.33) calculates the time of charge/discharge for this operation point.

$$t_{ZVS,P} = \frac{2 \cdot V_i \cdot C_P}{0.537} = \frac{2 \cdot 380 \cdot 84 \times 10^{-12}}{0.537} = 118.9\,ns \tag{4.33}$$

Since equation (4.33) results in a period lower than the dead time of 300 ns, all operation points utilized in the experiments with the prototype can safely operate with ZVS, due to the fact that operation points with higher power transfer - i.e., larger I_2 - will result in a lower charge/discharge period than calculated in equation (4.33).

4.2.7 Parameters Corrections

The leakage inductance from the built transformer (Table 9) and the inductance from the built inductor (Table 10) results in a higher inductance than initially calculated, as shows expression (4.35).

$$\begin{aligned} L_{meas} &= L_{dab,meas} + l_1 + l_2' \\ &= 463\,\mu H + 38.16\,\mu H + \left(\frac{99}{99}\right)^2 (38.18\,\mu H) \\ &= 539\,\mu H \end{aligned} \tag{4.34}$$

$$L_{meas} < L = 541.5\,\mu H \tag{4.35}$$

This will require a small adjustment in the ϕ_R value for the converter to reach the nominal power specification. Equation (4.36) calculates the new value.

As a result, other parameters calculated earlier in this chapter will be slightly different with the new nominal phase-shift value. Nevertheless, these differences will be ignored, given the small difference between the old and new values.

$$\phi_{R,new} = \frac{\pi}{2} \cdot \left(1 \pm \sqrt{1 - \frac{8 L_{meas} f_s P_R}{n V_i V_o}}\right) \cdot \frac{180°}{\pi}$$

$$= \frac{\pi}{2} \cdot \left(1 \pm \sqrt{1 - \frac{8 \cdot 539 \times 10^{-6} \cdot 20 \times 10^{3} \cdot 600}{n V_i V_o}}\right) \cdot \frac{180°}{\pi} \quad (4.36)$$

$$= 17.91°$$

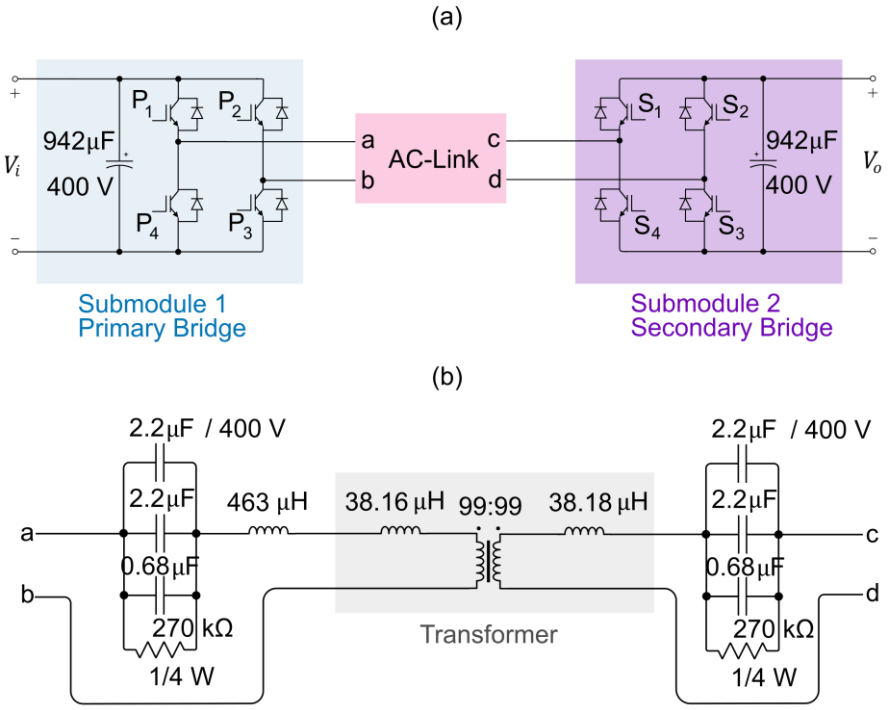
4.3 FINAL ASSEMBLY OF THE PROTOTYPE

Figure 39 shows a circuit diagram of the converter designed for experimental tests.

A development kit from Texas Instruments with a DSP, the LAUNCHXL-F28379D, is responsible for the generation of the PWM signals for controlling the power switches. Figure 40 shows a picture of the board.

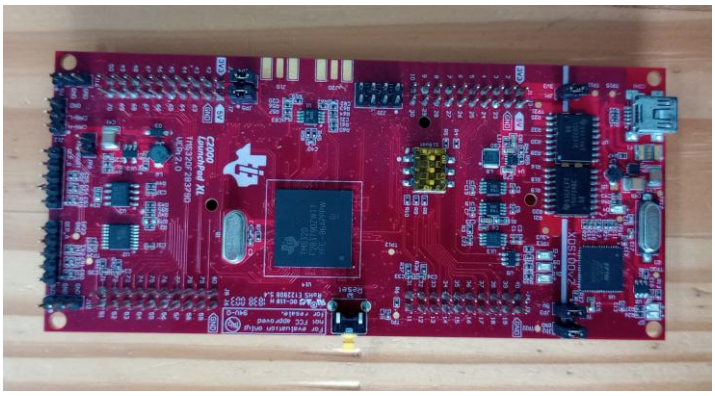
Finally, Figure 41 shows a picture of all the components assembled to form the DAB converter prototype.

Figure 39 – Prototype circuit diagram: (a) power converter (b) AC-Link.



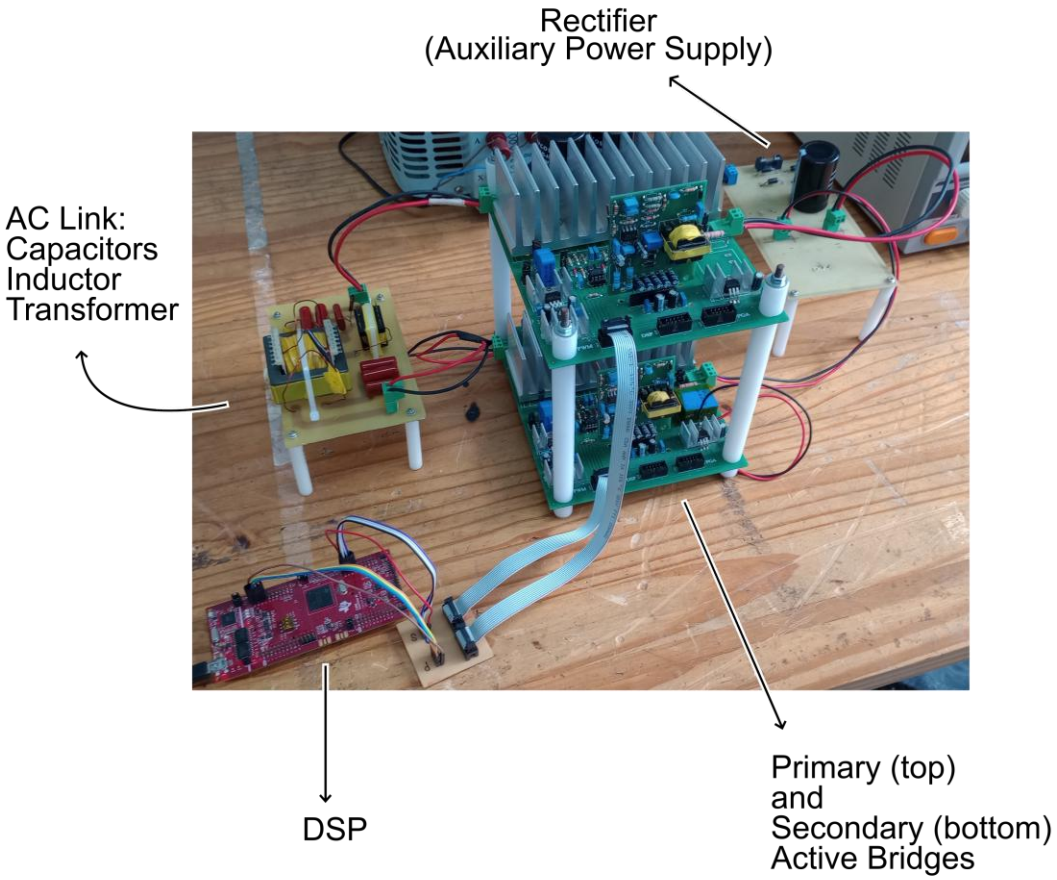
Source: provided by the author, 2025.

Figure 40 – DSP LAUNCHXL-F28379D board from Texas Instruments.



Source: provided by the author, 2025.

Figure 41 – Assembled DAB prototype and its components.



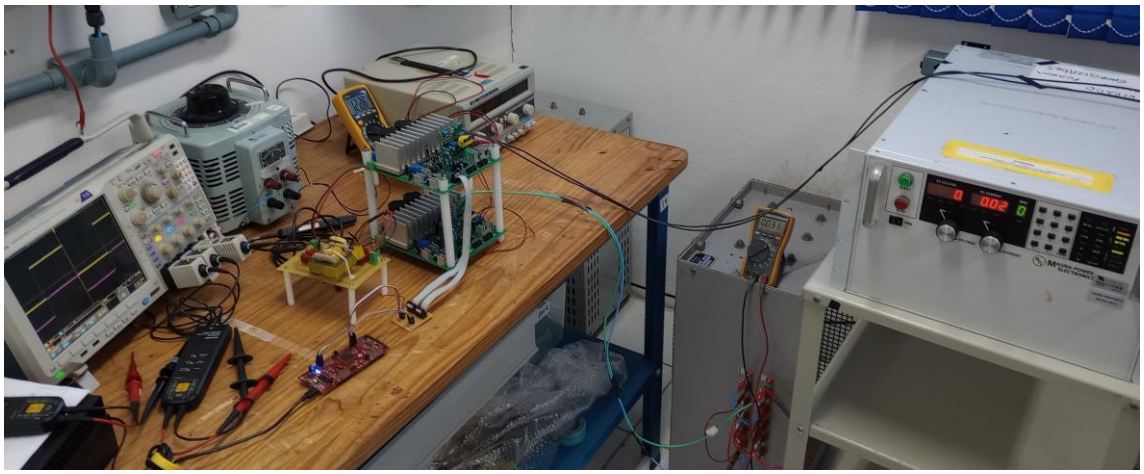
Source: Active Bridges provided by Castellain (2024). Other components provided by the author, 2025

5 EXPERIMENTAL VALIDATION OF THE PROTOTYPE

In this chapter, the DAB prototype designed in the previous chapter is tested with SPS modulation, for the purpose of validating the theoretical analysis presented in Chapter 3.

Figure 42 shows the workbench with the prototype and some of the measurement equipment for the tests. Table 27 in Appendix B shows all the equipment utilized for acquiring the measurement data and power supplies, shown in the following sections of this chapter.

Figure 42 – Setup for experimental tests with prototype for SPS modulation.



Source: provided by the author, 2025.

For the experimental tests, five points of operation are chosen for measurements, shown in Table 12. The converter is operated in open-loop. The necessary phase-shift and the power transmitted are calculated based on the specifications of the converter (Table 4), except the inductance, in which the value from Equation (4.19) is used. The equivalent resistance of the load used is based on the series connection of resistors in the resistor bank available in the laboratory, shown in Table 27.

Due to PCB construction constraints, some waveforms and measurements of interest are unable to be acquired, such as the semiconductors current and the output capacitor current.

Table 12 - Operation points for measurements acquisitions.

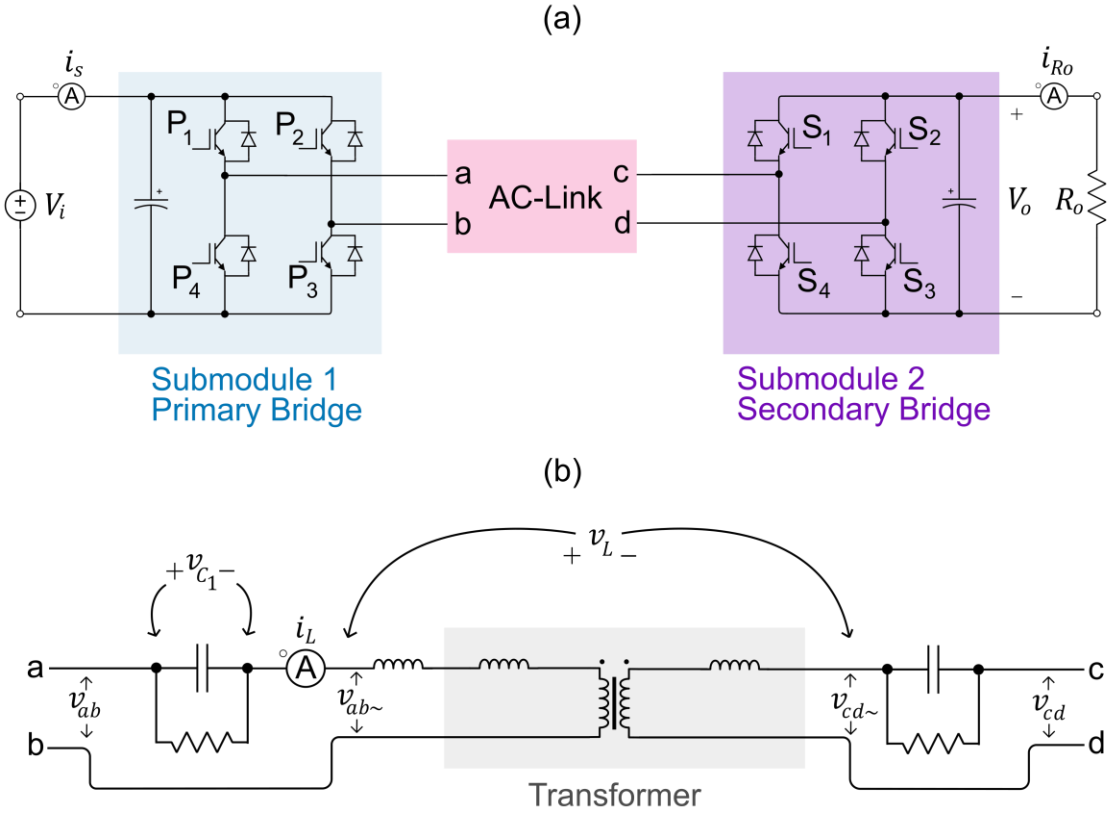
Operation Point	Load (Ω)	ϕ (°)	Output Power (%)
OP1	727	5.51	33 %
OP2	610	6.60	39 %
OP3	497	8.17	49 %
OP4	374	11.05	66 %
OP5	246	17.47	98 %

Source: provided by the author, 2025.

5.1 MAIN WAVEFORMS

Figure 43 shows where each voltage and current is measured.

Figure 43 – Measured voltages and current: (a) Converter, (b) AC-Link.



Source: provided by the author, 2025.

The main waveforms of the converter are acquired only for point OP5, which is under full load, approximately.

Figure 44 presents the waveforms of v_{ab}, v_{cd} and i_L. Figure 45 presents the waveforms of $v_{ab\sim}$, $v_{cd\sim}$ and i_L. It can be noted that v_{ab} and v_{cd} are almost identical to $v_{ab\sim}$ and $v_{cd\sim}$, respectively. That is because the voltage across the DC blocking capacitors is much lower than the amplitude of v_{ab} and v_{cd}, which makes it hard to see any kind of fluctuation in $v_{ab\sim}$ and $v_{cd\sim}$.

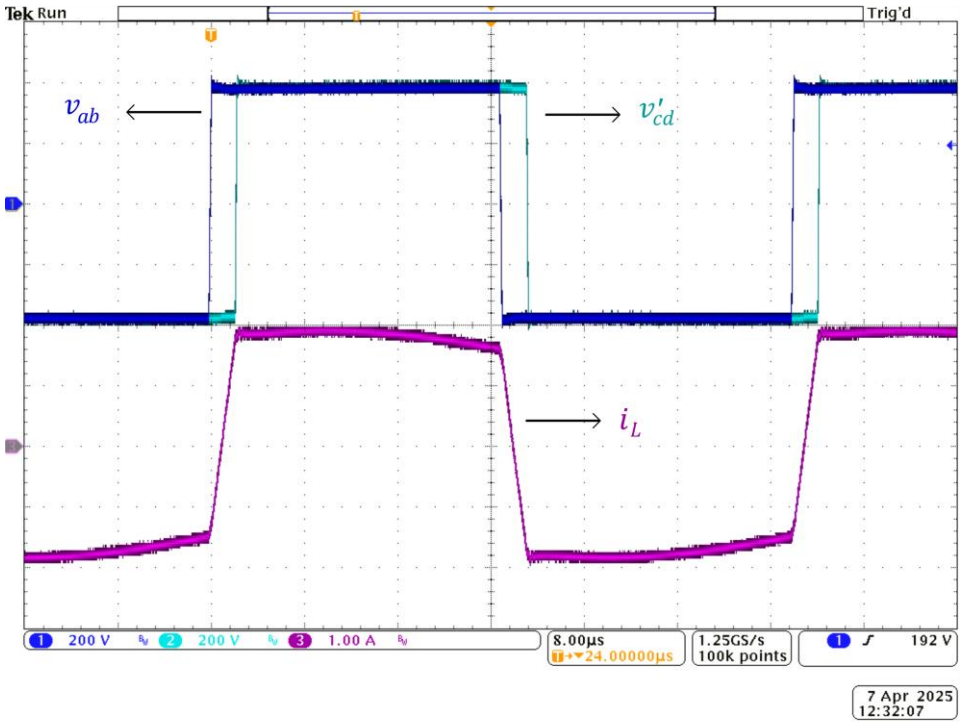
Figure 46 shows the current i_L in more detail, along with the estimated voltage $v_L = v_{ab\sim} - v_{cd\sim}$. It can be seen that i_L is not constant when both $v_{ab\sim}$ and $v_{cd\sim}$ have the same polarity, which is not expected for when the converter operates in Voltage Match mode. Rather, it shows the behavior of Boost mode, since the amplitude actually decreases when $v_{ab\sim}$ and $v_{cd\sim}$ have the same polarity. There are the many non-idealities of the converter that were not considering during the analysis. One of them is the parasitic resistance of the power switches and PCB traces. The transformer current creates a voltage drop across these resistances, which are added up to the voltage applied by the active bridges, causing the amplitude of $v_{cd\sim}$ to be slightly greater than V_o. Moreover, the voltage drop in the antiparallel diodes also affects the voltage applied to the transformer.

This can be confirmed by looking at the waveform of v_L, which gets slightly negative during the first half of T_s and slightly positive during the other half of T_s. Besides that, the DC blocking capacitor will also smooth out the shape of i_L. Figure 47 shows the voltage across the DC blocking capacitor of the primary bridge (v_{C1}).

Figure 48 shows the voltage (v_o) and current (i_{Ro}) waveforms at the load.

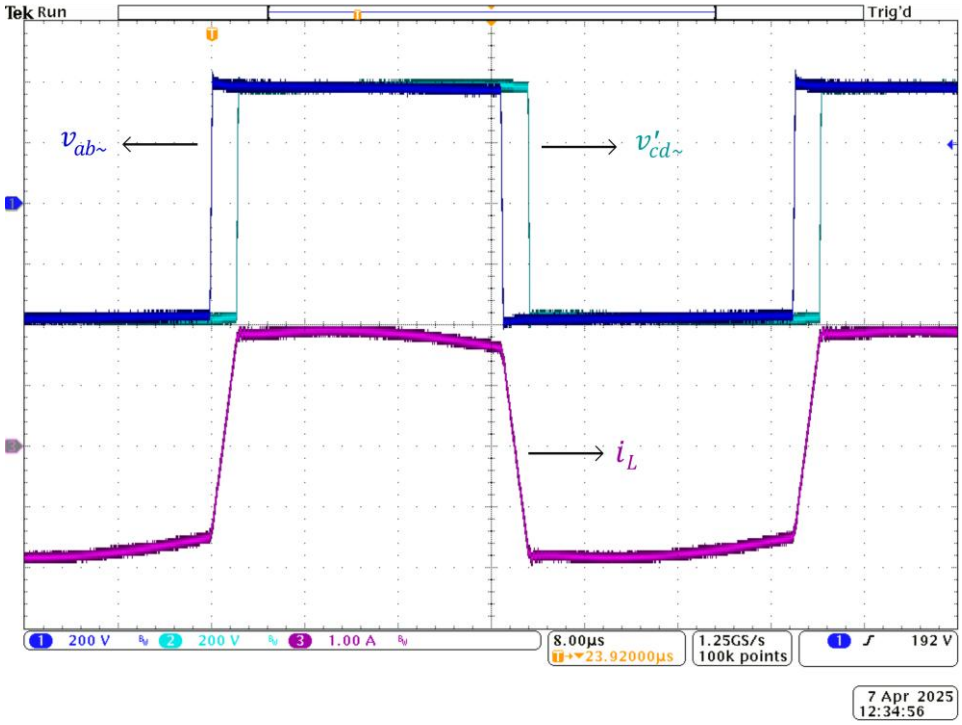
Figure 49 shows the voltage across the switch P_1 ($v_{ce,P1}$) and its command signal voltage ($v_{be,P1}$) during turn-on, along with current i_L. It can be noted that $v_{ce,P1}$ drops to zero while $v_{be,P1}$ is still negative, confirming ZVS operation of the switches in the primary bridge. During this period, i_L is negative and its amplitude is large enough to completely discharge the output capacitance of the switch before $v_{be,P1}$ turns positive.

Figure 44 – Experimental waveform results of SPS modulation: v_{ab}, v_{cd} and i_L.



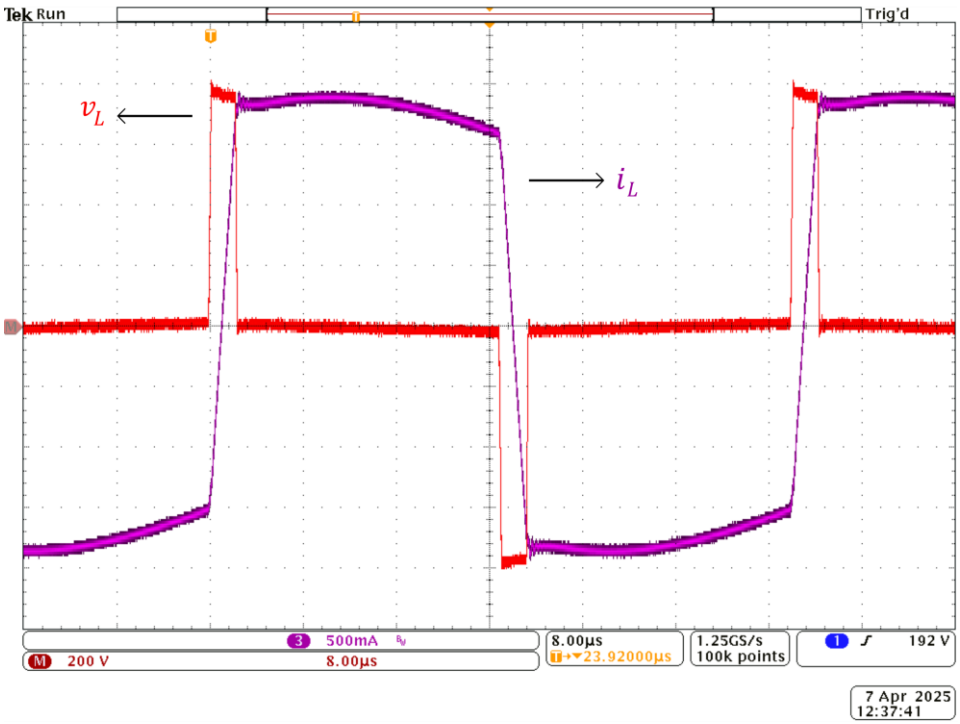
Source: provided by the author, 2025.

Figure 45 - Experimental waveform results of SPS modulation: $v_{ab\sim}$, $v_{cd\sim}$ and i_L.



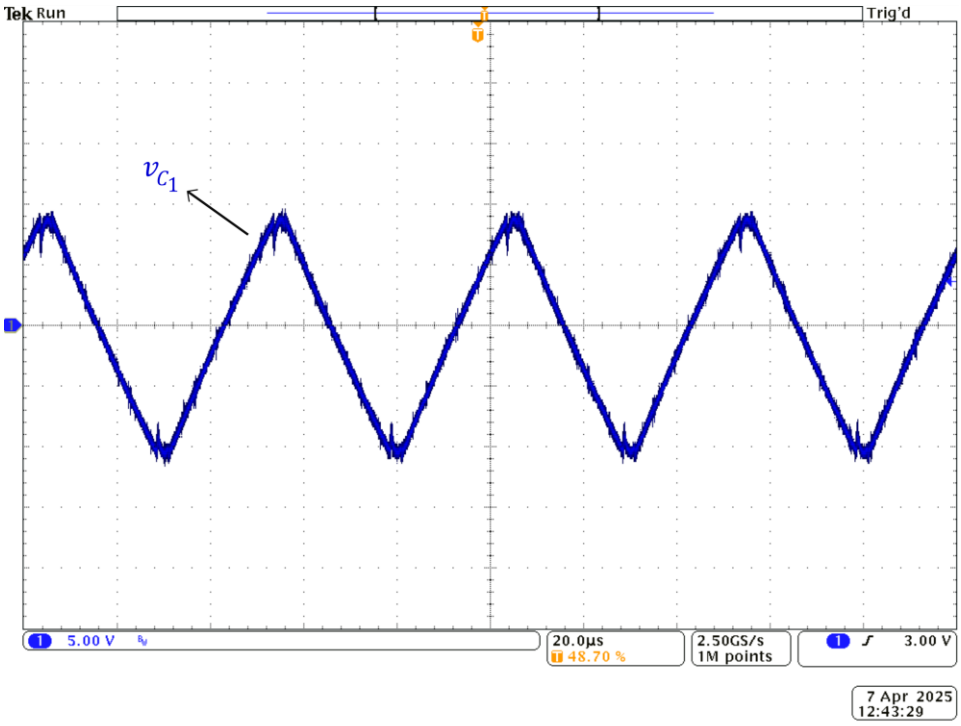
Source: provided by the author, 2025.

Figure 46 - Experimental waveform results of SPS modulation: v_L and i_L.



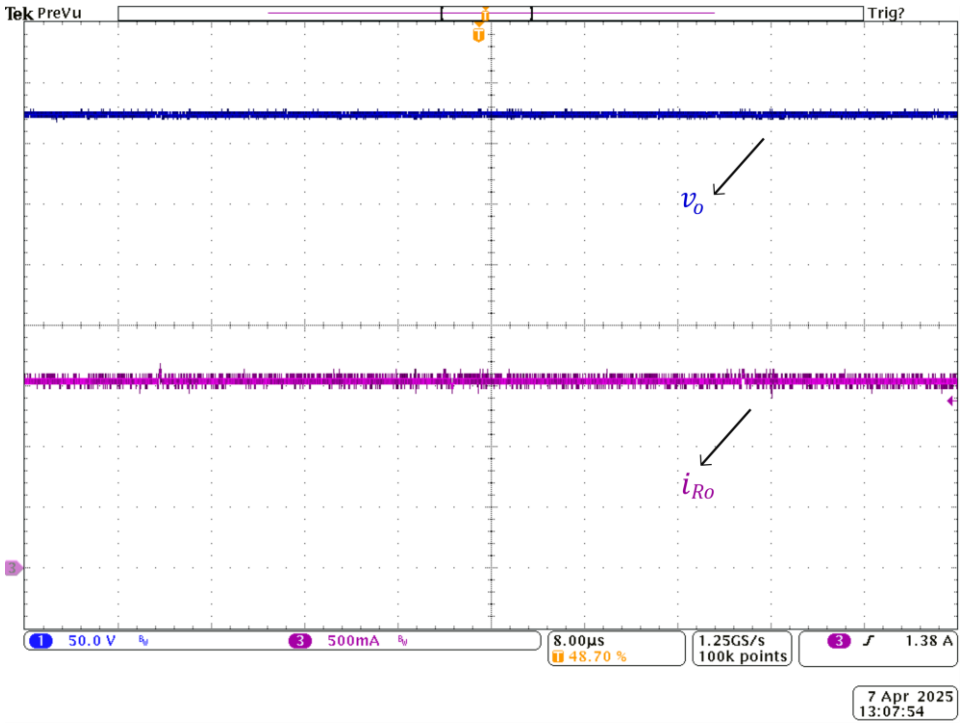
Source: provided by the author, 2025.

Figure 47 - Experimental waveform results of SPS modulation: v_{C_1}.



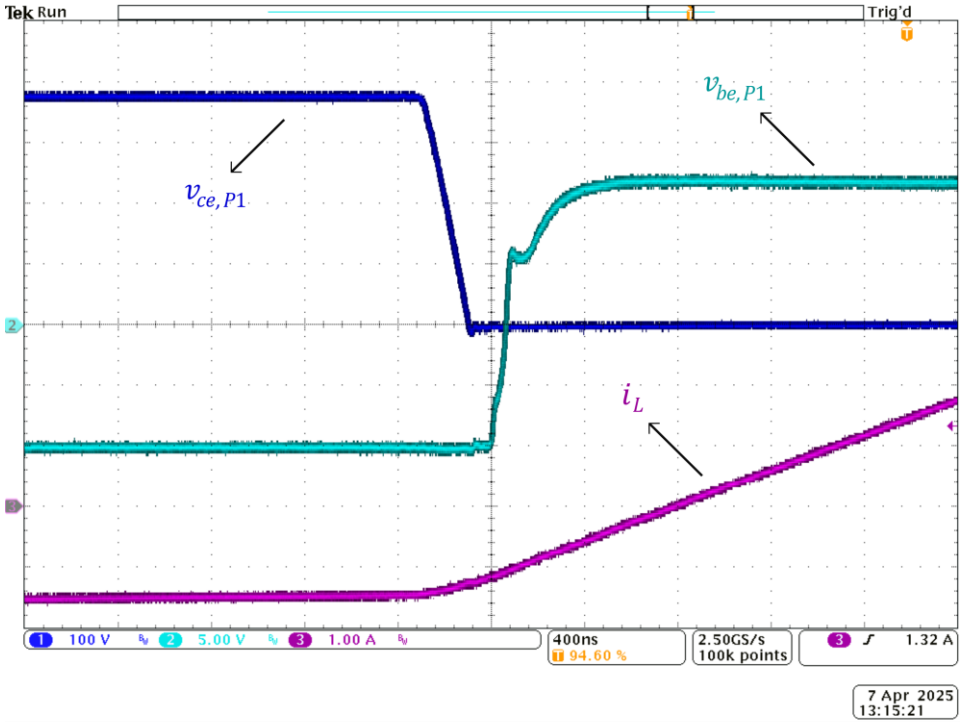
Source: provided by the author, 2025.

Figure 48 - Experimental waveform results of SPS modulation: v_o and i_{Ro}.



Source: provided by the author, 2025.

Figure 49 - Experimental waveform results of SPS modulation: $v_{ce,P1}$, $v_{be,P1}$ and i_L.



Source: provided by the author, 2025.

5.2 ESTIMATED AND MEASURED RESULTS

Measurements acquired from the operation points are compared with results from theoretical expressions derived in Chapter 3. For saving space, the following nomenclature may be used in the tables of this chapter: MM = Mathematical Model and MS = Measured.

Table 13 shows the calculated ϕ necessary for each operation point compared to the actual ϕ used in practice. The output load is measured only once before the test starts. Therefore, measured results are impacted by the change of the load's resistance over time caused by its increase in temperature during operation of the converter.

Table 13 – Actual phase-shift values used for each operation point.

Operation Point	ϕ (°)	
	Model	Actual
OP1	5.51	6.00
OP2	6.60	7.10
OP3	8.17	8.40
OP4	11.05	10.80
OP5	17.47	16.50

Source: provided by the author, 2025.

Table 14 shows results for the average value of the current from the input voltage source (I_S), i.e., input current and the input power. The measured values are expected to be greater, since the mathematical model presented in Chapter 3 considers lossless components. In other words, the input power must be greater in order to compensate for the losses in the components of the converter.

Table 15 shows results for RMS and peak values of transformer/inductor current and RMS values of the voltages at both sides. Concerning the measured values of $V_{ab\sim,rms}$ and $V_{cd\sim,rms}$, they are expected to be different than V_i and V_o, due to the DC blocking capacitors which slightly alters the waveform of the voltages applied to the total inductance (L), modifying its RMS value.

Furthermore, depending on the direction of power flow, a voltage value can be added to $v_{ab\sim}$ or $v_{cd\sim}$ because of the voltage drop on non-idealities of components, such as PCB trace resistances and winding resistance. Since the converter is operating with positive power flow, a voltage is added on the secondary side of the transformer, i.e., $v_{cd\sim}$, increasing its amplitude.

Table 14 – Experimental results of input current and input power.

Operation Point	I_S (A)		P_i (W)	
	Model	Measured	Model	Measured
OP1	0.52	0.55	198.74	208.58
OP2	0.62	0.65	236.57	249.56
OP3	0.76	0.82	290.20	310.00
OP4	1.01	1.08	385.92	411.80
OP5	1.54	1.64	586.95	622.85

Source: provided by the author, 2025.

Table 15 – Experimental results of current and voltages on the transformer.

Operation Point	$I_{L,rms}$ (A)		$I_{2,rms}$ (A)		$V_{ab\sim,rms}$ (V)		$V_{cd\sim,rms}$ (V)	
	MM	MS	MM	MS	MM	MS	MM	MS
OP1	0.53	0.55	0.53	0.55	380	385	380	384
OP2	0.64	0.66	0.64	0.67	380	383	380	386
OP3	0.79	0.83	0.79	0.82	380	384	380	386
OP4	1.06	1.11	1.06	1.12	380	384	380	386
OP5	1.65	1.71	1.65	1.72	380	384	380	386

Source: provided by the author, 2025.

Table 16 shows results of the switching currents at both sides of the transformer.

Table 17 shows the results of the transformer-inductor set apparent power (S_T), which is estimated with Equation (3.37) using the measured values of Table 15. The difference between the results is in agreement with the other results so far.

Table 16 - Experimental results of the switching currents.

Operation Point	I_1 (A)		I_2 (A)		$I_{1,sec}$ (A)		$I_{2,sec}$ (A)	
	MM	MS	MM	MS	MM	MS	MM	MS
OP1	0.54	0.66	0.54	0.48	0.54	0.81	0.54	0.31
OP2	0.65	0.81	0.65	0.53	0.65	0.95	0.65	0.39
OP3	0.80	0.95	0.80	0.73	0.80	1.05	0.80	0.57
OP4	1.08	1.27	1.08	0.99	1.08	1.37	1.08	0.83
OP5	1.71	1.85	1.71	1.57	1.71	2.00	1.71	1.38

Source: provided by the author, 2025.

Table 17 – Experimental results of the transformer apparent power.

Operation Point	S_T (VA)	
	Model	Estimated
OP1	202.92	211.47
OP2	242.56	255.70
OP3	299.36	317.62
OP4	402.65	429.28
OP5	628.65	660.28

Source: provided by the author, 2025.

Regarding Tables 15 and 16, the difference between the magnitude of the currents in the primary and secondary is due to the discrete inductor being placed at the primary side of the converter. For this reason, the current of the magnetizing inductance of the transformer is provided by the secondary bridge, thus increasing its current (Guenter *et al*., 2023).

Moreover, the equations derived in this thesis considers an infinite magnetizing inductance of the transformer, whereas in practice, this value is finite and can increase the magnitude of the current i_L, which explains the difference between mathematical model and measured values.

Table 18 shows results for output current and output power. The table shows that the measurements of point OP1, OP2 and OP5 are very close to the expected values, whereas OP3 and OP4 have slightly different values.

Table 18 – Experimental results of output current and power.

Operation Point	I_{Ro} (A)		P_o (W)	
	Model	Measured	Model	Measured
OP1	0.52	0.52	198.74	198.03
OP2	0.62	0.62	236.57	237.80
OP3	0.76	0.78	290.20	297.47
OP4	1.01	1.04	385.92	393.70
OP5	1.54	1.55	586.95	589.50

Source: provided by the author, 2025.

Table 19 shows results of the ripple and peak values of the DC blocking capacitor voltage in the primary side. Although the shape of v_{c1} (see Figure 47) is as expected, the measured values are approximately double the mathematical model values. It is believed that one of the 2.2 μF capacitors had a bad solder and was not connected in parallel with the other two capacitors during the tests, which would explain these values being almost double than expected.

The AC-link board ended up being modified before these results were analyzed (to fix problems from later tests). Thus, it would've been required to measure every parameter in this section again just in order to get the correct values for Table 19. Due to time constraints, it was decided to maintain these results.

Table 19 – Experimental results of DC blocking capacitor voltage.

Operation Point	ΔV_C (V)		$V_{max,C1}$ (V)	
	Model	Measured	Model	Measured
OP1	2.61	7.00	1.30	3.50
OP2	3.12	8.00	1.56	4.00
OP3	3.85	9.60	1.92	4.60
OP4	5.16	8.06	2.58	6.50
OP5	8.01	19.00	4.00	9.50

Source: provided by the author, 2025.

The differences between mathematical model and measurements are expected for many reasons: non-ideal behavior from real components (parasitic resistances, inductances and capacitances, delays in switching, unmatched parameters between power switches, measurement noise and others) and the fact that the expressions were derived for an ideal lossless converter without the DC blocking capacitors in series with the transformer. Phase-shift values used in practice are different to compensate these unconsidered aspects in the theoretical analysis.

Table 20 shows the measured temperatures of the transformer and inductor during the tests of each operation point. Initial temperatures of the magnetic cores are 28.5 °C and 22.5 °C for the transformer and inductor, respectively. The temperatures at OP5 are close to what was defined during the design.

Table 20 – Experimental results of the temperature in the magnetic cores.

Operation Point	Temperature (°C)	
	Transformer	Inductor
OP1	35.0	36.5
OP2	36.0	34.0
OP3	42.0	40.0
OP4	50.5	51.0
OP5	77.5	80.0

Source: provided by the author, 2025

5.3 EFFICIENCY OF THE POWER STAGE

The efficiency of the prototype is estimated using the equations of Chapter 4 and measurements of the inductor and transformer that were built. Table 21 presents a comparison of the estimated efficiency with the measured efficiency of the prototype. It can be seen that the maximum difference is of 2.43% and the minimum is 1.04%.

Figure 50 presents the mathematical model curve (blue) of the efficiency in function of ϕ and P, as well as the experimental results (purple) from Table 21.

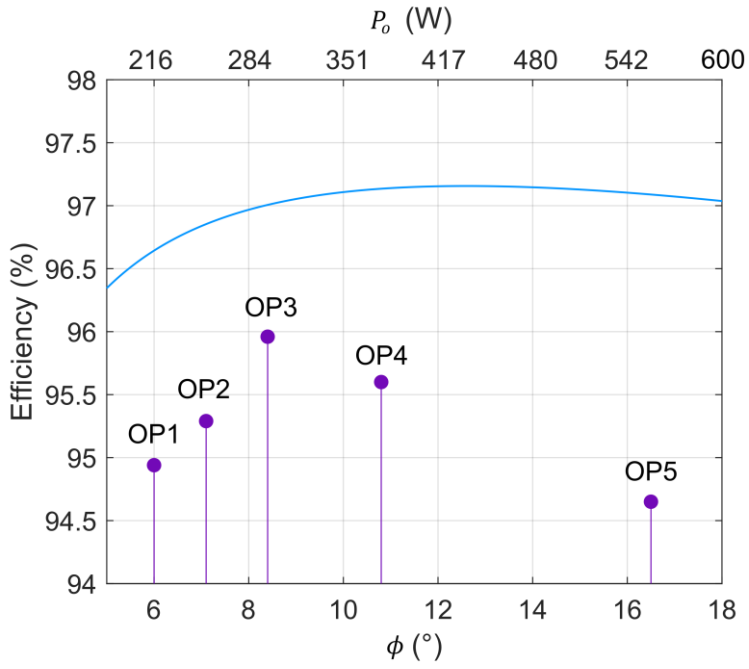
It is clear that the tendency curve formed by the experimental points starts to decrease much earlier than the estimated curve. This is likely because the IGBTs of the active bridges have already been used for other projects and its performance might have degraded due to past tests, thus making the use of the datasheet's parameter for loss estimative not so much accurate. More tests should be done to find out the exact reason for such differences in the results, but such investigation is beyond the scope of this thesis.

Table 21 – Efficiency estimates and measurements from each operation point.

Operation Point	Efficiency (%)	
	Model	Measured
OP1	96.64	94.94
OP2	96.85	95.29
OP3	97.00	95.96
OP4	97.13	95.60
OP5	97.08	94.65

Source: provided by the author, 2025.

Figure 50 – Plot of efficiency estimative (continuous line) and experimental results (dots) for the prototype operating with SPS modulation.



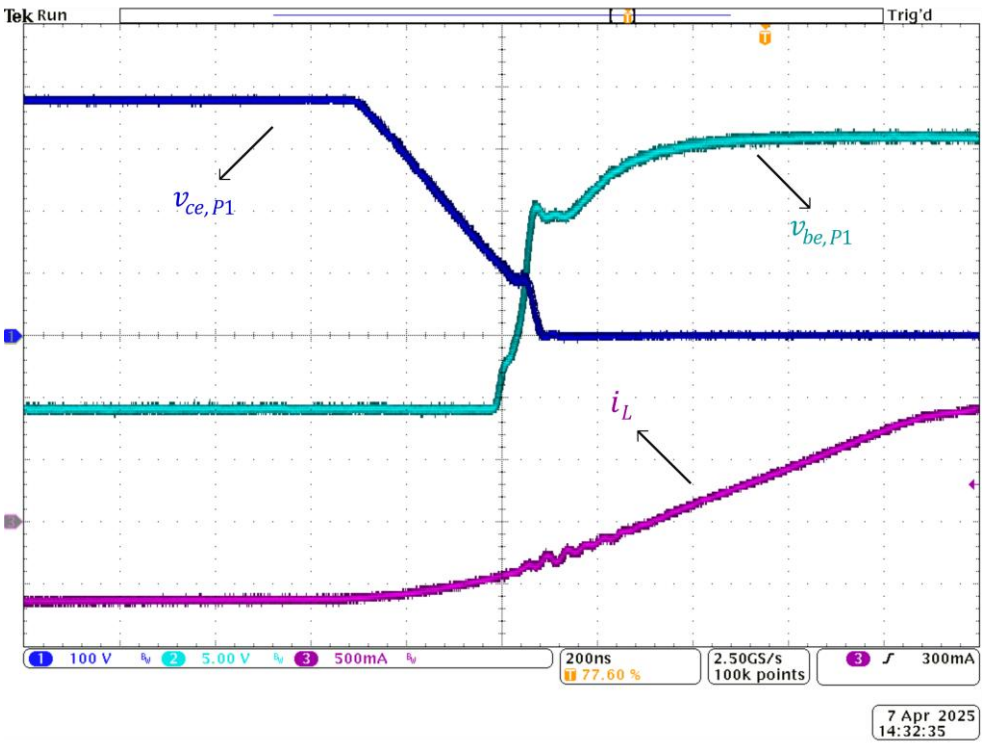
Source: provided by the author, 2025

5.4 OPERATION POINTS OUT OF ZVS REGION

It can be noticed that the lowest phase-shift value is 6° (point OP1), which is greater than $\phi_{ZVS,P}$ calculated in the previous chapter, section 4.2.6. This means that the converter should be operating with ZVS for all the operation points in Table 12.

However, during tests of the prototype, it is noted that the primary bridge is actually not operating with ZVS for OP1 to OP3. Figure 51 shows the waveforms for OP3, where $\phi = 8.4°$: the voltage across the switch P_1 ($v_{ce,P1}$) and its command signal voltage ($v_{be,P1}$) during turn-on, along with current i_L. It can be seen that $v_{ce,P1}$ is still decreasing when the $v_{be,P1}$ receives the command to turn positive, interrupting the process of ZVS, which was nearly at the end. One solution would be increasing the dead-time, however, it would mess with the converter's operation due to the phase-shifting period t_1.

Figure 51 - Experimental waveform results of SPS modulation: $v_{ce,P1}$, $v_{be,P1}$ and i_L for OP3.



Source: provided by the author, 2025.

This indicates that other parasitic capacitances present in other elements, such as the transformer and the additional inductor, are probably influencing the circuit and increasing the required current for discharging the output capacitance of the power switch, since the other capacitances also needs to be charged/discharged as well.

Parasitic resistances and the magnetizing inductance of the transformer are other elements that modifies the ZVS region of the converter. Nevertheless, the equations derived in this thesis does not considers these elements, which might be one of the explanations for the differences between the theoretical and experimental results.

6 DUAL PHASE-SHIFT MODULATION

In this chapter, the operation principle of the DAB converter using the DPS modulation is briefly described. Later, an algorithm is proposed to minimize the RMS and the peak value of the transformer current, which decreases conduction and magnetic core losses, thus increasing the efficiency of the converter. The algorithm is developed for when the converter operates with a specific condition, presented in the next sections. The analysis is done for positive power flow only.

6.1 OPERATION OVERVIEW

In the DPS modulation, there are two control variables, which are commonly referred as: the external phase-shift ϕ and the internal phase-shift ϕ_{int}. The external phase-shift is the same control variable of the SPS modulation. The internal phase-shift is applied between the command signals of the power switches in the same bridge, and it is equal for both bridges.

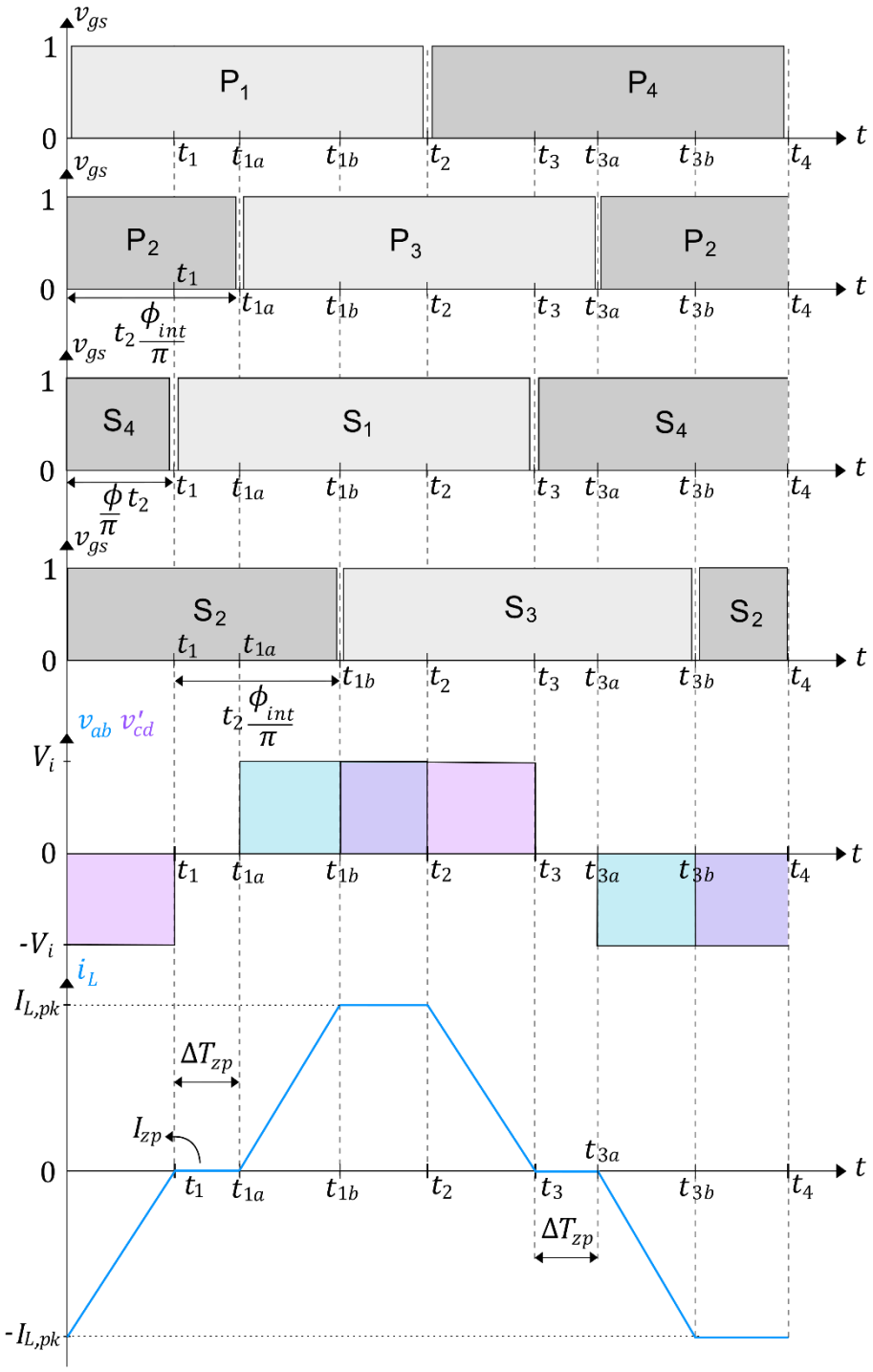
The addition of the internal phase-shift results in a three-level voltage waveform at the output voltage of the bridge: $+V$, 0 and $-V$. This is the same principle that is applied on full bridge inverters to achieve a three-level output voltage.

Figure 52 shows the switching signals with the definitions of ϕ and ϕ_{int}, as well as the voltage waveforms of v_{ab} and v_{cd} and the current waveform of i_L for the case of $\phi_{int} > \phi \ \wedge \phi_{int} < 90° \ \wedge \phi < 90°$ when operating in Voltage Match mode.

Figure 53 shows other possible combinations of ϕ and ϕ_{int} with their respective voltage and current waveforms.

As can be seen in Figure 52 and Figure 53, the new control variable allows shaping the transformer current in different ways, which creates optimization possibilities, especially for the medium to low power range of the converter. On the other hand, the converter analysis becomes more complex. Equations are much more difficult and time consuming to derive, and also requires more processor power in digital control systems.

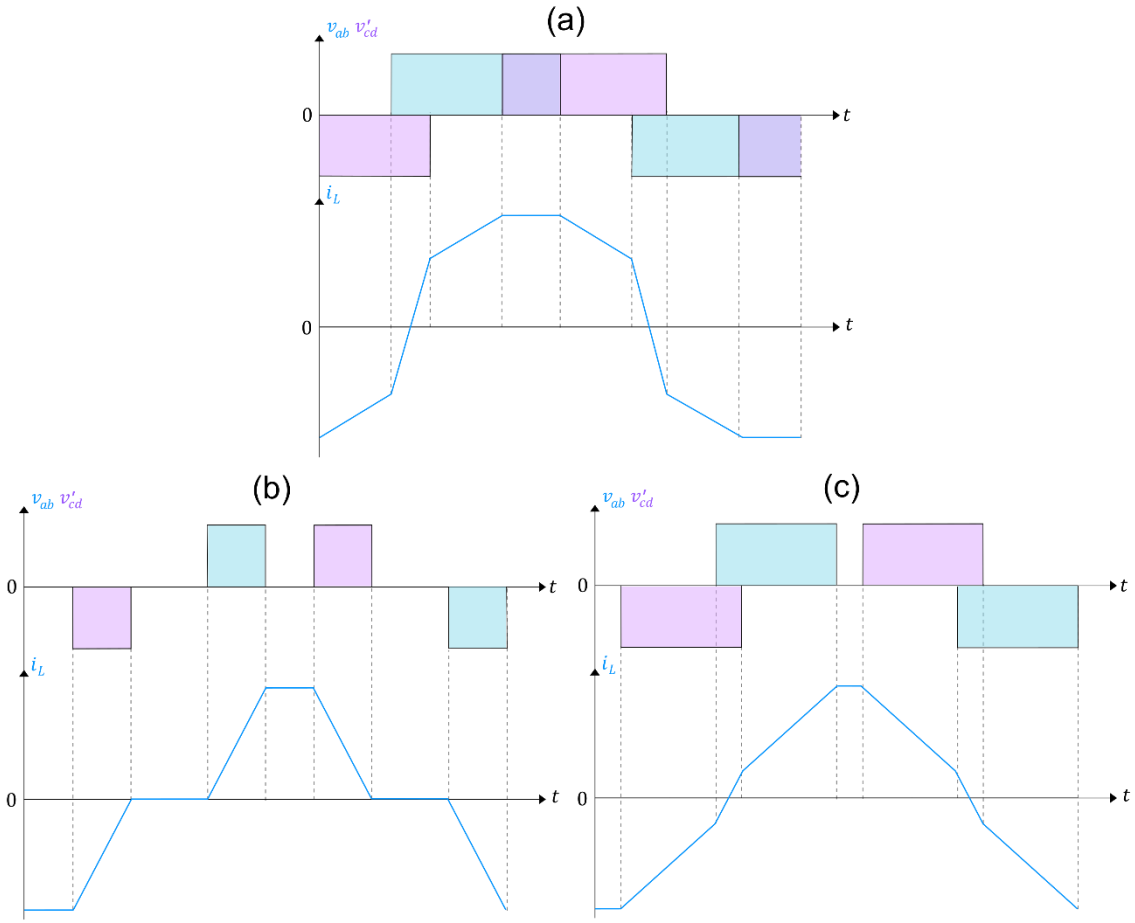
Figure 52 – Main waveforms for DPS modulation operating in Voltage Match mode and $\phi_{int} > \phi \wedge \phi_{int} < 90° \wedge \phi < 90°$.



Source: provided by the author, 2025.

The power transmitted P can be calculated with equation (6.2) (Kim et al., 2011). Figure 54 shows the plot of the normalized power transmitted $\bar{P} = P/P_b$ as a function of ϕ and ϕ_{int}.

Figure 53 – Different i_L shapes for other conditions in Voltage Match mode: a) $\phi_{int} < \phi \wedge \phi_{int} < 90° \wedge \phi < 90°$; b) $\phi_{int} > \phi \wedge \phi_{int} > 90° \wedge \phi < 90°$; c) $\phi_{int} < \phi \wedge \phi_{int} < 90° \wedge \phi > 90°$.

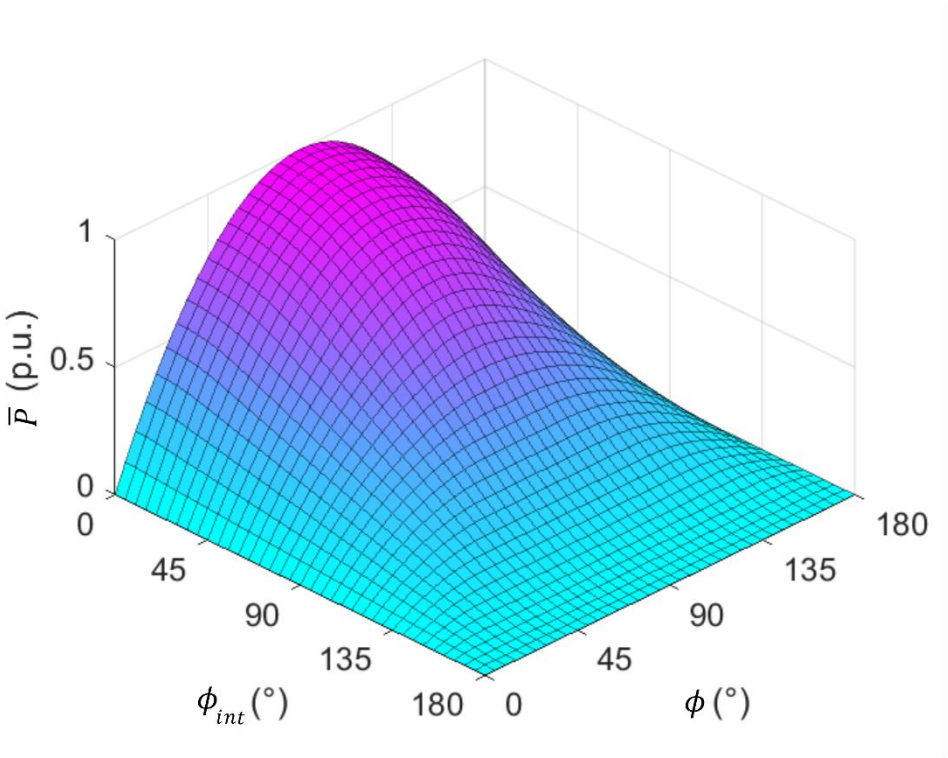


Source: provided by the author, 2025.

$$P_b = \frac{nV_oV_i}{8f_sL} \tag{6.1}$$

$$P = P_b \begin{cases} 2\dfrac{|\phi|}{180}\left(1 - \dfrac{|\phi_{int}|}{180} - \dfrac{1}{2}\dfrac{|\phi|}{180}\right) & \forall\ \phi + \phi_{int} < 180 \wedge \phi_{int} \geq \phi \\ 2\left[\dfrac{|\phi|}{180} - \left(\dfrac{|\phi|}{180}\right)^2 - \dfrac{1}{2}\left(\dfrac{|\phi_{int}|}{180}\right)^2\right] & \forall\ \phi + \phi_{int} < 180 \wedge \phi_{int} < \phi \\ \left[1 - 2\cdot\dfrac{|\phi_{int}|}{180} + \left(\dfrac{|\phi_{int}|}{180}\right)^2\right] & \forall\ \phi + \phi_{int} \geq 180 \wedge \phi_{int} \geq \phi \\ \left[1 + 2\dfrac{|\phi||\phi_{int}|}{180^2} - 2\dfrac{|\phi_{int}|}{180} - \left(\dfrac{|\phi|}{180}\right)^2\right] & \forall\ \phi + \phi_{int} \geq 180 \wedge \phi_{int} < \phi \end{cases} \tag{6.2}$$

Figure 54 – Normalized power transmitted plot versus ϕ and ϕ_{int} for DPS modulation.



Source: provided by the author, 2025.

As can be seen in Figure 54, there are many possible phase-shift pair values that can be used to transfer the same value of active power. However, other parameters such as RMS value of the inductor current, circulating power and peak value of the inductor current are different for each phase-shift pair (Kim et al., 2011). Hence, depending on the optimization objective, a different phase-shift pair value can be used to improve a certain aspect of the converter operation.

Moreover, it can be seen that the possibilities for improvement belongs in the lower to intermediate power range of the converter, since under maximum power level $\phi = 90°$ and $\phi_{int} = 0°$, which is essentially the SPS modulation.

In the particular conditions of $\phi_{int} > \phi \wedge \phi_{int} < 90° \wedge \phi < 90°$, illustrated in Figure 52, there is a period in which no active power is transferred between the input and output ports of the converter. This happens when both the voltages v_{ab} and v_{cd} are zero at the same time (e.g., at the $[t_1, t_{1a}]$ interval). Current does not flow through the input and output ports, but it might still flow through the

transformer and the power switches. Thus, only conduction losses are generated during this period.

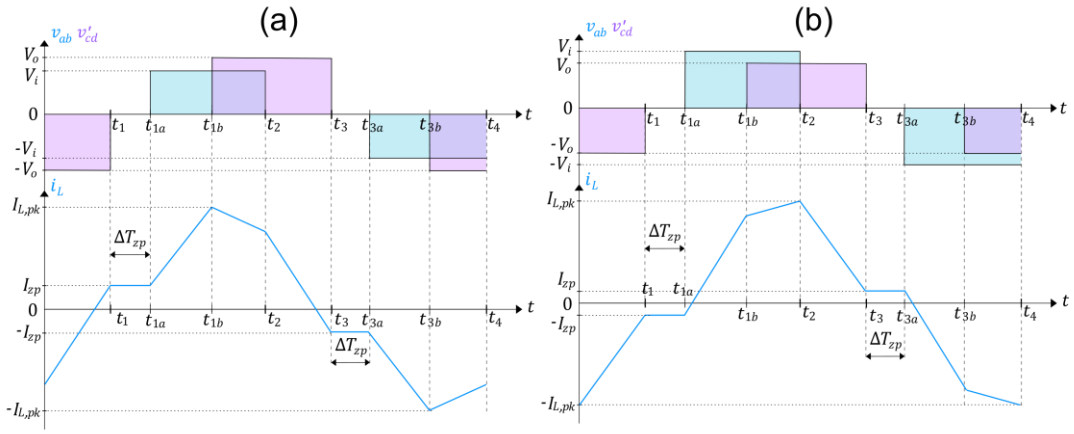
In Voltage Match mode, the inductor current during this period is zero, as shown in Figure 52. However, this does not happen for boost and buck modes, as can be seen in Figure 55. The waveform of currents i_i and i_o for modes buck and boost can be seen in at Appendix C.

This also happens when $\phi_{int} > \phi \wedge \phi_{int} > 90° \wedge \phi < 90°$ or $\phi_{int} < \phi \wedge \phi_{int} < 90° \wedge \phi > 90°$, but these conditions are not covered because the current $I_{L,rms}$ is much greater in these cases.

Many DPS-based modulation strategies proposed focus on reducing either the overall conduction loss, circulating power or improving the ZVS region of the converter, but none offered an analysis or solution for improving this particular aspect of the converter operation.

Therefore, in the next section, an investigation to verify if it is possible to improve this aspect is done.

Figure 55 - v_{ab}, v'_{cd} and i_L waveforms in DPS modulation when $\phi_{int} > \phi \wedge \phi_{int} < 90° \wedge \phi < 90°$ for: a) Boost mode; b) Buck mode.



Source: provided by the author, 2025.

6.2 CURRENT STRESS UNDER THE CONDITION $\phi < \phi_{int}$

In order to verify a possible solution, two target parameters are defined: I_{zp} and ΔT_{zp}, seen in Figure 52 and Figure 55. This period in which there is no active power being transferred is designated as “zero-power” in this thesis.

The inductor current is constant during the zero-power period, thus I_{zp} is a constant value. For reducing losses, I_{zp} should be reduced. It is important to note that the value of I_{zp} will impact on the ability of the switches to operate with ZVS. Furthermore, ΔT_{zp} should also be reduced, to increase the period in which the converter is actually transferring active power.

As stated before, deriving equations to analyze the behavior of the target parameters can be exhaustive. Hence, to understand how the control variables ϕ and ϕ_{int} modify these parameters, a series of simulations in PLECS 4.8.6 are done to gather some data. Specifically, the parameters P, I_{zp}, ΔT_{zp}, $I_{L,rms}$ and $I_{L,pk}$ are analyzed for various operation points.

The simulations are done for all three operation modes of the converter: voltage match, boost and buck, i.e., $K = 1$, $K > 1$ and $K < 1$, respectively. The converter parameters are the same as presented in Table 4 with $L = 594\,\mu H$, unless stated otherwise.

For a fair comparison, data from operation points with the same level of power transmitted have to be considered. For this purpose, the power level of $P \approx 300\,W$ is chosen for the Voltage Match mode. Table 22 presents the parameters values of the operation points for the given power transmitted.

Table 22 – Simulation results in Voltage Match mode for investigation of DPS modulation.

ϕ (°)	ϕ_{int} (°)	P (W)	I_{zp} (mA)	ΔT_{zp} (μs)	$I_{L,rms}$ (A)	$I_{L,pk}$ (A)
20	90	299.35	6.94	9.66	1.21	1.78
18	80	306.43	6.93	8.50	1.15	1.60
16	70	305.25	6.85	7.40	1.08	1.42
14	60	295.82	6.68	6.32	0.99	1.24
12	40	300.57	6.68	3.89	0.92	1.07

Source: provided by the author, 2025.

It can be seen in Table 22 that I_{zp} is not zero. There are a few reasons that can lead to this: a DC component in $i_L(t)$; Voltage drops on the parasitic resistances of the PCB traces might increase the voltage applied to the

transformer, which would modify the shape of the current; Dead time will cause slightly different slew rates of the voltages applied to the transformer in a switching period. Since this analysis considers an ideal converter, the results for I_{zp} are not much relevant for developing the solution.

For the Boost mode simulations, $V_i = 350\ V$ and $V_o = 380\ V$. Vice-versa for Buck mode simulations. Table 23 presents the data collected of the operation points for $P \approx 250\ W$. Due to the symmetrical nature of the converter, the results for Buck and Boost mode are almost identical.

Table 23 - Simulation results in Buck and Boost modes for investigation of DPS modulation.

(ϕ,ϕ_{int}) (°)	P (W)		I_{zp} (mA)		ΔT_{zp} (μs)		$I_{L,rms}$ (A)		$I_{L,pk}$ (A)	
	Buck	**Boost**	**Buck**	**Boost**	**Buck**	**Boost**	**Buck**	**Boost**	**Buck**	**Boost**
(18,90)	252.5	251.0	310	320	10.00	9.96	1.08	1.08	1.79	1.78
(16,80)	255.0	253.3	340	360	8.86	8.85	1.03	1.03	1.66	1.66
(14,70)	249.9	248.1	380	390	7.74	7.73	0.96	0.96	1.53	1.53
(12,50)	258.1	255.9	450	460	5.25	5.28	0.92	0.91	1.44	1.44
(10,30)	251.6	249.2	520	530	2.77	2.75	0.85	0.84	1.34	1.34

Source: provided by the author, 2025.

By looking at Table 22 and Table 23, a couple of conclusions can be made:

- As the value of the phase-shift pair decreases, I_{zp} increases, while ΔT_{zp} decreases.
- As the value of the phase-shift pair decreases, both $I_{L,rms}$ and $I_{L,pk}$ decrease.

6.2.1 Final Remarks

With the data shown, choosing the phase-shift pair which minimizes I_{zp} might not be the best choice, since this will increase the other parameters analyzed (ΔT_{zp}, $I_{L,rms}$ and $I_{L,pk}$). Besides that, there isn't a significant reduction of I_{zp}, which is approximately 200 mA between the maximum and minimum value

of Table 23, which are from phase-shift pairs (18°, 90°) and (10°, 30°). This is about the same difference between the maximum and minimum value obtained of $I_{L,rms}$. The biggest difference comes from the maximum and minimum value of $I_{L,pk}$, which is about 400 mA.

Of course, utilizing a phase-shift values with more decimal points can yield large reductions for I_{zp}. However, this comes at the expense of increasing $I_{L,rms}$ and $I_{L,pk}$, which are much more important parameters when trying to increase the efficiency of the converter. Furthermore, if I_{zp} is increased, it might guarantee that the power switches operate with ZVS.

As seen in the mathematical model of the converter operating with SPS presented in Chapter 3, and also from equations of $I_{L,rms}$ and $I_{L,pk}$ derived from DPS modulation by Kim et al. (2011), using the lowest phase-shift pair possible will result in the lowest current stress.

More possibilities of improvement can be achieved if f_s is modified, but it is out of the scope of this thesis.

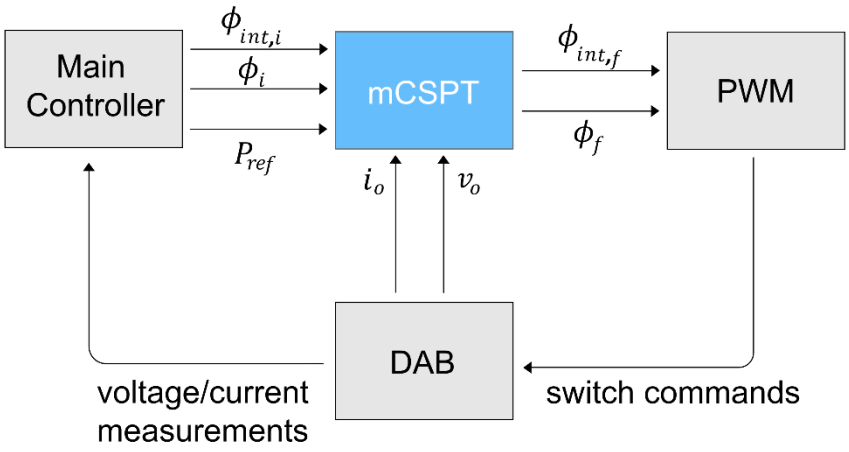
6.3 ALGORITHM PROPOSAL

In light of the investigation's outcomes, this thesis proposes an online algorithm to automatically find the lowest phase-shift pair value for a given power level (or output voltage). The algorithm stems from solar inverters' MPPT algorithms, which uses Perturb & Observe techniques to track the maximum power operation point. In this case, the algorithm tracks the minimum current stress operation point. Thus, it is going to be referred as minimum Current Stress Point Tracking (mCSPT).

The algorithm is supposed to be executed when the converter is already in steady state at the desired power level. Therefore, there needs to be a main controller that provides the initial values of the phase-shift pair. The design of such controller will not be covered in this thesis since it could be used with any controller. For example, a standard PI controller for SPS, in which a design method is presented by Santos-Silva (2019), with a fixed ϕ_{int} value could be used, among other modulations strategies more elaborated such as presented

by Kim et al. (2011) or Ding et al. (2021). Figure 56 presents a block diagram of the system with the proposed algorithm.

Figure 56 – Block diagram of a control system using the mCSPT algorithm.



Source: provided by the author, 2025.

The external controller may be configured to limit operation of the converter under the conditions of $\phi_{int} > \phi \wedge \phi_{int} < 90° \wedge \phi < 90°$, which can reduce EMI caused by the converter since the switches are activated one by one. Hence, the developed algorithm will be demonstrated only for this case.

The advantage of using an automatic and online algorithm is that it does not rely on mathematical expressions, which would require accurately measured converter parameters. Otherwise, theoretical and experimental results would notably deviate due to non-ideal aspects of the converter, such as dead-time, mismatch in switches' turn on/off times and signal delays. The goal for the developed algorithm is for its implementation to be as simple as possible.

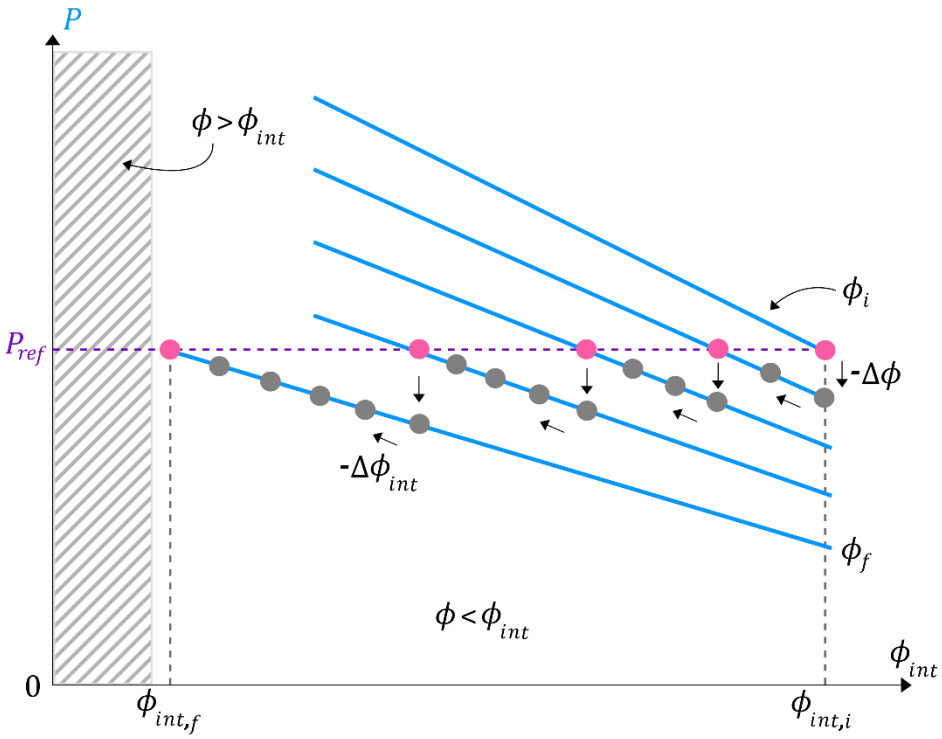
6.3.1 Description of the Algorithm Operation

The mCSPT operation is based on a simple action: decrementing both phase-shift values in steps, one phase-shift at a time, until they reach the minimum value necessary for delivering the required active power.

Figure 57 illustrates the idea by showing the power transmission plot versus the internal phase-shift, where each curve has a different ϕ value.

Basically, the algorithm walks through every operation point that can transmit the desired active power until it reaches the last one.

Figure 57 – Plot of P versus ϕ_{int} and ϕ, illustrating the operation of the mCSPT algorithm.



Source: provided by the author, 2025.

For a demonstration considering a resistor as a load, the algorithm is going to use the output voltage as a reference ($V_{o,ref}$), instead of the active power transfer. This will simplify the implementation of the algorithm by requiring only an output voltage sensor. Furthermore, it is assumed that the initial values of the phase-shift pair will be the highest possible.

Four algorithm parameters are defined for its operation: the external phase-shift step ($\Delta\phi$), the internal phase-shift step ($\Delta\phi_{int}$), a voltage margin tolerance (V_{tol}) and a waiting period (T_w). The waiting period is necessary for the settling time of v_o after a phase-shift step, due to the dynamics of the output capacitor. If T_w is not enough for v_o to achieve steady state after a phase-shift step, the algorithm might not work as expected.

The algorithm starts by checking if v_o is inside the upper limit defined by $V_{o,ref} + V_{tol}$ and the lower limit defined by $V_{o,ref} - V_{tol}$, i.e., if the output voltage is in steady state.

Then, ϕ is decremented by $\Delta\phi$ once. When this happens, v_o will decrease. After that, ϕ_{int} is decremented by $\Delta\phi_{int}$, causing v_o to rise. After every phase-shift step taken, the algorithm holds on for the period T_w to be over. Phase-shift steps $\Delta\phi$ and $\Delta\phi_{int}$ can each have their own T_w period.

A comparison of v_o with $V_{o,ref}$ is done to check if the converter is in steady state. If $v_o < V_{o,ref} - V_{tol}$, then ϕ_{int} is decremented again. If $v_o > V_{o,ref} - V_{tol} \wedge v_o < V_{o,ref} + V_{tol}$, then the algorithm stores the current phase-shift pair (ϕ and ϕ_{int}) into a variable. The whole process starts again by decrementing ϕ by $\Delta\phi$.

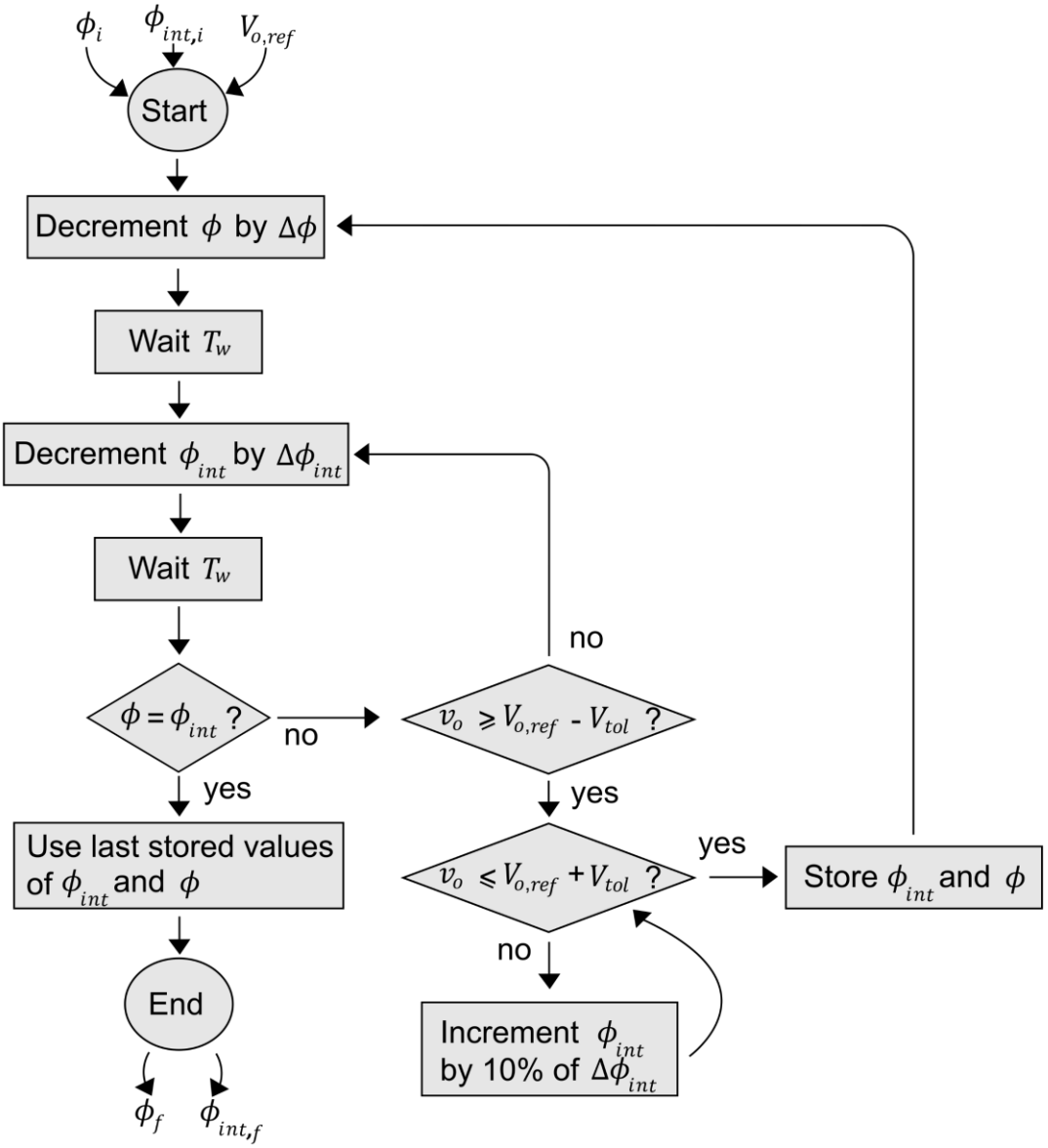
In case the condition $v_o \leq V_{o,ref} + V_{tol}$ is false, ϕ_{int} is incremented by 10% of the phase-shift step value (or a lower percentage), to make sure the output voltage decreases until it is inside the voltage margin defined by $V_{o,ref}$ and V_{tol}. This probably wouldn't happen if $\Delta\phi_{int}$ is small enough, but in case it does, this operation will try to keep the algorithm on track.

When the algorithm has decremented the phase-shift pair values to the point of $\phi = \phi_{int}$, the converter will not achieve $V_{o,ref}$ anymore without leaving the operating region of $\phi < \phi_{int}$. Therefore, the last stored phase-shift pair value is applied to the converter and it is the minimum phase-shift pair value possible for the given $V_{o,ref}$. At this point, the algorithm "ends". The operation described is illustrated in the flowchart of Figure 58.

A couple of points should be taken into consideration when implementing the algorithm:

- A converter with a high output capacitance will require more time for the algorithm to finish, i.e., longer T_w, since the settling time of v_o will be longer. Depending on the converter parameters, it might take a few seconds for it to finish.
- A small phase-shift step guarantees that the converter operation will remain close to $V_{o,ref}$, assuring a more smooth and precise execution of the algorithm. On the other hand, the algorithm will take more time

Figure 58 – Flowchart diagram of the mCSPT algorithm operation.



Source: provided by the author, 2025.

to finish. Noise and other non-idealities might interfere when trying to apply such a small phase-shift.

- This version of the algorithm implemented for the tests does not know the difference between a phase-shift step or a load change, since it only relies on the measurement of the output voltage. If the load changes during the execution of the algorithm, it will not work properly, which can lead to overvoltage or undervoltage, potentially damaging the load. An output current sensor could be used to detect if the load

changes, and some adaption of the algorithm has to be done in order to account for the load change.

- It is important to be aware that, during the execution of the algorithm, either the output voltage or current, or both, will be decreased. If the load is sensitive to big changes of voltage and current, the phase-shift steps should be as low as possible in order to mitigate and prevent any damage on the load during the execution of the algorithm.

Should the algorithm be used in an application where the output voltage is provided by the load (e.g., another converter or a battery), both voltage and current sensors are needed to measure v_o and i_o. The parameter for reference of the algorithm then becomes the output power. In this case, since the output voltage will depend on the load, the output current will suffer changes during the execution of the algorithm.

6.3.2 Simulation

A simulation is done in PLECS to verify the algorithm operation. The converter parameters are the same as the prototype designed in Chapter 4 (see Table 4), except that $L = 590\ \mu H$ and the output capacitance is 9.42 μF. The load is a 722 Ω resistor, resulting in an output power of approximately 200 W.

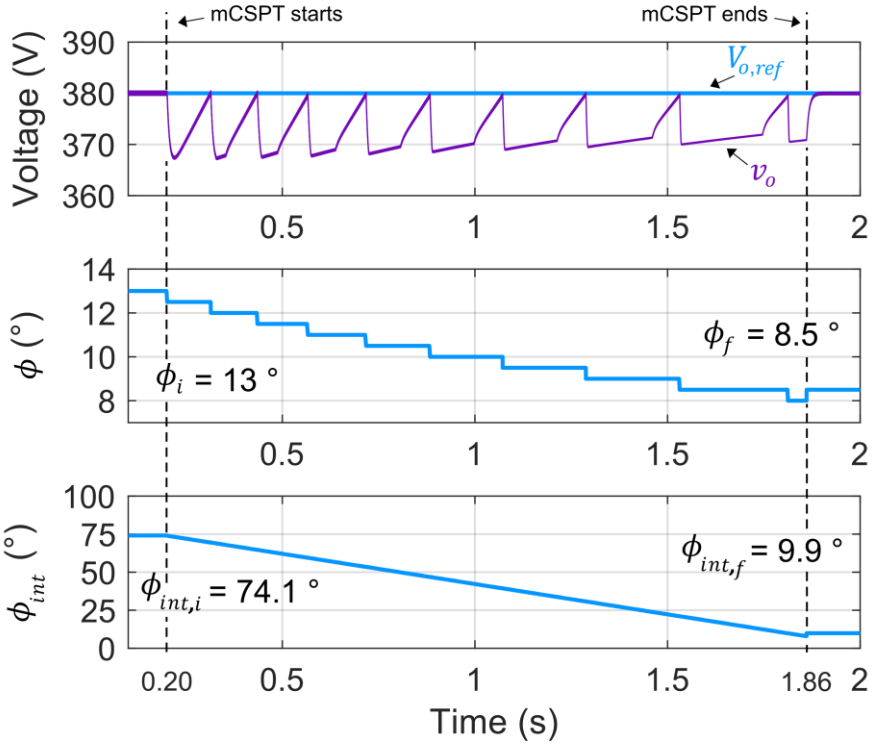
The parameters utilized for the algorithm are: $V_{o,ref} = 380\ V$, $\Delta\phi = 0.5°$, $\Delta\phi_{int} = 0.1°$, $V_{tol} = 0.5\ V$, $T_w = 20T_s$ after $\Delta\phi$ and $T_w = 50T_s$ after $\Delta\phi_{int}$.

Figure 59 presents the plots of v_o, ϕ and ϕ_{int} over time. Before the algorithm starts, the converter is already operating in steady state, with $\phi_i = 13°$ and $\phi_{int,i} = 74.1°$.

The algorithm starts by decreasing ϕ from 13° to 12.5°, which causes v_o to drop from 380 V to around 368 V. After that, ϕ_{int} is decreased in 0.1° steps and v_o starts to increase, until v_o reaches 380 V. When it reaches steady state, the algorithm stores the current phase-shift pair values and the same process starts again: ϕ is decreased by 0.5° once and ϕ_{int} is decreased by 0.1° until v_o reaches $V_{o,ref}$.

This process is repeated until $\phi = \phi_{int} = 8\,°$. Since the converter will not be able to achieve $v_o = 380\,V$ without straying away from the condition of $\phi < \phi_{int}$, the algorithm changes the phase-shift pair to the last values stored in which it achieved $V_{o,ref}$, which are $\phi_f = 8.5\,°$ and $\phi_{int,f} = 9.9\,°$. Thus, ending the algorithm operation. Even though the output capacitance is relatively small, it still takes around 1.7 seconds for the mCSPT to finish.

Figure 59 – Simulation results of mCSPT execution: output and reference voltage (top), external (middle) and internal (bottom) phase-shift.

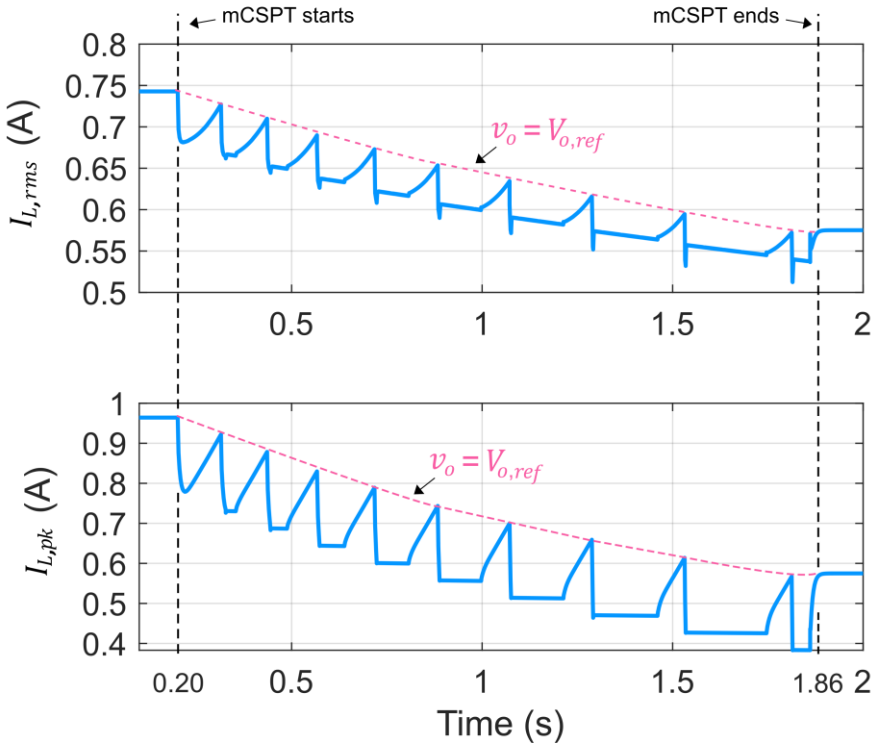


Source: provided by the author, 2025.

Figure 60 shows the values of $I_{L,rms}$ and $I_{L,pk}$ of the converter in the simulation as the algorithm is executed. It can be seen that both parameters are decreased over time (considering the points in the dashed-line curve, which represents all operation points when $v_o = V_{o,ref}$), as a result of using lower phase-shift pair values.

Figure 61 shows the waveform of current i_L before the algorithm starts. The zero-power period is $\Delta T_{zp} = 9\,\mu s$ and the peak and RMS values of the current are $I_{L,pk} = 0.96\,A$ and $I_{L,pk} = 0.74\,A$, respectively.

Figure 60 - Simulation results of mCSPT execution: RMS (top) and peak (bottom) values of transformer current.



Source: provided by the author, 2025.

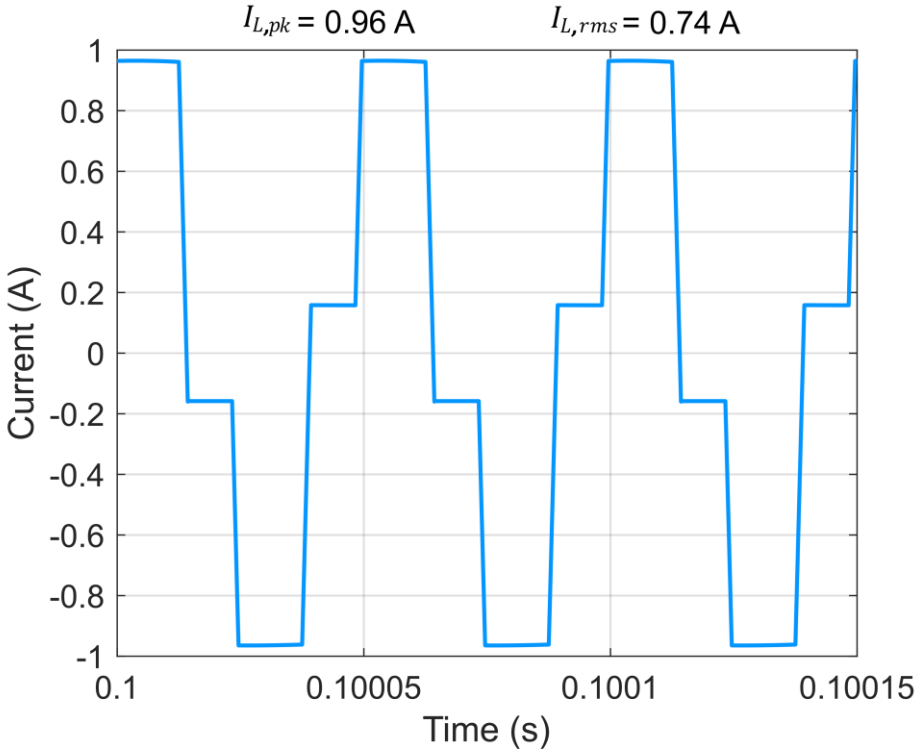
The reason that $I_{zp} \neq 0$ in Figure 61 and Figure 62 is because of some resistances that were added to the circuit for dampening the average value of i_L, which appears every time a phase-shift step is given.

Figure 62 shows the waveform of current i_L after the algorithm ends. The zero-power period is $\Delta T_{zp} = 0.7\ \mu s$ and the peak and RMS values of the current are approximately $I_{L,pk} = 0.57\ A$ and $I_{L,pk} = 0.57\ A$, respectively.

By comparing the results of $I_{L,rms}$ and $I_{L,pk}$ before and after the execution of the algorithm, it is clear that there is a decrease of these parameters. Hence proved the improvement of current stress in the transformer and switches by the algorithm.

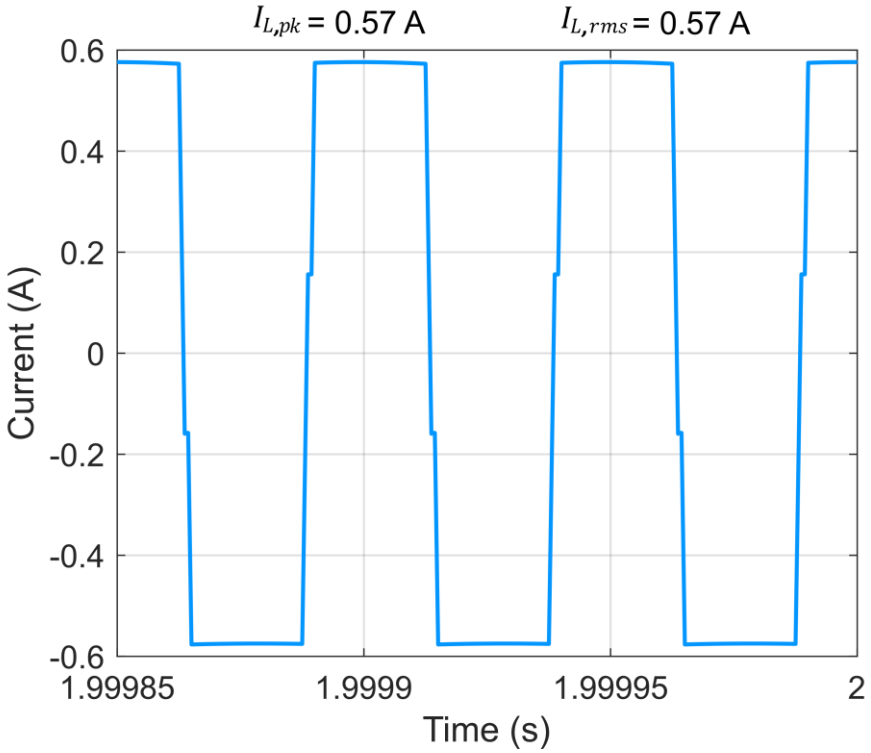
Another observation that can be done by looking at Figure 62 is that, the waveform of i_L practically looks like the current waveform resulted by implementing SPS modulation. This shows that achieving the minimum current stress in DPS modulation comes at the expense of operating in the threshold between SPS and DPS modulations.

Figure 61 - Simulation results of transformer current before mCSPT execution.



Source: provided by the author, 2025.

Figure 62 - Simulation results of transformer current after mCSPT execution.



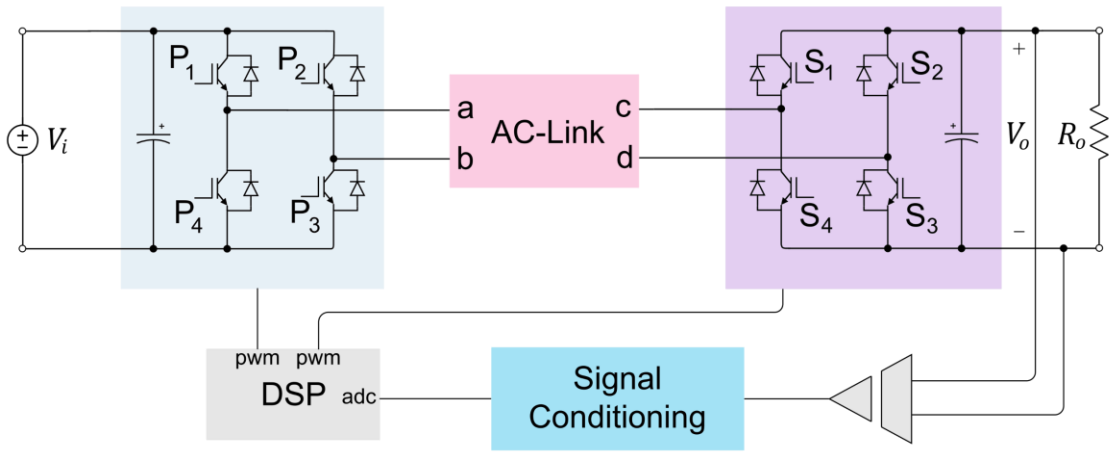
Source: provided by the author, 2025.

6.3.3 Experimental Setup

For practical validation of the algorithm, the prototype designed in Chapter 4 is used. The algorithm is implemented in the DSP. A signal conditioning board is connected between the output of the voltage sensor and the ADC pin of the DSP. A digital low-pass filter of 9th order (500 Hz bandwidth) is implemented, while also averaging its output. The signal conditioning board and the digital filters are needed for eliminating EMI that messes with the voltage measurement by the DSP.

Figure 63 illustrates a diagram of the experimental setup. The design and circuit diagram of the signal conditioning board can be seen in the Appendix D. The code implemented in the DSP can be seen in Appendix E.

Figure 63 – Hardware setup diagram for mCSPT experimental test.



Source: provided by the author, 2025.

The parameters for the mCSPT used for the test are shown in Table 24. The load is a 722 Ω resistor, resulting in an output power of approximately 200 W. A waiting period T_w of 1 second might be rather long comparing to the switching frequency of the converter, but it is chosen for a safer test, avoiding potential damage to the prototype.

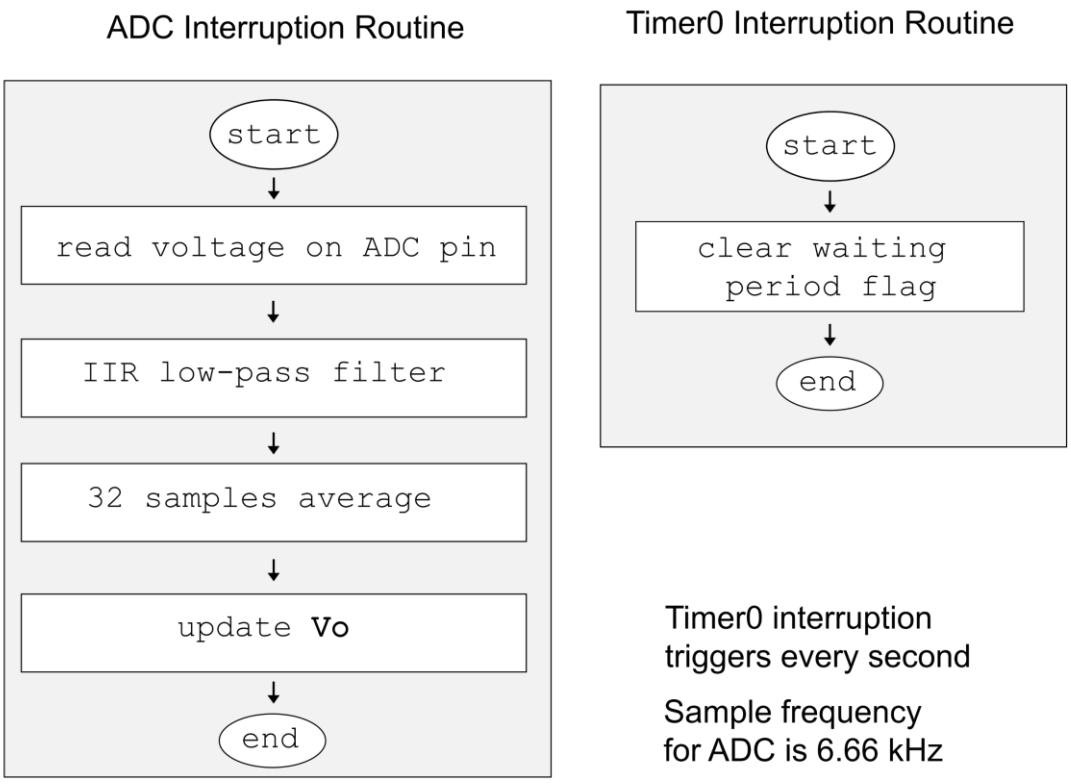
Figure 64 shows a simplified flowchart of the logic implemented for the peripherals used and Figure 65 shows the pseudocode of the simplified logic implemented for the algorithm in the main loop of the DSP.

Table 24 – mCSPT parameters for experimental test.

Parameter	Value
$V_{o,ref}$	380 V
V_{tol}	0.2 V
T_w	1 s
$\Delta\phi$	1°
$\Delta\phi_{int}$	1°
ϕ_i	12°
$\phi_{int,i}$	90°

Source: provided by the author, 2025.

Figure 64 – Flowchart diagram of interruption routines implemented in the DSP for mCSPT testing.



Source: provided by the author, 2025.

Figure 65 – Pseudocode of the mCSPT algorithm implemented in the DSP for experimental test.

```
Main Loop
{
      If mCSPT is activated
            If ϕ equals ϕ_int
                  Use last stored values of ϕ and ϕ_int
                  Finish mCSPT
            End if
            If Vo is between lower and upper limits
                  Converter is in steady-state
            End if
            If five consecutive steady-state readings are done
                  Store values of ϕ and ϕ_int
                  Set flag for Δϕ
            Clear flag for Δϕ_int
            End if
            If Vo is lower than the lower limit
                  Clear flag for Δϕ
                  Set flag for Δϕ_int
            End if
            If Δϕ flag is set and the waiting period is over
                  Decrement ϕ by Δϕ
                  Set flag for waiting period
            End if
            If Δϕ_int flag is set and the waiting period is over
                  Decrement ϕ_int by Δϕ_int
                  Set flag for waiting period
            End if
      End if
      Update PWM phase-shift with ϕ and ϕ_int
}
```

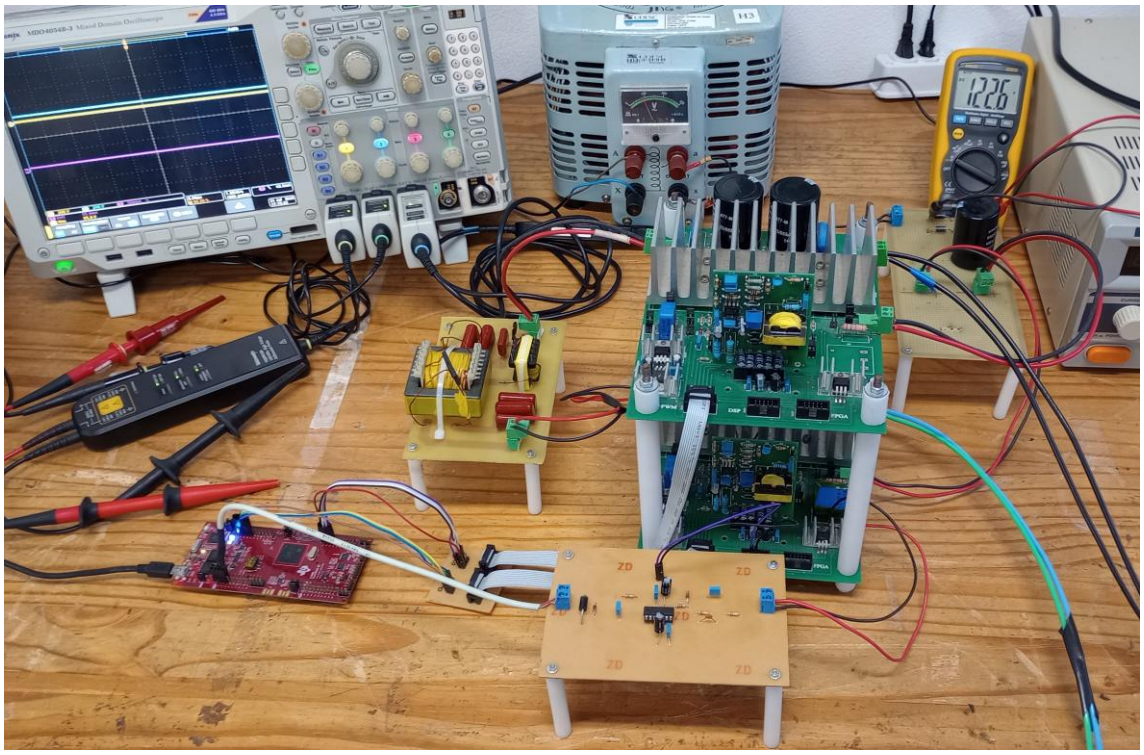
Source: provided by the author, 2025.

The test is conducted in a mix of open-loop and closed-loop control:

1. The initial values of ϕ and ϕ_{int} are manually set. The converter is operating in open-loop and steady-state;
2. The algorithm is manually executed. During this period, the converter operates in closed-loop;
3. After the algorithm finishes, the converter goes back to operate in open-loop with the phase-shift values found by the algorithm.

Figure 66 shows a picture of the workbench with the test setup.

Figure 66 – Picture of hardware setup for experimental test of mCSPT.



Source: provided by Castellain (2024) and the author, 2025.

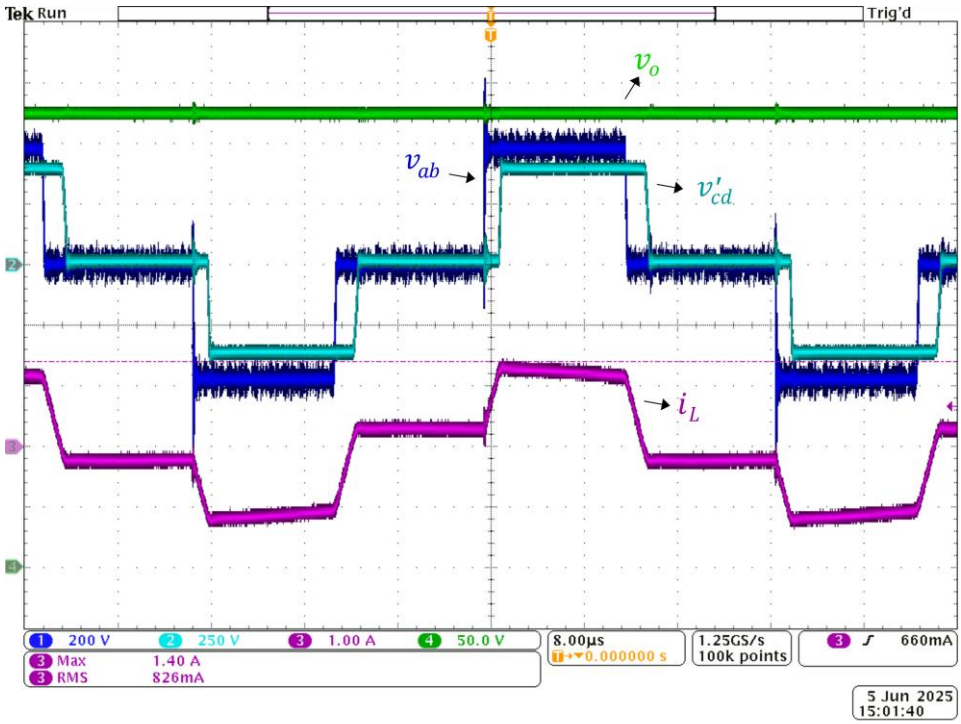
6.3.4 Experimental Results

Figure 67 presents the current and voltages waveform of the converter operating before the algorithm is executed. The voltage v_o is at 380 V. Voltages v_{ab} and v'_{cd} are characterized by the long zero voltage period due to $\phi_{int,i} = 90°$, which in turn results in a long constant current period of i_L.

Figure 68 shows the voltage being measured by the DSP, as seen in the Code Composer Studio software, while the algorithm is executing. The Index axis represent the number of a sample. In this tool, a new sample is plotted each second. It can be seen that the output voltage of the converter behaviors just like the simulation's results seen in Figure 59.

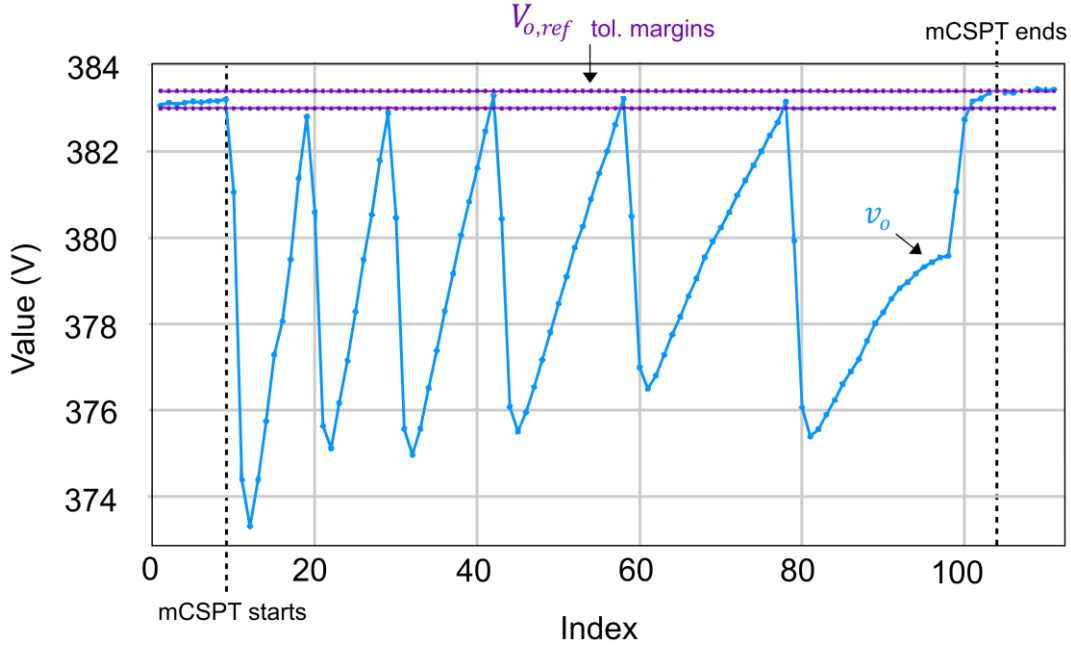
Note that, in Figure 68, the voltage reference is not exactly 380 V. Rather, it is around 383 V. The reason for this is while v_o is constant at 380 V, the output voltage of the sensor slowly increases overtime, probably due to the thermal drift caused by a hot shunt resistor which is placed close to the sensor. A different $V_{o,ref}$ is used in practice to compensate for the thermal drift of the voltage sensor.

Figure 67 – Main experimental voltages and current waveforms of DAB operating before mCSPT execution.



Source: provided by the author, 2025.

Figure 68 – Output voltage measured by the DSP seen in Code Composer Studio software during mCSPT execution.



Source: provided by the author, 2025.

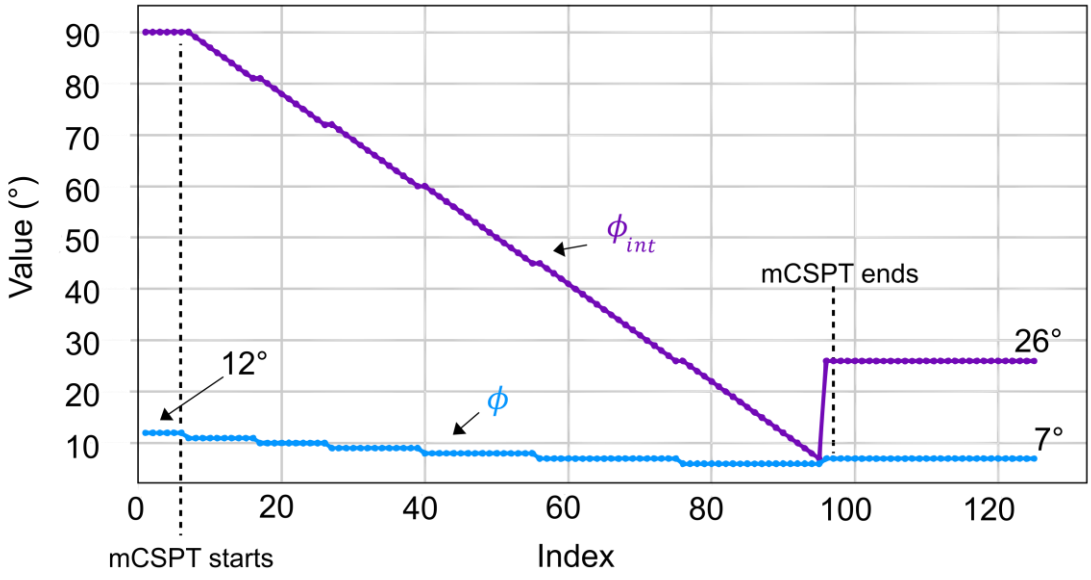
Furthermore, it can be seen that around the Index 20 and 30, the output voltage is still lower than the lower limit for the algorithm. This is likely due to the refresh rate of the Code Composer Studio's graph and the internal clock of the DSP being unsynchronized.

Figure 69 presents the values of ϕ and ϕ_{int} during the execution of the algorithm, also seen by the Code Composer Studio software. The final values of the phase-shift reached by the mCSPT are $\phi_f = 7°$ and $\phi_{int,f} = 26°$.

Figure 70 presents the waveform of v_o during the execution of the algorithm. Although the scale of the oscilloscope makes it difficult to see the exact shape of the curve, it is clear that it follows the same pattern as Figure 59.

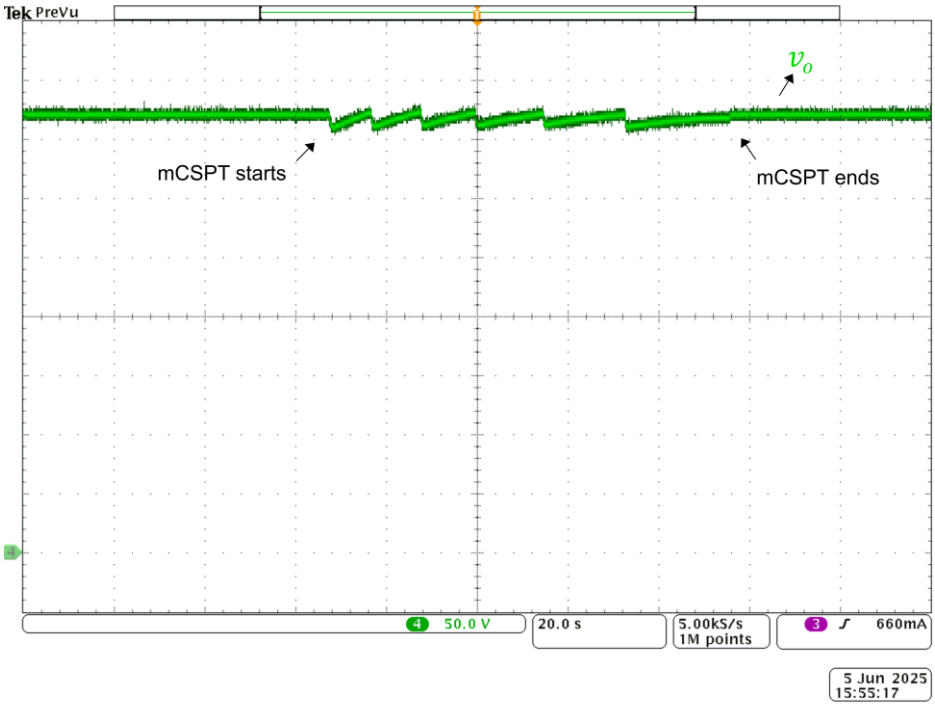
Figure 71 presents the waveforms of v_o, v_{ab}, v'_{cd} and i_L after the algorithm is executed. It is clear that the phase-shift applied to the converter is much lower, reducing drastically the zero-voltage period of voltages v_{ab} and v'_{cd}, while maintaining the same output voltage.

Figure 69 – External (blue) and internal (purple) phase-shifts used by the DSP seen in Code Composer Studio software during mCSPT execution.



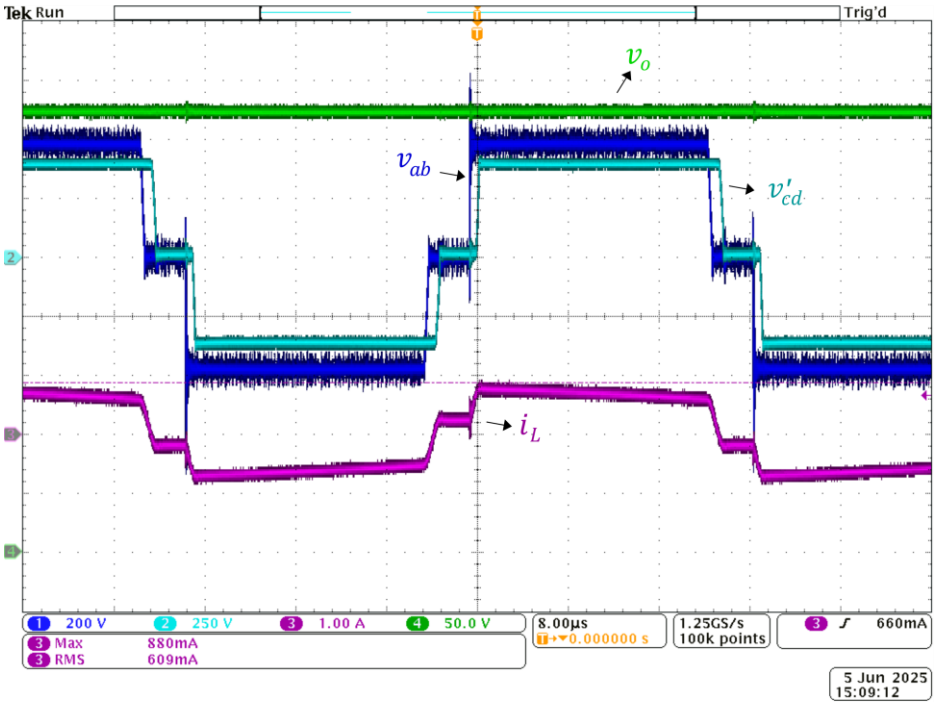
Source: provided by the author, 2025.

Figure 70 – Experimental output voltage waveform of the converter during mCSPT execution.



Source: provided by the author, 2025.

Figure 71 - Main experimental voltages and current waveforms of DAB operating after mCSPT execution.



Source: provided by the author, 2025.

Table 25 presents the parameters $I_{L,rms}$ and $I_{L,pk}$ measured by the oscilloscope before and after the algorithm. Both parameters are reduced as a result of using a lower value for the phase-shift pair, as expected.

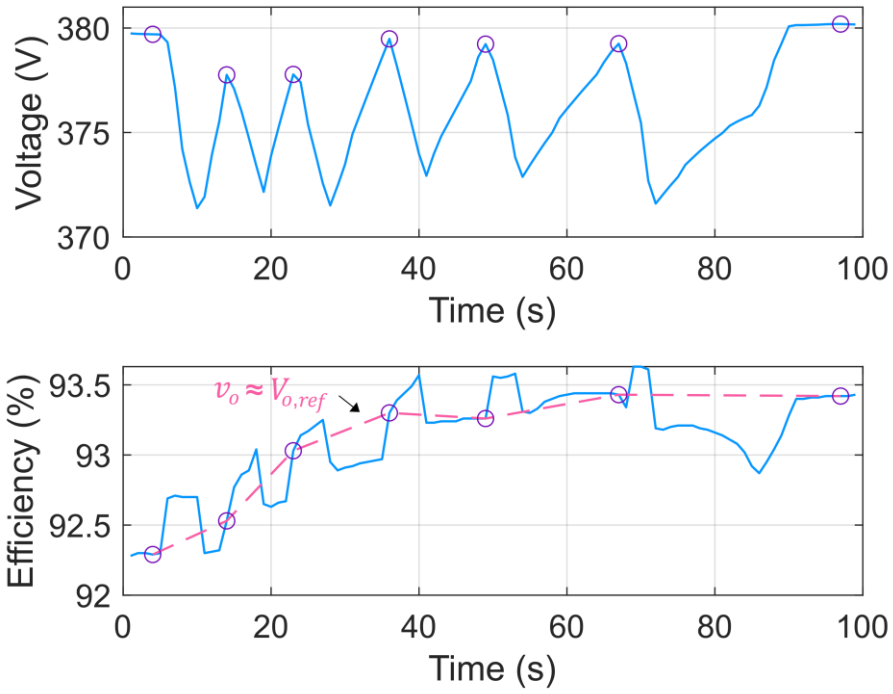
Table 25 – Experimental measurements of RMS and peak values of transformer current before and after mCSPT execution.

Parameter	Before mCSPT	After mCSPT
$I_{L,rms}$	826 mA	609 mA
$I_{L,pk}$	1.40 A	0.88 A

Source: provided by the author, 2025.

Figure 72 presents the voltage v_o and the efficiency of the converter during the execution of the algorithm, measured by the power analyzer in a new test (same initial conditions).

Figure 72 – Experimental measurement by power analyzer of output voltage (top) and efficiency (bottom) of converter during mCSPT execution.



Source: provided by the author, 2025.

The efficiency of the converter before the mCSPT is around 92.2 %. After the mCSPT execution, the efficiency is increased to 93.4%. The pink dashed line shows the tendency of the converter efficiency as the phase-shift pair is lowered. The circles represent the points where the algorithm achieved the voltage reference. Again, there are two points where the voltages are slightly lower than the reference because of no synchronization between the power analyzer and the DSP. The efficiency can still be improved if lower phase-shift steps are utilized.

7 CONCLUSION

In this Master's thesis, a comprehensive literature review and circuit analysis of the Dual Active Bridge converter has been conducted. The scope of the literature review is limited to single-phase, voltage-fed and non-resonant topologies of the converter. It covers a wide range of topics for understanding key characteristics of its operation and design challenges for this power converter in a qualitative manner.

The circuit analysis done considers the DAB converter employing the SPS modulation, which is the simplest one, during steady-state. A step-by-step analysis of the topological states is shown, along with voltages and currents waveforms. Following it is a mathematical analysis for deriving equations of many important parameters of the converter, such as power transmission, transformer current, apparent power of transformer, semiconductor current stresses and soft-switching, with figures showing plots for visualizing the behavior of the parameters as a function of the phase-shift. The equations presented are paramount for designing any DAB converter.

A prototype of 600 W and 380 V with unity gain was designed and built for experimental tests. The measurements obtained of the converter operating with SPS modulation matches the theoretical analysis done, validating the equations and the circuit analysis. The efficiency estimated using the derived equations is close to the measurement done by a power analyzer, with a maximum difference of 2.64%.

Furthermore, a brief description of the DPS modulation and an investigation of its impact on the transformer current is done, limited to the condition that the external phase-shift is lower than the internal phase-shift, where there is a period in which there is no active power being transferred. It is shown with simulation results that the magnitude of the current during this period can be decreased, but only if the RMS and peak value of the transformer current are increased. However, by increasing the current of this period, the overall current stress in the converter is reduced. This happens when the phase-shift pair value is the lowest possible.

For the purpose of achieving this current stress reduction, an algorithm named “minimum Current Stress Point Tracking” is proposed. The mCSPT automatically finds the lowest phase-shift pair possible for a given power reference, without the need to implement complex equations that results from the circuit analysis of DSP modulation and measurement of components’ parameters.

Both simulated and experimental results of the mCSPT operation are presented, validating the minimization of the current stress when the converter is using DPS modulation. Moreover, measurements confirm an increase of the converter efficiency after the mCSPT is executed, in which even greater efficiency could be achieved by fine tuning the parameters of the algorithm.

The implemented version of the mCSPT in this Master’s thesis was for test and validation only. For implementing this algorithm in a real product, further developments must be done to ensure that it is executed properly. Future work/improvements that can be proposed for the mCSPT algorithm are:

- Add an output current sensor or an estimator (that does not require a sensor) so that the algorithm can detect if the load changes during its execution and stop, waiting until the main controller compensates for the new load;
- Find a way to automatically set the period T_w without relying on trial-and-error for any given output capacitance. Make the algorithm capable of self-configure in any converter that it is applied on;
- By modifying the switching frequency of the converter, more combinations of the control variables are possible, which may yield even lower values of $I_{L,rms}$ and $I_{L,pk}$ than fixed switching frequency operation. An investigation can be done to see if a variable switching frequency is practicable to implement in the algorithm;
- Analyze impacts of the algorithm on soft-switching operation;
- Expand the functionality of the algorithm to other conditions, such as $\phi > \phi_{int}$;
- Evaluate the possibility to apply the algorithm on other modulations, such as EPS and TPS;

- Store all of the phase-shift pair values found during the “track” and create different modes for the algorithm, e.g., use the phase-shift pair which results in the highest ΔT_{zp};
- Stability analysis of the converter with the algorithm;
- Impacts and mitigation of load changes during the execution of the algorithm;
- Impacts and possible improvements on filtering design for the execution of the algorithm.

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APPENDIX A – FURTHER MATHEMATICAL ANALYSIS OF SPS MODULATION

In this Appendix, more mathematical analysis is presented for the DAB converter operating with SPS modulation.

Section A.1 presents an analysis of the input apparent and non-active power of the converter. Sections A.2 and A.3 presents big equations derived from Chapter 3, shown here for better readability. These equations can aid in the task of designing the converter.

A.1 INPUT APPARENT AND NON-ACTIVE POWER

The input apparent power S_i is given by equation (A.1), which is the apparent power seen by the input voltage source. In practice, it is the apparent power seen after the input capacitor C_i (see Figure 1).

$$S_i = V_i I_{i,rms} = V_i I_{L,rms} \tag{A.1}$$

Substituting equation (A.1) in (3.37) results in the expression (A.2).

$$S_i = \frac{V_i}{2Lf_s}\sqrt{-\frac{2}{3}V_i V_o'\left(\frac{|\phi|}{\pi}\right)^3 + V_i V_o'\left(\frac{|\phi|}{\pi}\right)^2 + \left(\frac{V_i^2}{12} - \frac{V_i V_o'}{6} + \frac{{V_o'}^2}{12}\right)} \tag{A.2}$$

S_i can also be normalized by defining an apparent power base value $S_{i,b}$ as in equation (A.3). The normalized input apparent power $\overline{S_i}$ is given by equation (A.4) as a function of ϕ and K.

$$S_{i,b} = \frac{V_i^2}{4Lf_s} \tag{A.3}$$

$$\overline{S_i} = \frac{S_i}{S_{i,b}} = \sqrt{\frac{1}{3}\left[-8K\left(\frac{|\phi|}{\pi}\right)^3 + 12K\left(\frac{|\phi|}{\pi}\right)^2 + (1-K)^2\right]} \tag{A.4}$$

It can be seen in equation (3.21) and (A.4) that $\overline{S_i} = \overline{I_L}$. Therefore, the plots shown in section 3.3.2 describing the behavior of $\overline{I_L}$ also applies to $\overline{S_i}$, with the only difference being the base value $S_{i,b}$.

The output apparent power S_o seen by the output capacitor C_o (see Figure 1) is defined in expression (A.5). Substituting equation (3.26) in (A.5) results in equation (A.6)

$$S_o = V_o I_{o,rms} \tag{A.5}$$

$$S_o = \frac{nV_o}{2Lf_s}\sqrt{-\frac{2}{3}V_i V_o'\left(\frac{|\phi|}{\pi}\right)^3 + V_i V_o'\left(\frac{|\phi|}{\pi}\right)^2 + \left(\frac{V_i^2}{12} - \frac{V_i V_o'}{6} + \frac{{V_o'}^2}{12}\right)} \tag{A.6}$$

The definition of non-active power N is shown in equation (A.7), which includes the reactive power Q and the harmonic distortion power D.

$$N = \sqrt{S^2 - P^2} = \sqrt{Q^2 + D^2} \tag{A.7}$$

Substituting equations (3.10) and (A.2) in (A.7), the expression for the input source non-active power N_i presented in (A.8) can be deduced.

$$N_i = \frac{V_i}{2Lf_s}\left\{\frac{1}{12}\left[-12{V_o'}^2\left(\frac{|\phi|}{\pi}\right)^4 + \left(24{V_o'}^2 - 8V_i V_o'\right)\left(\frac{|\phi|}{\pi}\right)^3 + 12\left(V_i V_o' - {V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + (V_i - V_o')^2\right]\right\}^{1/2} \tag{A.8}$$

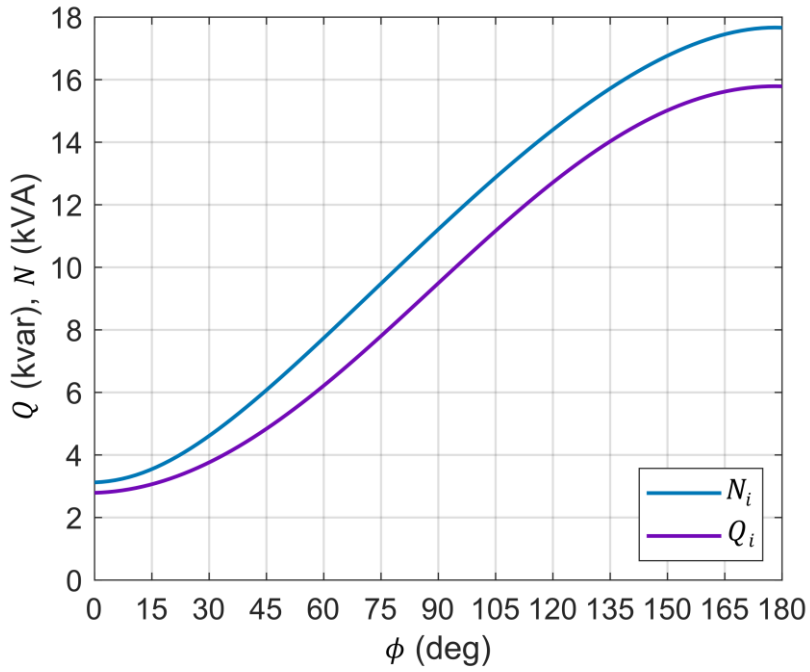
The output non-active power can be derived the same way but using S_o instead of S_i in equation (A.7).

Schibli (2000) derives the expression for the reactive power of the converter seen by the input capacitor as equation (A.9). However, this analysis only considers the fundamental component of the voltage applied to the inductor ($v_{ab}(t)$), as opposed to equation (A.8), which considers all harmonic components.

$$Q_i = \frac{\left(\frac{2\sqrt{2}}{\pi} V_i\right)^2 - \left(\frac{2\sqrt{2}}{\pi}\right)^2 V_i n V_o \cos(\phi)}{2\pi f_s L} \quad \text{(A.9)}$$

Figure 73 shows the powers Q_i and N_i plotted as function of ϕ. It can be seen that there is a small difference between the two curves, which is expected. Although equation (A.9) is simpler, equation (A.8) should be used if more accuracy is needed.

Figure 73 – Plot of Q_i and N_i versus ϕ for $K = 0.7$. Parameters of the converter are: $V_i = 100\ V, n = 1, L = 13.88\ \mu H$ and $f_s = 10\ kHz$.



Source: provided by the author, 2024.

The expressions presented are valid for all modes of operation, regardless of power flow direction.

A.2 SEMICONDUCTORS CURRENT STRESS

Solving the equations for the average and RMS current in the semiconductors shown in section 3.3.6, the following expressions are derived for $\phi > 0$:

$$I_P = \frac{1}{32Lf_s}\frac{1}{(V_i + V_o')}\left[\left(-8V_iV_o' - 4{V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(12V_iV_o' + 4{V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \tag{A.10}$$

$$I_{P,rms} = \frac{1}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i + V_o')}\left[\left(-16V_i^2V_o' - 16V_i{V_o'}^2 - 8{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right)^3 + \left(24V_i^2V_o' + 12V_i{V_o'}^2 + 12{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(-6V_i^2V_o' + 12V_i{V_o'}^2 - 6{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right) + \left(V_i^3 + V_i^2V_o' - 5V_i{V_o'}^2 + 3{V_o'}^3\right)\right]\right\}^{1/2} \tag{A.11}$$

$$I_{DP} = \frac{1}{32Lf_s}\frac{\left[V_i + V_o'\left(2\frac{|\phi|}{\pi} - 1\right)\right]^2}{(V_i + V_o')} \tag{A.12}$$

$$I_{DP,rms} = \frac{V_i + V_o'\left(2\frac{|\phi|}{\pi} - 1\right)}{8Lf_s}\sqrt{\frac{1}{3}\frac{\left[V_i + V_o'\left(2\frac{|\phi|}{\pi} - 1\right)\right]}{(V_i + V_o')}} \tag{A.13}$$

$$I_S = \frac{n}{32Lf_s}\frac{1}{(V_i + V_o')}\left[4V_i^2\left(\frac{|\phi|}{\pi}\right)^2 + \left(-4V_i^2 + 4V_iV_o'\right)\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \tag{A.14}$$

$$I_{S,rms} = \frac{n}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i + V_o')}\left[(8V_i^3)\left(\frac{|\phi|}{\pi}\right)^3 + \left(-12V_i^3 + 12V_i^2V_o'\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(6V_i^3 - 12V_i^2V_o' + 6V_i{V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(-V_i^3 + 3V_i^2V_o' - 3V_i{V_o'}^2 + {V_o'}^3\right)\right]\right\}^{1/2} \tag{A.15}$$

$$I_{DS} = \frac{n}{32Lf_s}\frac{1}{(V_i + V_o')}\left[(-4V_i^2 - 8V_iV_o')\left(\frac{|\phi|}{\pi}\right)^2 + (4V_i^2 + 12V_iV_o')\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \tag{A.16}$$

$$I_{DS,rms} = \frac{n}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i + V_o')}\left[\left(-8V_i^3 - 16V_i^2V_o' - 16V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^3 + \left(12V_i^3 + 12V_i^2V_o' + 24V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(-6V_i^3 + 12V_i^2V_o' - 6V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(3V_i^3 - 5V_i^2V_o' + V_iV_o'^2 + V_o'^3\right)\right]\right\}^{1/2} \tag{A.17}$$

These expressions are valid for the case shown in section 3.3.6, which requires the conditions $\phi > 0$, $i_L(0) < 0$ and $i_L(t_1) > 0$ to be met.

Since the converter has a symmetric operation, the derived equations can be interchanged between components if the power flow becomes negative (i.e., $\phi < 0$). Table 26 shows which expressions should be used in this case, as long as $i_L(0) < 0$ and $i_L(t_1) > 0$.

Table 26 – Semiconductors current stresses for negative power flow operation.

Device	Equivalent Expression	
	Average Value	RMS Value
Primary Side Switch	(A.12)	(A.13)
Primary Side Diode	(A.10)	(A.11)
Secondary Side Switch	(A.16)	(A.17)
Secondary Side Diode	(A.14)	(A.15)

Source: provided by the author, 2024.

For the case when $\phi > 0$, $i_L(0) < 0$ and $i_L(t_1) < 0$, equations (A.18) through (A.25) can be used for calculating the current stress in the semiconductors.

$$I_P = \frac{1}{32Lf_s}\frac{1}{(V_i - V_o')}\left[4{V_o'}^2\left(\frac{|\phi|}{\pi}\right)^2 + \left(4V_iV_o' - 4{V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \quad \text{(A.18)}$$

$$\begin{aligned} I_{P,rms} = \frac{1}{8Lf_s}\Bigg\{\frac{1}{3}\frac{1}{(V_i - V_o')}\Bigg[&8{V_o'}^3\left(\frac{|\phi|}{\pi}\right)^3 + \left(12V_i{V_o'}^2 - 12{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right)^2 \\ &+ \left(6V_i^2V_o' - 12V_i{V_o'}^2 + 6{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right) \\ &+ \left(V_i^3 - 3V_i^2V_o' + 3V_i{V_o'}^2 - {V_o'}^3\right)\Bigg]\Bigg\}^{1/2} \end{aligned} \quad \text{(A.19)}$$

$$\begin{aligned} I_{DP} = \frac{1}{32Lf_s}\frac{1}{(V_i - V_o')}\Bigg[&\left(8V_iV_o' - 4{V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(-4V_iV_o' + 4{V_o'}^2\right)\left(\frac{|\phi|}{\pi}\right) \\ &+ (V_i - V_o')^2\Bigg] \end{aligned} \quad \text{(A.20)}$$

$$\begin{aligned} I_{DP,rms} = \frac{1}{8Lf_s}\Bigg\{\frac{1}{3}\frac{1}{(V_i - V_o')}\Bigg[&\left(-16V_i^2V_o' + 16V_i{V_o'}^2 - 8{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right)^3 \\ &+ \left(24V_i^2V_o' - 36V_i{V_o'}^2 + 12{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right)^2 \\ &+ \left(-6V_i^2V_o' + 12V_i{V_o'}^2 - 6{V_o'}^3\right)\left(\frac{|\phi|}{\pi}\right) \\ &+ \left(V_i^3 - 3V_i^2V_o' + 3V_i{V_o'}^2 - {V_o'}^3\right)\Bigg]\Bigg\}^{1/2} \end{aligned} \quad \text{(A.21)}$$

$$I_S = \frac{n}{32Lf_s}\frac{1}{(V_i - V_o')}\left[4V_i^2\left(\frac{|\phi|}{\pi}\right)^2 + \left(-4V_i^2 + 4V_iV_o'\right)\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \quad \text{(A.22)}$$

$$I_{S,rms} = \frac{n}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i - V_o')}\left[(-8V_i^3)\left(\frac{|\phi|}{\pi}\right)^3 + (12V_i^3 - 12V_i^2V_o')\left(\frac{|\phi|}{\pi}\right)^2 + \left(-6V_i^3 + 12V_i^2V_o' - 6V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(V_i^3 - 3V_i^2V_o' + 3V_iV_o'^2 - V_o'^3\right)\right]\right\}^{1/2} \quad \text{(A.23)}$$

$$I_{DS} = \frac{n}{32Lf_s}\frac{1}{(V_i - V_o')}\left[(-4V_i^2 + 8V_iV_o')\left(\frac{|\phi|}{\pi}\right)^2 + (4V_i^2 - 4V_iV_o')\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \quad \text{(A.24)}$$

$$I_{DS,rms} = \frac{n}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i - V_o')}\left[\left(8V_i^3 - 16V_i^2V_o' + 16V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^3 + \left(-12V_i^3 + 36V_i^2V_o' - 24V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(6V_i^3 - 12V_i^2V_o' + 6V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(V_i^3 - 3V_i^2V_o' + 3V_iV_o'^2 - V_o'^3\right)\right]\right\}^{1/2} \quad \text{(A.25)}$$

When $\phi < 0$, the equations can be interchanged using the same logic of Table 26.

Finally, for the case when $\phi > 0$, $i_L(0) > 0$ and $i_L(t_1) > 0$, equations (A.26) through (A.33) can be used for calculating the current stress in the semiconductors.

$$I_P = \frac{1}{32Lf_s}\frac{1}{(V_i - V_o')}\left[\left(-8V_iV_o' + 4V_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(4V_iV_o' - 4V_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \quad \text{(A.26)}$$

$$I_{P,rms} = \frac{1}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i - V_o')}\left[\left(-16V_i^2V_o' + 16V_iV_o'^2 - 8V_o'^3\right)\left(\frac{|\phi|}{\pi}\right)^3 + \left(24V_i^2V_o' - 36V_iV_o'^2 + 12V_o'^3\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(-6V_i^2V_o' + 12V_iV_o'^2 - 6V_o'^3\right)\left(\frac{|\phi|}{\pi}\right) + \left(V_i^3 - 3V_i^2V_o' + 3V_iV_o'^2 - V_o'^3\right)\right]\right\}^{1/2} \quad \text{(A.27)}$$

$$I_{DP} = \frac{1}{32Lf_s}\frac{1}{(V_i - V_o')}\left[4V_o'^2\left(\frac{|\phi|}{\pi}\right)^2 + \left(4V_iV_o' - 4V_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + (V_i - V_o')^2\right] \quad \text{(A.28)}$$

$$I_{DP,rms} = \frac{V_i + V_o'\left(2\frac{|\phi|}{\pi} - 1\right)}{8Lf_s}\sqrt{\frac{1}{3}\frac{\left[V_i + V_o'\left(2\frac{|\phi|}{\pi} - 1\right)\right]}{(V_i - V_o')}} \quad \text{(A.29)}$$

$$I_S = \frac{n}{32Lf_s}\frac{1}{(V_i - V_o')}\left[(4V_i^2 - 8V_iV_o')\left(\frac{|\phi|}{\pi}\right)^2 + (-4V_i^2 + 4V_iV_o')\left(\frac{|\phi|}{\pi}\right) - (V_i - V_o')^2\right] \quad \text{(A.30)}$$

$$I_{S,rms} = \frac{n}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i - V_o')}\left[\left(8V_i^3 - 16V_i^2V_o' + 16V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^3 + \left(-12V_i^3 + 36V_i^2V_o' - 24V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(6V_i^3 - 12V_i^2V_o' + 6V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(V_i^3 - 3V_i^2V_o' + 3V_iV_o'^2 - V_o'^3\right)\right]\right\}^{1/2} \quad \text{(A.31)}$$

$$I_{DS} = \frac{n}{32Lf_s}\frac{1}{(V_i - V_o')}\left[(-4V_i^2)\left(\frac{|\phi|}{\pi}\right)^2 + (4V_i^2 - 4V_iV_o')\left(\frac{|\phi|}{\pi}\right) - (V_i - V_o')^2\right] \quad \text{(A.32)}$$

$$I_{DS,rms} = \frac{n}{8Lf_s}\left\{\frac{1}{3}\frac{1}{(V_i - V_o')}\left[(-8V_i^3)\left(\frac{|\phi|}{\pi}\right)^3 + (12V_i^3 - 12V_i^2V_o')\left(\frac{|\phi|}{\pi}\right)^2 + \left(-6V_i^3 + 12V_i^2V_o' - 6V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(V_i^3 - 3V_i^2V_o' + 3V_iV_o'^2 - V_o'^3\right)\right]\right\}^{1/2} \quad \text{(A.33)}$$

When $\phi < 0$, the equations can be interchanged using the same logic of Table 26.

A.3 OUTPUT CAPACITOR

In section 3.3.7, solving equation (3.71) for C_o can lead to the expression (A.34) for computation of the output capacitance for the desired ΔV_o.

$$C_o = \frac{1}{\Delta V_o}\frac{n}{32Lf_s^2\left(V_i^2 - V_o'^2\right)}\left[-8V_i^3\left(\frac{|\phi|}{\pi}\right)^4 + (16V_i^3 - 16V_i^2V_o')\left(\frac{|\phi|}{\pi}\right)^3 + \left(-16V_i^3 + 24V_i^2V_o' - 8V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right)^2 + \left(8V_i^3 - 16V_i^2V_o' + 8V_iV_o'^2\right)\left(\frac{|\phi|}{\pi}\right) + \left(-2V_i^3 + 4V_i^2V_o' - 2V_iV_o'^2\right)\right] \quad \text{(A.34)}$$

This expression is valid for the case shown in section 3.3.7, which is operating in buck mode ($V_i > nV_o$) and under the conditions $i_L(0) < 0$, $i_L(t_1) > 0$ and $\phi > 0$.

For voltage match mode, equation (A.35) can be used.

$$C_o = \frac{1}{\Delta V_o}\frac{n}{32Lf_s^2(V_i + V_o')}\left[-4V_i^2\left(\frac{|\phi|}{\pi}\right)^4 + 16V_i^2\left(\frac{|\phi|}{\pi}\right)^3 + (-24V_i^2 + 4V_iV_o')\left(\frac{|\phi|}{\pi}\right)^2 + (8V_i^2 - 8V_iV_o')\left(\frac{|\phi|}{\pi}\right) + \left(-V_i^2 + 2V_iV_o' - V_o'^2\right)\right] \quad \text{(A.35)}$$

The RMS value of the current in the capacitor C_o can be calculated with equation (A.36), derived from equation (3.72).

$$I_{C_o,rms} = \frac{n}{4Lf_s}\left[\frac{1}{3}\left(-12V_i^2\left(\frac{|\phi|}{\pi}\right)^4 + (24V_i^2 - 8V_iV_o')\left(\frac{|\phi|}{\pi}\right)^3 + (-12V_i^2 + 12V_iV_o')\left(\frac{|\phi|}{\pi}\right)^2 + \left(V_i^2 - 2V_iV_o' + V_o'^2\right)\right)\right]^{1/2} \quad \text{(A.36)}$$

This expression is valid for any case as long as $\phi > 0$.

APPENDIX B – EQUIPMENT FOR EXPERIMENTAL TESTS

Table 27 resumes the equipment used for the experimental tests of the prototype done in this Master's thesis.

Table 27 – Equipment used for the experimental tests.

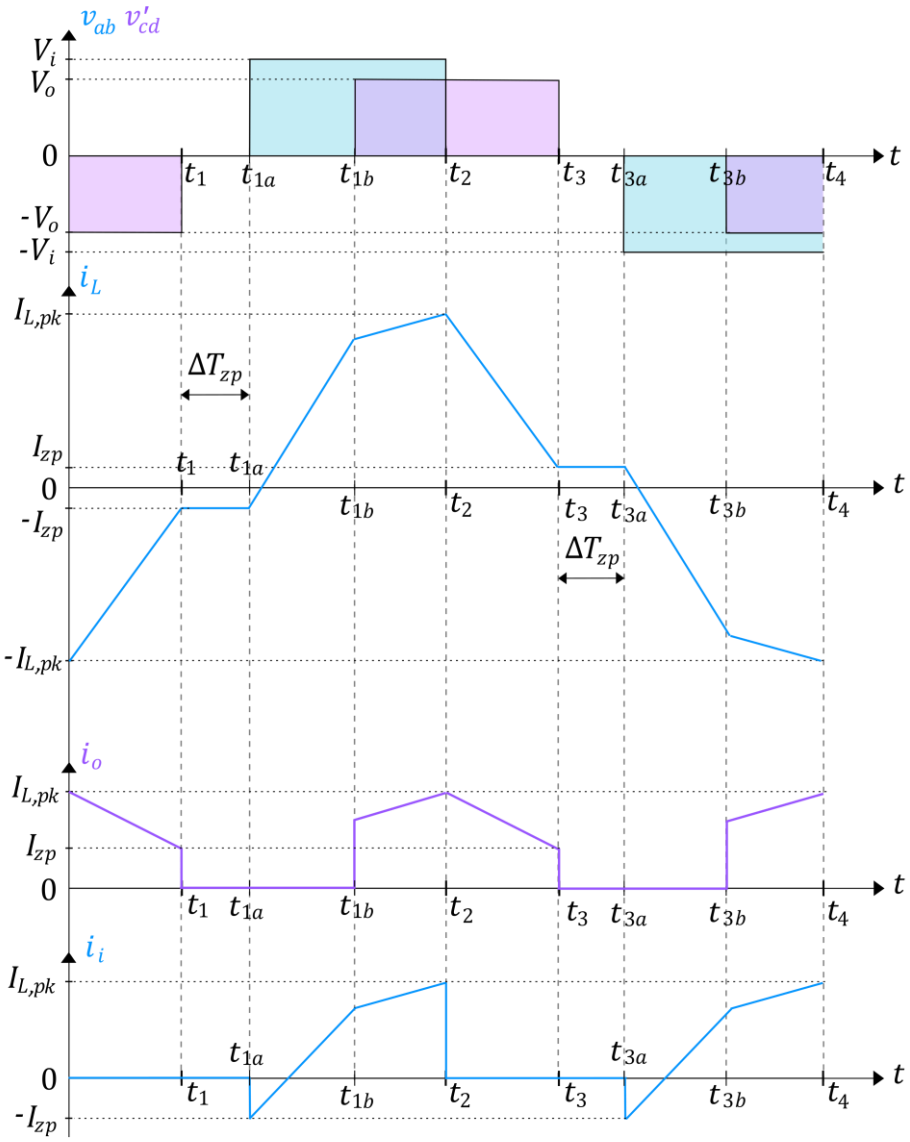
Equipment	Purpose	Manufacturer	Model
Variable AC Voltage Source	Auxiliary Power Supply	JNG	TDGC2 - 5 kVA
Multimeter	DC Voltage Measurement	Hikari	HM-2200
Oscilloscope	Waveform Acquisition	Tektronix	MDO4054B-3
Differential Voltage Probe	Waveform Acquisition	Tektronix	THDP0100
Current Probe	Waveform Acquisition	Tektronix	TCP2020
Power Analyzer	Efficiency Measurement	Tektronix	PA4000
LCR Meter	Impedance Measurement	Politerm	MS5308
6x122 Ω 1 kW Resistor Bank	Load	Eletele	x
DC Voltage Source	Input Voltage Source	Magna-Power	TSD1000-25/380+HS

Source: provided by the author, 2025.

APPENDIX C – MORE WAVEFORMS OF DPS MODULATION INVESTIGATION

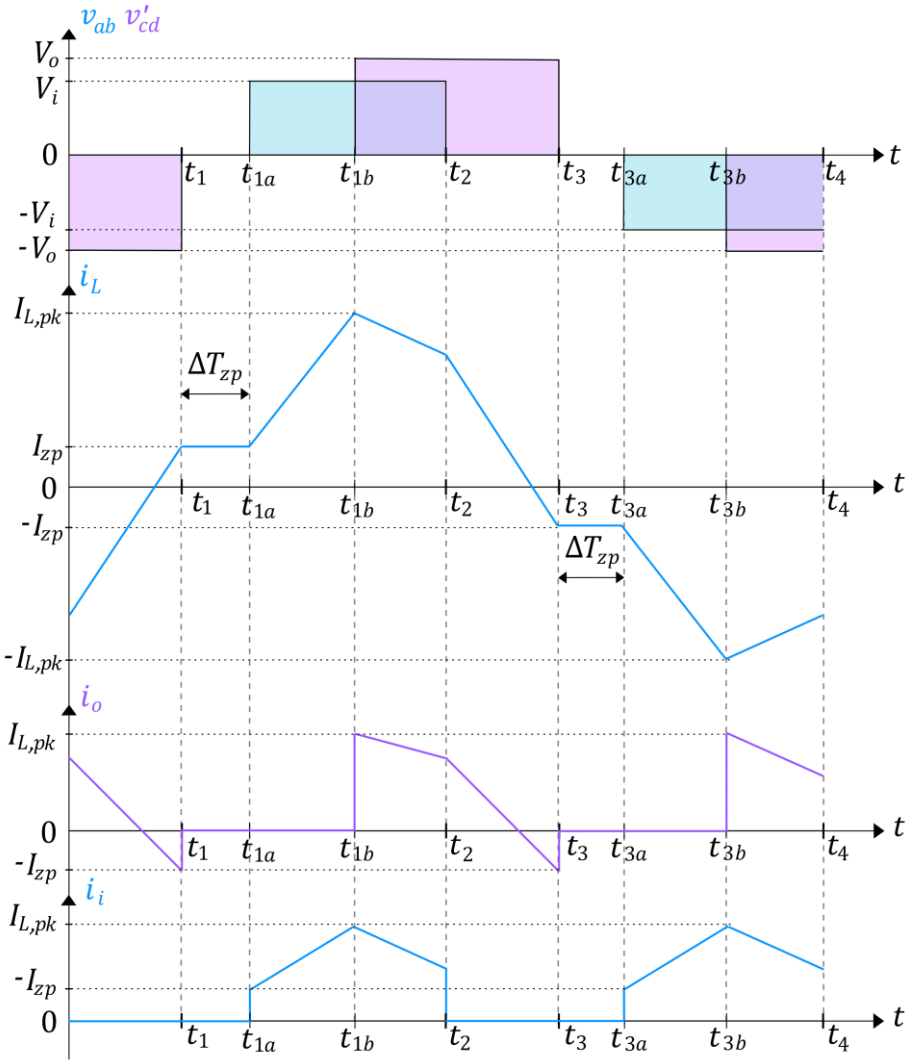
Figure 74 and Figure 75 shows the input and output current for the case of $\phi < \phi_{int}$ for buck mode and boost mode, respectively, during no active power transfer period, showing that no power flows through the input source or the load when both v_{ab} and v_{cd} are zero.

Figure 74 – DPS modulation waveforms for $\phi < \phi_{int}$ during buck mode operation with input and output currents.



Source: provided by the author, 2025.

Figure 75 - DPS modulation waveforms for $\phi < \phi_{int}$ during boost mode operation with input and output currents.



Source: provided by the author, 2025.

APPENDIX D – SIGNAL CONDITIONING BOARD DESIGN METHODOLOGY

The signal conditioning board is composed of a 3rd order low-pass active filter, a buffer and diodes for protection of the DSP in case of overvoltage or undervoltage.

When the converter reaches the nominal output voltage, the maximum voltage supplied by the voltage sensor can be calculated with equation (D.1):

$$M = \frac{V_o}{R_1} \cdot \frac{N_p}{N_s} \cdot R_2 = \frac{380}{56 \times 10^3} \cdot \frac{2500}{1000} \cdot 150 = 2.54\,V \quad \text{(D.1)}$$

Where N_p and N_s are provided by the datasheet of the component (LEM). The maximum voltage provided by the sensor is lower than 3.3 V, which is the maximum voltage allowed by the pins of the DSP. Therefore, it is safe to be connected directly to the DSP without any attenuation gain.

The design methodology of the filters follows the same as De Oliveira (2022). The 3rd order low-pass active filter is composed of two filters designed separately. The first is a 2nd order low-pass active filter with a cut frequency (f_c) of 2 kHz and damp coefficient (ξ) of 0.707. Selecting C_1 as equation (D.2), C_2 can be calculated using equation (D.3). The resistor R can the be calculated using equation (D.4).

$$C_1 = 1\,nF \quad \text{(D.2)}$$

$$C_2 = \xi^2 \cdot C_1 = 0.707^2 \cdot 1 \times 10^{-9} \approx 470\,pF \quad \text{(D.3)}$$

$$R = \frac{1}{2\pi \cdot f_c \cdot \sqrt{C_1 \cdot C_2}} = \frac{1}{2\pi \cdot 2000 \cdot \sqrt{1 \times 10^{-9} \cdot 470 \times 10^{-12}}} \approx 120\,k\Omega \quad \text{(D.4)}$$

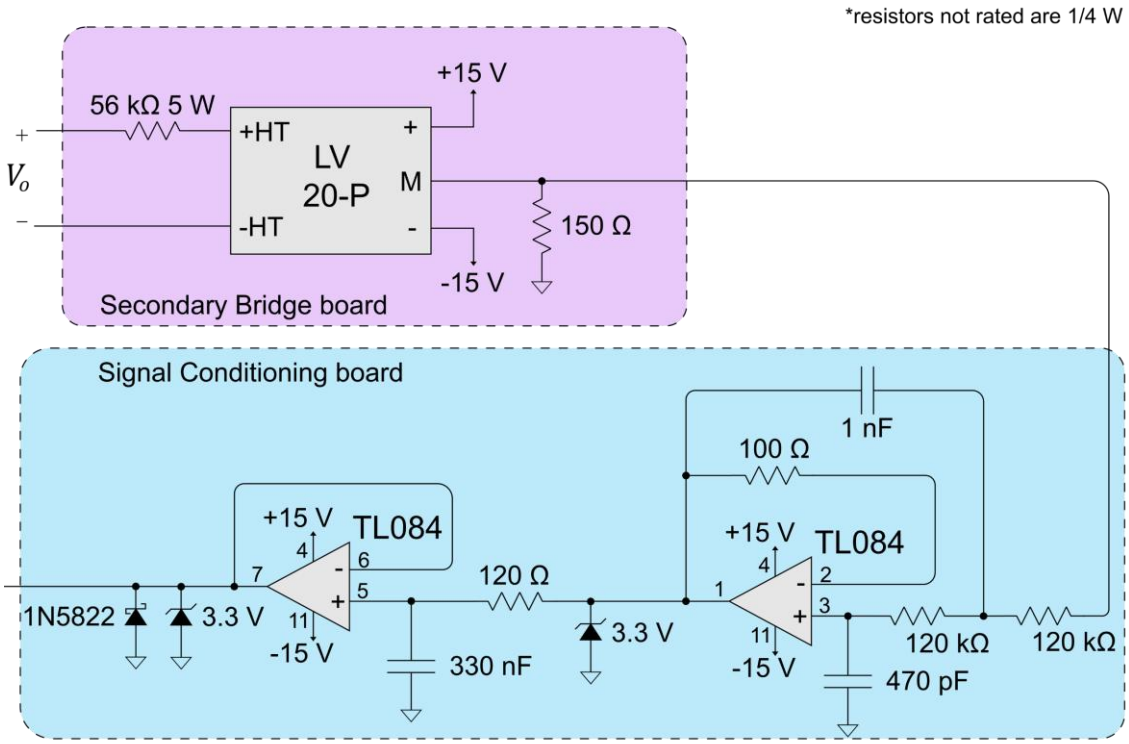
The second filter is a 1st order passive filter. The cut frequency for this filter is double the frequency of the first filter, to avoid interactions between the poles of the two filters. Choosing $C_3 = 330\,nF$, the resistance can be calculated with equation (D.5).

$$R_3 = \frac{1}{2\pi \cdot (2 \cdot f_c) \cdot C_3} = \frac{1}{2\pi \cdot (2 \cdot 2000) \cdot 330 \times 10^{-9}} \approx 120\ \Omega \qquad \text{(D.5)}$$

The op-amp used for the circuit is the TL084, which possesses 4 op-amps in the chip. Two Zener diodes of 3.3 V are used at the output of the op-amps for protecting the DSP pin in case of overvoltage. A Schottky diode (1N5822) is used at the output of the buffer for protecting the DSP pin in case of negative voltage, which can also damage the pin.

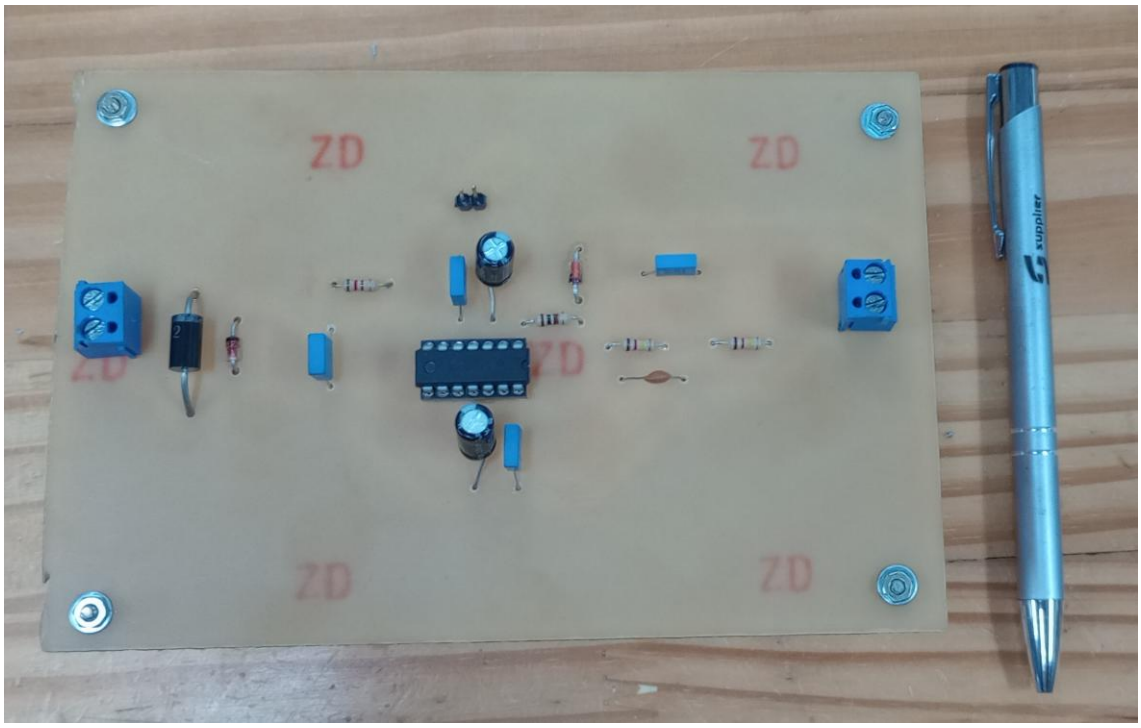
Figure 76 presents the circuit diagram of the signal conditioning board and Figure 77 shows a picture of the PCB.

Figure 76 – Circuit schematic of output voltage sensor and signal conditioning board for testing the mCSPT algorithm.



Source: provided by the author, 2025.

Figure 77 – Picture of signal conditioning board.

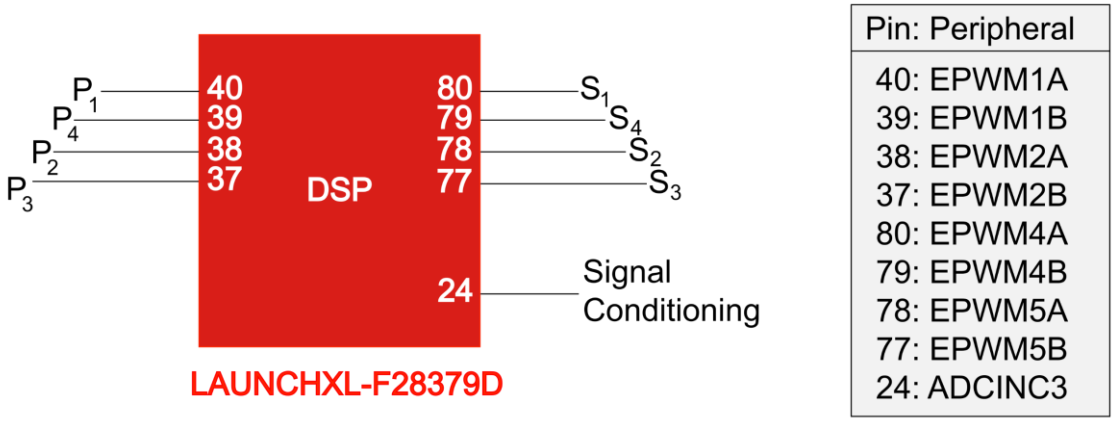


Source: provided by the author, 2025.

APPENDIX E – DSP CODE ALGORITHM IMPLEMENTATION

In this Appendix, it is presented the code implemented in the DSP to test the mCSPT algorithm proposed in Chapter 6. The code is written in C language and the compiler used is the Code Composer Studio 20. In the project, there are three main files: *Peripheral_Setup.h*, *Peripheral_Setup.c* and *main.c*, which are presented in this order down below and can also be seen in (Teichert, 2025). Figure 78 shows the pins used in the DSP board and where it is connected in the prototype (see Figure 63) (ground/reference pin not shown), as well as their respective peripheral.

Figure 78 – Schematic diagram of DSP connections.



Source: provided by the author, 2025.

```
/*
 * file name: Peripheral_Setup.h
 */
#ifndef PERIPHERAL_SETUP_H_
#define PERIPHERAL_SETUP_H_
#include "F28x_Project.h"  // import libraries from ControlSuite

void Setup_GPIO(void); // function to setup GPIO pins of DSP
void Setup_ePWM(void); // function to setup PWM pins of DSP
void Setup_ADC(void); // function to setup ADC module
#define PWM_PERIOD        2500 //20 kHz, timer period for PWM frequency.
#define PWM_HALF_PERIOD    (PWM_PERIOD>>1)
#define PWM_DEADTIME        30  // 300 ns

#endif /* PERIPHERAL_SETUP_H_ */

/*
 *  end of Peripheral_Setup.h
 */
```

```c
/*
 * file name: Peripheral_Setup.c
 */
#include "Peripheral_Setup.h"
#include "F2837xD_Adc_defines.h"
#include "F2837xD_EPwm_defines.h"
#include "F2837xD_adc.h"
#include "F2837xD_epwm.h"
#include "F2837xD_sysctrl.h"

void Setup_GPIO(void){
    EALLOW; //ENABLES modifications in locked/protected registers
    // Configures board LEDS
    GpioCtrlRegs.GPAMUX2.bit.GPIO31 = 0; // set as GPIO, Blue LED
    GpioCtrlRegs.GPADIR.bit.GPIO31 = 1; // set as output
    GpioCtrlRegs.GPBGMUX1.bit.GPIO34 = 0; // set as GPIO, Red LED
    GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1; // set as output
    GpioCtrlRegs.GPBMUX1.bit.GPIO34 = 0; // set as output
    GpioCtrlRegs.GPAPUD.bit.GPIO31 = 1;
    GpioCtrlRegs.GPBPUD.bit.GPIO34 = 1;
    GpioCtrlRegs.GPBCSEL1.bit.GPIO34 = GPIO_MUX_CPU1;
    GpioCtrlRegs.GPACSEL4.bit.GPIO31 = GPIO_MUX_CPU1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO14 = 0;
    GpioCtrlRegs.GPAMUX1.bit.GPIO14 = 0;
    GpioCtrlRegs.GPAPUD.bit.GPIO14 = 1;
    GpioCtrlRegs.GPADIR.bit.GPIO14 = 1;
    // PWMs
    GpioCtrlRegs.GPAGMUX1.bit.GPIO0 = 0; // PWM1A
    GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;  // set as PWM
    GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;   // disable pull-up
    GpioCtrlRegs.GPAGMUX1.bit.GPIO1 = 0; // PWM1B
    GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO1 = 1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO2 = 0; // PWM2A
    GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO2 = 1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO3 = 0; // PWM2B
    GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO3 = 1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO6 = 0; // PWM4A
    GpioCtrlRegs.GPAMUX1.bit.GPIO6 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO6 = 1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO7 = 0; // PWM4B
    GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO7 = 1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO8 = 0; // PWM5A
    GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO8 = 1;
    GpioCtrlRegs.GPAGMUX1.bit.GPIO9 = 0; // PWM5B
    GpioCtrlRegs.GPAMUX1.bit.GPIO9 = 1;
    GpioCtrlRegs.GPAPUD.bit.GPIO9 = 1;
    EDIS;  //DISABLES modifications in locked/protected registers
}
```

```
void Setup_ePWM(void){

    EALLOW;
    CpuSysRegs.PCLKCR2.bit.EPWM1 = 1;    // enable clock for peripheral ePWM
    CpuSysRegs.PCLKCR2.bit.EPWM2 = 1;
    CpuSysRegs.PCLKCR2.bit.EPWM4 = 1;
    CpuSysRegs.PCLKCR2.bit.EPWM5 = 1;
    CpuSysRegs.PCLKCR0.bit.TBCLKSYNC =0; //disable counter clock for setting
up the registers
    EDIS;
    // PWM 1
    EPwm1Regs.TBPRD = PWM_PERIOD;  // Sets timer period, PWM frequency. PRD =
(uCclock / (2xfsx2)), considering updown counter (CTR register), uCclock =
200 MHz
    EPwm1Regs.CMPA.bit.CMPA = PWM_HALF_PERIOD; // desired duty cycle, TBPRD
>> 1 equals D = 0.5;
    EPwm1Regs.TBPHS.bit.TBPHS = 0;          // phase-shift between PWMs,
TBPHS = TBPRD*phi/360
    EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO; // sets up counter
synchronism with other PWMs
    EPwm1Regs.TBCTR = 0x0000; // clears counter for initialization with zero
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // sets up counter for up
down mode (triangle waveform)
    EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE ;        // Disable phase loading
    EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;        // prescale, clock ratio
to SYSCLKOUT. When the desired PWM frequency is too low, prescalling might be
necessary
    EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;           //
    EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;     // load registers in pwmA
only when counter is ZERO or PRD
    EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;   //
    EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;     // pwmB
    EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;   //
    EPwm1Regs.AQCTLA.bit.PRD = AQ_NO_ACTION; // action qualify, desired
action for the pin when the counter reaches a certain value (zero, PRD, or
CMPA)
    EPwm1Regs.AQCTLA.bit.ZRO = AQ_NO_ACTION; //
    EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR; //rising, when counter > CMPA, clear
output (0)
    EPwm1Regs.AQCTLA.bit.CAD = AQ_SET; //falling, when counter < CMPA, set
output (1)
    EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // invert ePWMB signal from
ePWMA, i.e., pwmB is complementary from pwmA
    EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable dead-time
between pwmA and pwmB
    EPwm1Regs.DBFED.bit.DBFED = PWM_DEADTIME;                //falling dead-
time period based in PRD, 100 = 1 us for TBPRD=2000
    EPwm1Regs.DBRED.bit.DBRED = PWM_DEADTIME;                //rising dead-
time period based in PRD
    // Using PWM1 as Trigger for ADC
    EPwm1Regs.ETSEL.bit.SOCAEN = 1;  // Enable SOC on A group
    EPwm1Regs.ETSEL.bit.SOCASEL = ET_CTR_ZERO; // Trigger ADC at top
    EPwm1Regs.ETPS.bit.SOCAPRD = ET_3RD; // Trigger on every 3rd event = 6.6
kHz
```

```
    // PWM 2
    EPwm2Regs.TBPRD = PWM_PERIOD;
    EPwm2Regs.CMPA.bit.CMPA = PWM_HALF_PERIOD;
    EPwm2Regs.TBPHS.bit.TBPHS = PWM_PERIOD; // 180° phase-shift
    EPwm2Regs.TBCTL.bit.PHSDIR = 0;
    EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // set up counter synchronism
with other PWMs
    EPwm2Regs.TBCTR = 0x0000;
    EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
    EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE ;     // ENable phase loading
    EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
    EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
    EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
    EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;   //
    EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;     // pwmB
    EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;   //
    EPwm2Regs.AQTSRCSEL.bit.T1SEL = 7; // enables EPWMxSYNCIN as T1 event
trigger
    EPwm2Regs.AQCTLA.bit.PRD = AQ_NO_ACTION;
    EPwm2Regs.AQCTLA.bit.ZRO = AQ_NO_ACTION;
    EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
    EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;
    EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
    EPwm2Regs.DBFED.bit.DBFED = PWM_DEADTIME;
    EPwm2Regs.DBRED.bit.DBRED = PWM_DEADTIME;

    // PWM 4
      EPwm4Regs.TBPRD = PWM_PERIOD;
      EPwm4Regs.CMPA.bit.CMPA = PWM_HALF_PERIOD;
      EPwm4Regs.TBPHS.bit.TBPHS = 0;  //  will be changed during operation
      EPwm4Regs.TBCTL.bit.PHSDIR = 0;
      EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
      EPwm4Regs.TBCTR = 0x0000;
      EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
      EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE ;
      EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
      EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;
      EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
      EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;
      EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
      EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;
      EPwm4Regs.AQTSRCSEL.bit.T1SEL = 7;
      EPwm4Regs.AQCTLA.bit.PRD = AQ_NO_ACTION;
      EPwm4Regs.AQCTLA.bit.ZRO = AQ_NO_ACTION;
      EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;
      EPwm4Regs.AQCTLA.bit.CAD = AQ_SET;
      EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
      EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
      EPwm4Regs.DBFED.bit.DBFED = PWM_DEADTIME;
      EPwm4Regs.DBRED.bit.DBRED = PWM_DEADTIME;
```

```
    // PWM 5
      EPwm5Regs.TBPRD = PWM_PERIOD;
      EPwm5Regs.CMPA.bit.CMPA = PWM_HALF_PERIOD;
      EPwm5Regs.TBPHS.bit.TBPHS = PWM_PERIOD;
      EPwm5Regs.TBCTL.bit.PHSDIR = 0;
      EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
      EPwm5Regs.TBCTR = 0x0000;
      EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
      EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE ;
      EPwm5Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
      EPwm5Regs.TBCTL.bit.CLKDIV = TB_DIV1;
      EPwm5Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
      EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD;
      EPwm5Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
      EPwm5Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO_PRD;
      EPwm5Regs.AQTSRCSEL.bit.T1SEL = 7;
      EPwm5Regs.AQCTLA.bit.PRD = AQ_NO_ACTION;
      EPwm5Regs.AQCTLA.bit.ZRO = AQ_NO_ACTION;
      EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR;
      EPwm5Regs.AQCTLA.bit.CAD = AQ_SET;
      EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
      EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
      EPwm5Regs.DBFED.bit.DBFED = PWM_DEADTIME;
      EPwm5Regs.DBRED.bit.DBRED = PWM_DEADTIME;
    EALLOW;
    CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    EDIS;
}
```

```
void Setup_ADC(void){

  Uint16 acqps; // variable for number of sample window
  if (ADC_RESOLUTION_12BIT == AdccRegs.ADCCTL2.bit.RESOLUTION)\
    acqps = 250;
  else // resolution is 16 bits
    acqps = 63;  // 320 ns
  EALLOW;
  CpuSysRegs.PCLKCR13.bit.ADC_C = 1; // enables clock for ADC A module
  AdccRegs.ADCCTL2.bit.PRESCALE = 6; // sets ADCCLK divider to /4
  AdcSetMode(ADC_ADCC, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE); //
function for configuration of ADC, single mode (1 pin reading)
  AdccRegs.ADCCTL1.bit.INTPULSEPOS = 1; // Sets interrupt pulse one cycle
before result is finished
  AdccRegs.ADCCTL1.bit.ADCPWDNZ = 1; // power up the ADC
  DELAY_US(1000);
  AdccRegs.ADCSOC0CTL.bit.CHSEL = 3 ; //select channel 3 of ADC C, pin 24
  AdccRegs.ADCSOC0CTL.bit.ACQPS = acqps; // define number of sample window
  AdccRegs.ADCSOC0CTL.bit.TRIGSEL = 5;  // trigger on ePWM1 SOCA
  AdccRegs.ADCSOC1CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC1CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC1CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOC2CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC2CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC2CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOC3CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC3CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC3CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOC4CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC4CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC4CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOC5CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC5CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC5CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOC6CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC6CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC6CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOC7CTL.bit.CHSEL = 3 ;
  AdccRegs.ADCSOC7CTL.bit.ACQPS = acqps;
  AdccRegs.ADCSOC7CTL.bit.TRIGSEL = 5;
  AdccRegs.ADCSOCPRICTL.bit.SOCPRIORITY = 8; // disables robin mode
  AdccRegs.ADCINTSEL1N2.bit.INT1SEL = 7; // end of SOC7 will set INT1 flag
  AdccRegs.ADCINTSEL1N2.bit.INT1E = 1;      // enable INT1 flag
  AdccRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;    // make sure INT1 flag is cleared
  EDIS;
}


/*
 * end of Peripheral_Setup.c
 */
```

```
/**
 * file name: main.c
 */

// Author: Henrique Thomaselli Teichert | 10 June 2025
// DSP LAUNCHXL-F28379D board from Texas Instruments is used
// CODE WRITTEN BASED ON WANER WODSON YOUTUBE TUTORIALS
// https://www.youtube.com/watch?v=JDRp4eQkO3Y
// ControlSuite needs to be installed, v200 files are used
/* List of necessary files in the folder project:
F2837xD_Adc.c
F2837xD_CpuTimers.c
F2837xD_DefaultISR.c
F2837xD_EPwm_defines.h
F2837xD_GlobalVariablesDefs.c
F2837xD_Gpio.c
F2837xD_PieCtrl.c
F2837xD_PieVect.c
F2837xD_SysCtrl.c
*/

#include "F2837xD_device.h"
#include "F2837xD_EPwm_defines.h"
#include "F2837xD_Pie_defines.h"
#include "F2837xD_cputimervars.h"
#include "F2837xD_epwm.h"
#include "Peripheral_Setup.h"
#include "F2837xD_Adc_defines.h"
#include "F2837xD_adc.h"
#include "math.h"

uint32_t count = 0; // unsigned integer 32 bits

float phi = 0; // external phase-shift angle in degrees
int phase_shift = 0; // external phase-shift in bits
float phi_int = 0; // internal phase-shift angle in degrees
int phase_shift_int = 0; // internal phase-shift in bits

int protection = 0;

float adc_reading; // stores the initial value of ADC
uint32_t index = 0 ;

int i;
int N=32; //Number of samples
float LP_filter[32] = {0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0}; // vector for calculating average
of low-pass filter output
float LP_filter_avg = 0; // variable for calculating average of low-pass
filter output
float LP_filter_avg_real = 0; // variable for calculating average of low-pass
filter output

// 9th order low-pass filter, IIR type, passband 500 Hz, stopband 600 Hz,
// sample rate 6.6 kHz, passband ripple 0.01, stopband attenuation 60 dB
const float NUM[10] = {
   0.001756807673,-0.008235667832,  0.01792298257, -0.02095705457,
0.009619504213,
```

```
   0.009619504213, -0.02095705457,  0.01792298257,-0.008235667832,
0.001756807673
};      // discrete function "b" coefficients

const float DEN[10] = {
                1,   -(-7.310033321),    -(24.31672287),    -(-
48.2035408),    -(62.65714645),
     -(-55.32103729),    -(33.15006638),   -(-12.99282169),    -
(3.021174908),   -(-0.317465663)
};      // discrete function "a" coefficients

float LP_filter_yn = 0; // variables for storing values for the low-pass
filter
float LP_filter_xn = 0;
float LP_filter_yn1 = 0;
float LP_filter_xn1 = 0;
float LP_filter_xn2 = 0;
float LP_filter_yn2 = 0;
float LP_filter_xn3 = 0;
float LP_filter_yn3 = 0;
float LP_filter_xn4 = 0;
float LP_filter_yn4 = 0;
float LP_filter_xn5 = 0;
float LP_filter_yn5 = 0;
float LP_filter_xn6 = 0;
float LP_filter_yn6 = 0;
float LP_filter_xn7 = 0;
float LP_filter_yn7 = 0;
float LP_filter_xn8 = 0;
float LP_filter_yn8 = 0;
float LP_filter_xn9 = 0;
float LP_filter_yn9 = 0;

float bit2Vo = (3.0/4096.0); // bit to Volts conversion
float bit2Vo_pol[3] = {-3.5845, 151.3435, 1.3115}; // coefficients of
linearized output voltage of the voltage sensor
float Vo = 0; // output voltage measured used in the algorithm


// mCSPT algorithm variables
int alg_start = 0; // starts the algorithm
int alg_end = 0; // ends the algorithm
float Vo_ref = 383; // output voltage reference
float Vtol = 0.2; // Voltage tolerance
float upper_vo_limit = 0; // upper output voltage limit
float lower_vo_limit = 0; // lower output voltage limit
int steadystate = 0;
int Tw = 1; // flag variable for waiting period triggered by timer0
float phi_step = 1; // external phase-shift step (in degrees)
float phi_int_step = 1; // internal phase-shift step (in degrees)
int flag_ext_step = 0;
int flag_int_step = 0;
float phi_final = 0;
float phi_int_final = 0;



__interrupt void isr_adc_output_voltage(void);
```

```
__interrupt void isr_cpu_timer0(void);
__interrupt void isr_cpu_timer1(void);

int main(void){
    InitSysCtrl();          // Initialize System Control

    DINT;                   // Disable all CPU interrupts (global)
    InitPieCtrl();          // Initialize the PIE control registers to their
default state
    IER = 0X0000;           // Disable CPU interrupts
    IFR = 0X0000;           // Clear all CPU interrupt flags
    InitPieVectTable();     // Initialize the PIE vector table

    Setup_GPIO();
    Setup_ePWM();
    Setup_ADC();
    ConfigureDAC();

    EALLOW;

    PieVectTable.ADCC1_INT = &isr_adc_output_voltage; // call given function
when adc interrupt is activated;
    PieCtrlRegs.PIEIER1.bit.INTx3 = 1;   // enable interrupt column 3 of line
1 , ADC C3     , spruhm8k page 98
    PieVectTable.TIMER0_INT = &isr_cpu_timer0;
    PieCtrlRegs.PIEIER1.bit.INTx7 = 1; // enable interrupt column 7 of line 1
, timer0

    EDIS;
    IER |= (M_INT1); // enable interruptions of line 1

    InitCpuTimers();
    ConfigCpuTimer(&CpuTimer0, 200, 1000000); // 1 second timer

    CpuTimer0Regs.TCR.all = 0x4001; // enables CPU timer interrupt

    EINT;                   // Enable Global interrupts INTM
    ERTM;                   // Enable Global Realtime interrupt DBGM

    GpioDataRegs.GPBDAT.bit.GPIO34 = 1; // turns off red led
    GpioDataRegs.GPADAT.bit.GPIO14 = 0; // pin used for ADC debug

    while(1)                //infinite loop for the main code to be used for
the application
   {
       upper_vo_limit = Vo_ref + Vtol; // defining voltage limits for the
mCSPT execution
       lower_vo_limit = Vo_ref - Vtol;

        if(protection == 1) // if protection is activated, disable PWMs and
turn-off all switches. Code has to be re-flashed into the DSP
        {
            EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm1Regs.CMPA.bit.CMPA = 0; // ZERO duty cycle
            EPwm2Regs.CMPA.bit.CMPA = 0; // ZERO duty cycle
```

```
            EPwm4Regs.CMPA.bit.CMPA = 0; // ZERO duty cycle
            EPwm5Regs.CMPA.bit.CMPA = 0; // ZERO duty cycle
        }  //

        //-----------------------------------------------------------------
-----------------------------------------------
        // mCSPT algorithm
        if(alg_start == 1 && alg_end == 0)
        {
            GpioDataRegs.GPBDAT.bit.GPIO34 = 0; // turns on red led

            if(phi == phi_int) // when both phase-shifts are equal, use the
last stored phase-shift pair and finishes the mCSPT
            {
                phi = phi_final;
                phi_int = phi_int_final;
                alg_end = 1;
                alg_start = 0;
                flag_ext_step = 0;
                flag_int_step = 0;
            }

            if(Vo > lower_vo_limit && Vo < upper_vo_limit) // condition of
output voltage in steady state
            {
                steadystate = 1;
                flag_int_step = 0;
            }
            if (steadystate == 1 && Tw == 0)
            {count++;}
            if (steadystate == 0 && Tw == 0)
            {count = 0;}
            if (count==5) // waits for a count of x consecutives steady state
readings before storing the phase-shift values
            {
                phi_final = phi;
                phi_int_final = phi_int;
                count = 0;
                flag_ext_step = 1;
            }

            if(Vo < lower_vo_limit ) // condition of output voltage out of
steady state
            {
                steadystate = 0;
                flag_ext_step = 0;
                flag_int_step = 1;
            }

            if(Vo > upper_vo_limit) // condition of output voltage out of
steady state
            {
                steadystate = 0;
                flag_ext_step = 1;
                flag_int_step = 0;
            }
```

```
            if(flag_ext_step == 1 && Tw == 0 && flag_int_step == 0) //
external phase-shift decrement
            {
                phi = phi - phi_step;
                Tw = 1;
            }

            if(flag_int_step == 1 && Tw == 0 && flag_ext_step == 0) //
internal phase-shift decrement
            {
                phi_int = phi_int - phi_int_step;
                Tw = 1;
            }

        }

        if(alg_end == 1 && alg_start == 0)
        {GpioDataRegs.GPBDAT.bit.GPIO34 = 1;} // turns off red led

        //-------------------------------------------------------------------
-------------------------------------------------

        // applying phase-shift to PWM signals

        if(phi > 20) // limiting external phase-shhift angle values between
20° and 3°
        {phi = 20; }
        if(phi < 3)
        {phi = 3; }

        if(phi_int > 90) // limiting internal phase-shhift angle values
between 90° and 0°
        {phi_int = 90; }
        if(phi_int < 0)
        {phi_int = 0; }


        if(phi_int >= 0 && phi >= 0) // applying the phase-shift between PWMs
        {
                phase_shift_int = (int) ( ((phi_int/180)*PWM_PERIOD));
                phase_shift = (int) ((phi/180)*PWM_PERIOD);

                EPwm2Regs.TBCTL.bit.PHSDIR = TB_UP; // changes sign of phase
to positive
                EPwm2Regs.TBPHS.bit.TBPHS = PWM_PERIOD - phase_shift_int; //
180 + phase-shift

                EPwm4Regs.TBCTL.bit.PHSDIR = TB_DOWN; // changes sign of
phase to positive
                EPwm4Regs.TBPHS.bit.TBPHS = phase_shift  ; // 0 + phase-shift

                EPwm5Regs.TBCTL.bit.PHSDIR = TB_UP; // changes sign of phase
to negative
                EPwm5Regs.TBPHS.bit.TBPHS = PWM_PERIOD  - phase_shift -
phase_shift_int ; //360 - phase-shift
```

```
                // preventing PWM to remain active when changing to phase-
shift near duty cycle (CMPA)
                if( PWM_HALF_PERIOD <  EPwm2Regs.TBPHS.bit.TBPHS )
                {EPwm2Regs.AQCTLA2.bit.T1U = 1;} // set output to low
                if( PWM_HALF_PERIOD >  EPwm2Regs.TBPHS.bit.TBPHS )
                {EPwm2Regs.AQCTLA2.bit.T1U = 0;} // do nothing

                if( PWM_HALF_PERIOD <  EPwm5Regs.TBPHS.bit.TBPHS )
                {EPwm5Regs.AQCTLA2.bit.T1U = 1;} // set output to low
                if( PWM_HALF_PERIOD >  EPwm5Regs.TBPHS.bit.TBPHS )
                {EPwm5Regs.AQCTLA2.bit.T1U = 0;} // do nothing
        }
   }

    return 0;
}


__interrupt void isr_adc_output_voltage(void){

    GpioDataRegs.GPATOGGLE.bit.GPIO14 = 1; // pin used for debug

    // adc_reading is the average of all voltage measured by the ADC C
registers (0 to 7)
    adc_reading = (float) (AdccResultRegs.ADCRESULT0 +
AdccResultRegs.ADCRESULT1 + AdccResultRegs.ADCRESULT2 +
AdccResultRegs.ADCRESULT3 + AdccResultRegs.ADCRESULT4 +
AdccResultRegs.ADCRESULT5 + AdccResultRegs.ADCRESULT6 +
AdccResultRegs.ADCRESULT7)/8;

    // low-pass filter
    LP_filter_xn =  adc_reading ;
    LP_filter_yn = NUM[0]*LP_filter_xn + NUM[1]*LP_filter_xn1 +
NUM[2]*LP_filter_xn2 + NUM[3]*LP_filter_xn3 + NUM[4]*LP_filter_xn4 +
NUM[5]*LP_filter_xn5 + NUM[6]*LP_filter_xn6 + NUM[7]*LP_filter_xn7 +
NUM[8]*LP_filter_xn8 + NUM[9]*LP_filter_xn9 + DEN[1]*LP_filter_yn1 +
DEN[2]*LP_filter_yn2 + DEN[3]*LP_filter_yn3 + DEN[4]*LP_filter_yn4 +
DEN[5]*LP_filter_yn5 + DEN[6]*LP_filter_yn6 + DEN[7]*LP_filter_yn7 +
DEN[8]*LP_filter_yn8 + DEN[9]*LP_filter_yn9 ; // low-pass filter output
    LP_filter_xn1 = LP_filter_xn; // storing current sample for next
iteration
    LP_filter_yn1 = LP_filter_yn; // storing current output for next
iteration
    LP_filter_xn2 = LP_filter_xn1;
    LP_filter_yn2 = LP_filter_yn1;
    LP_filter_xn3 = LP_filter_xn2;
    LP_filter_yn3 = LP_filter_yn2;
    LP_filter_xn4 = LP_filter_xn3;
    LP_filter_yn4 = LP_filter_yn3;
    LP_filter_xn5 = LP_filter_xn4;
    LP_filter_yn5 = LP_filter_yn4;
    LP_filter_xn6 = LP_filter_xn5;
    LP_filter_yn6 = LP_filter_yn5;
    LP_filter_xn7 = LP_filter_xn6;
    LP_filter_yn7 = LP_filter_yn6;
    LP_filter_xn8 = LP_filter_xn7;
    LP_filter_yn8 = LP_filter_yn7;
    LP_filter_xn9 = LP_filter_xn8;
```

```
    LP_filter_yn9 = LP_filter_yn8;
    LP_filter[index] = LP_filter_yn; // stores current output value in a
vector for average

    index++;
    if (index == N)
    {
        index = 0;
        //average of 32 stored values of the low-pass filter output
        LP_filter_avg = bit2Vo*((LP_filter[0] + LP_filter[1] + LP_filter[2] +
LP_filter[3] + LP_filter[4] + LP_filter[5] + LP_filter[6] +
LP_filter[7]+LP_filter[8] + LP_filter[9] + LP_filter[10] + LP_filter[11] +
LP_filter[12] + LP_filter[13] + LP_filter[14] + LP_filter[15] + LP_filter[16]
+ LP_filter[17] + LP_filter[18] + LP_filter[19] + LP_filter[20] +
LP_filter[21] + LP_filter[22] + LP_filter[23]+LP_filter[24] + LP_filter[25] +
LP_filter[26] + LP_filter[27] + LP_filter[28] + LP_filter[29] + LP_filter[30]
+ LP_filter[31])/N);
        LP_filter_avg_real = bit2Vo_pol[0]*((LP_filter_avg)*(LP_filter_avg))
+ bit2Vo_pol[1]*(LP_filter_avg) + bit2Vo_pol[2];
        Vo = LP_filter_avg_real;
    }

    if(Vo >= 390.0) // if output voltage measured exceeds 390 V, activate
protection (turns off PWMs)
    { protection = 1;}

    GpioDataRegs.GPATOGGLE.bit.GPIO14 = 1; // pin used for debug

    AdccRegs.ADCINTFLGCLR.bit.ADCINT1 = 1 ; //clear INT1 flag
    PieCtrlRegs.PIEACK.bit.ACK1=1;
}

__interrupt void isr_cpu_timer0(void)
{
    GpioDataRegs.GPATOGGLE.bit.GPIO31 = 1; // blinks blue led
    Tw = 0; // clears waiting period flag for mCSPT algorithm

    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}



/**
 * end of main.c
 */
```

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ATESTADO DE VERSÃO FINAL

Eu, Yales Rômulo de Novaes, professor(a) do curso de Mestrado Acadêmico em Engenharia Elétrica, declaro que esta é a versão final aprovada pela comissão julgadora da dissertação/tese intitulada: **"The Dual Active Bridge Converter: A Study on SPS modulation and a Current Stress Reduction Algorithm for DPS Modulation"** de autoria do(a) acadêmico Henrique Thomaselli Teichert.

Joinville, 29 de Setembro de 2025.

Assinatura digital do(a) orientador(a):

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Yales Rômulo de Novaes