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Single-stage high power factor step-up/step-down isolated AC/DC converter

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Abstract: This study presents a single-stage (S^2) isolated current rectifier with power factor correction, based on a full-bridge flyback converter. This converter is designed to operate with adjustable output voltage so that it can operate in two distinct operation modes, step-up or step-down, depending on the input and output voltages. The proposed converter presents some features that make it attractive for many applications, such as constant switching frequency, step-down and step-up operation, high power level capability and the absence of an auxiliary pre-loading circuit to control the inrush current. This study presents the theoretical analysis of the converter for continuous conduction mode as well as experimental results based on a 3 kW prototype.

1 Introduction

Isolated power factor corrected AC–DC PWM (pulse width modulated) converters have been widely used as front-end converters in electronic equipment with power factor correction (PFC) and galvanic isolation requirements. These converters are an alternative for traditional isolated diode rectifiers that draw pulsed current from the AC mains, whose drawbacks are the introduction of unacceptable current harmonics, voltage distortions and electromagnetic interference in the utility line [1]. Passive power filters can be used to mitigate these problems with high efficiency and low cost, but result in bulky and heavy converters because of the size of the line frequency transformer, inductors and capacitors [2].

The conventional solution to achieve high power factor and galvanic isolation is to use a two-stage converter comprising a step-up PFC pre-regulator converter and another DC-DC isolated converter [3–7]. However, it is possible to reduce size and cost by using single-stage (S^2) power sources with power factor correction and galvanic isolation [8–26]. An interesting single-stage isolated converter for power factor correction is the isolated current fed flyback – push–pull rectifier [8]. This isolated converter has high power factor and it can operate as a step-up or step-down converter. However, because of the push-pull features, this converter has some disadvantages that limit its application only for low and medium power levels: transformer saturation and high voltage stress across the switches. Another single-stage configuration is the current fed full-bridge boost converter [9]. This converter has high-frequency galvanic isolation and it also has high power factor. Nevertheless, the switches are subjected to high voltage levels when they are turned off by protection circuits. In addition, this topology only operates as a step-up converter.

Thus, as an attempt to overcome these disadvantages, this paper proposes a current fed full-bridge flyback isolated current rectifier with power factor correction. The main features of the proposed converter are: single-stage converter, high power factor, galvanic isolation, constant switching frequency, step-down or step-up operation, it does not need an auxiliary pre-loading circuit to reduce the startup current (in-rush).

By comparing it with the flyback – push–pull converter, the proposed converter has lower voltage stress across the switches, allowing the utilisation of the switches with reduced voltage and bigger current limits, increasing the range of the power levels. Other advantage is the possibility of using a DC-blocking capacitor in series with the primary winding of the transformer, avoiding its saturation. By comparing it with the full-bridge boost converter, the proposed topology can also operate as a step-down converter and the switches are not subjected to high voltage peaks when the short circuit protection acts blocking all the switches.

With these features, the authors believe that the proposed converter can be very useful for several applications such as front-end converter to AC power sources, variable DC power source to power amplifiers and full-range isolated universal input to AC drivers.

2 Proposed topology and operation principles

Fig. 1 shows a simplified circuit of the proposed converter. The converter comprises a line diode rectifier (D_1, D_2, D_3 and D_4), a flyback-coupled inductor (L_C), four main switches (S_1, S_2, S_3 and S_4), a full-bridge transformer (T_1),

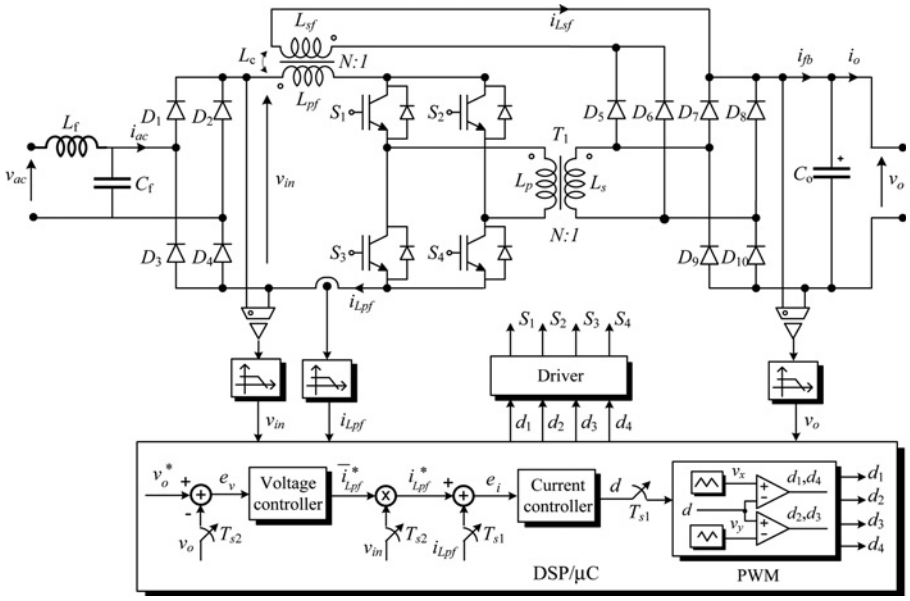

Fig. 1 *Proposed converter*

two flyback diodes (D_5 and D_6), four full-bridge diodes (D_7, D_8, D_9 and D_{10}) and an output filter capacitor (C_o). The turns ratio for both magnetic devices are equal (N:1), as illustrated in Fig. 1. Consequently, the output voltage referred to the primary winding of the transformer is given by

$$V_o' = NV_o \tag{1}$$

This converter is designed for operation in continuous conduction mode (CCM). For this conduction mode, there are two different operation modes depending on the input and output voltage levels. The converter operates in step-up mode when the rectified input voltage is lower than the output voltage referred to the primary winding of the transformer (V_o'), as shown in Fig. 2*a*. On the other hand, the converter operates in step-down mode when input voltage is higher than V_o', as shown in Fig. 2*b*.

θ_1 and θ_2 are the angles that limit the operation mode of the converter and depends of V_o' and V_{in}, where

$$\theta_1 = \text{as in}\frac{V_o'}{V_p} \tag{2}$$

And

$$\theta_2 = \pi - \theta_1 \tag{3}$$

Considering that the switching frequency is much higher than the fundamental frequency, the input voltage can be assumed constant for each switching cycle. As a result, the proposed converter can be analysed as a DC–DC converter in this time interval.

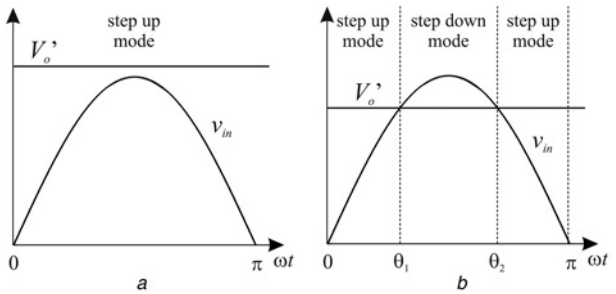

Fig. 2 *Operation modes of the converter*

a Step-up
b Step-up/down

2.1 Step-up mode

In this operating mode, the main switches operate with duty cycle D given by

$$D = \frac{t_c}{T_s}, \quad 0.5 < D \leq 1.0 \tag{4}$$

where t_c is the conduction time of the main switches and T_s is the switching period. The operation stages for this mode are described as follows. The main waveforms for the step-up mode are presented in Fig. 3*a*. The definition of conduction mode is related to the magnetising current $i_{LC} = i_{Lpf} + i_{Lsf}$. As can be seen in Fig. 3*a*, the magnetising current in L_c remains continuous.

2.1.1 First stage ($0 \leq t \leq t_c - T_s/2$): During this stage, all switches are turned on and the input voltage is applied to the primary inductor, as can be seen in Fig. 4*a*. The current i_{LPF} increases linearly whereas L_C stores energy. There is no energy transfer from input source to the load, and only the output capacitor supplies energy to the load.

2.1.2 Second stage ($t_c - T_S/2 \leq t \leq T_s/2$): In this stage, shown in Fig. 4*b*, the switches S_2 and S_3 are turned off, whereas switches S_1 and S_4 remain turned on. The voltage across the primary inductor is $(V_{in} - NV_o)/2$, and the primary inductor current decreases linearly. In this stage, both currents flowing through primary windings of the coupled inductor and the transformer are the same. Similarly, the currents in both secondary windings are the same. These currents are related to each other by the turns ratio. For this reason, the turns ratio of the transformer and the coupled inductor must be equal, as mentioned before. During this stage there is energy transfer from input source to the output through D_5 and D_{10}.

2.1.3 Third stage ($T_s/2 \leq t \leq t_c$): All switches are turned on, which results in an operating stage that is identical to the first stage.

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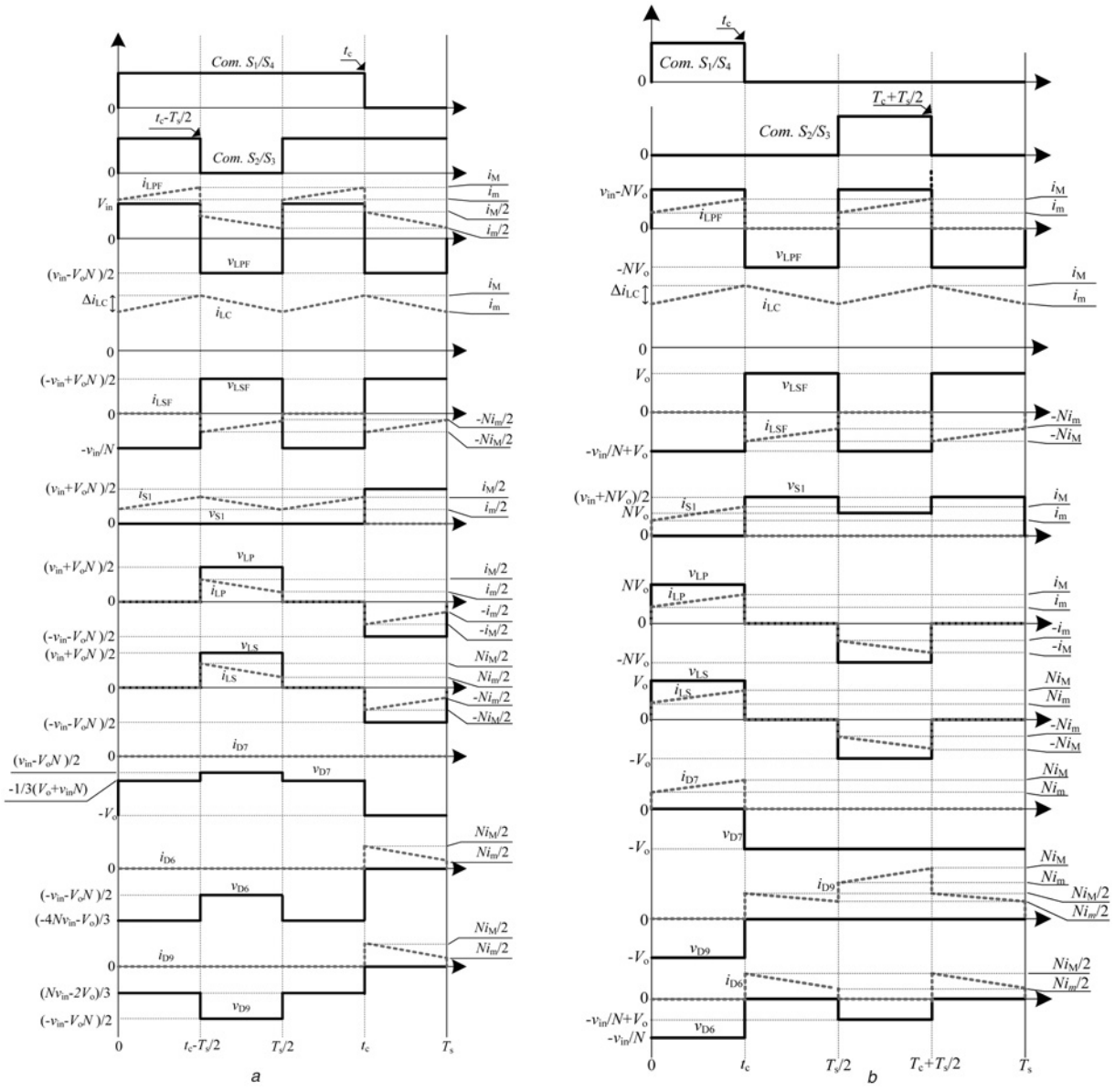

Fig. 3 *Theoretical waveforms for the*

a Step-up mode
b Step-down mode

2.1.4 Fourth stage ($t_c \le t \le T_s$): In this stage, shown in Fig. 4*c*, the switches S_1 and S_4 are turned off and the switches S_2 and S_3 remain turned on. The voltage across the primary inductor is $(V_{in} - NV_o)/2$ and the primary inductor current decreases linearly. The same current flows in the primary winding of coupled inductor and transformer and in their respective secondary windings. During this stage, there is energy transfer from the input source to the output through D_6 and D_9.

2.2 Step-down mode

In this mode, main switches operate with duty cycle $0 < D \le 0.5$. The operation stages for this mode are analysed as follows. The main waveforms for the step-down mode can be seen in Fig. 3*b*. Observe that the conduction mode is also related to the magnetising current in L_c

2.2.1 First stage ($0 \le t \le t_c$): During this stage, illustrated in Fig. 5*a*, switches S_1 and S_4 are turned on and S_2 and S_3 are turned off. The voltage across the primary inductor is $(V_{in} - NV_o)$ and the current i_{LPF} increases linearly. There is energy transfer from input source to the output through the transformer, D_7 and D_{10}.

2.2.2 Second stage ($t_c \le t \le T_s/2$): In this stage, all switches are turned off, as can be observed in Fig. 5*b*. There is current in secondary winding of the coupled inductor because of the stored energy in first stage, which flows to output through D_5, D_6, D_9 and D_{10}. The voltage applied to the secondary inductor is $-V_o$ and the current decreases linearly.

2.2.3 Third stage ($T_s/2 \le t \le t_c + T_s/2$): During this stage, the switches S_2 and S_3 are turned on and S_1 and S_4 remains turned off. Again, the voltage across the primary inductor is $(V_{in} - NV_o)$ and the current i_{LPF} increases linearly. There is energy transfer from input source to the output through the transformer, D_8 and D_9, as shown in Fig. 5*c*.

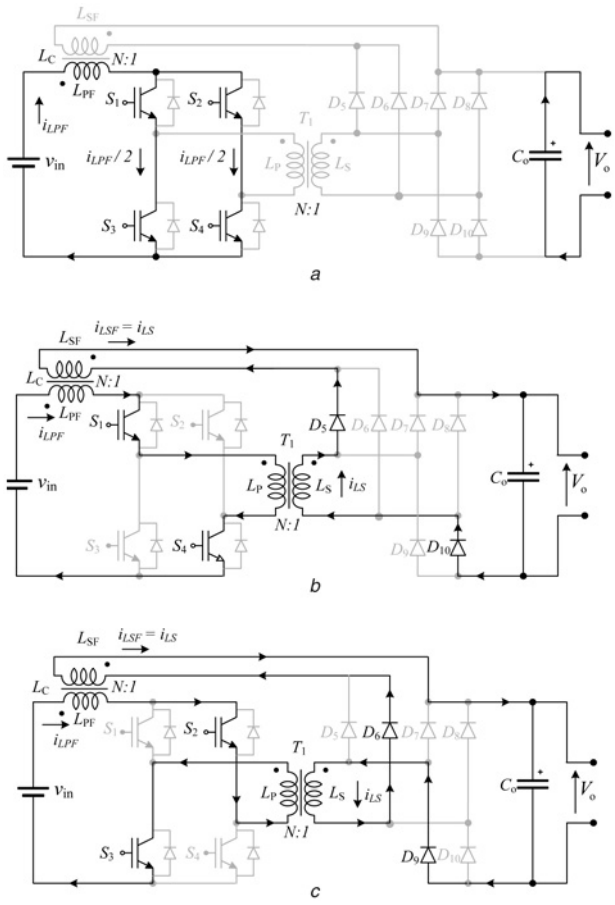

Fig. 4 *Operation stages in step-up mode*

a First and third stages
b Second stage
c Fourth stage

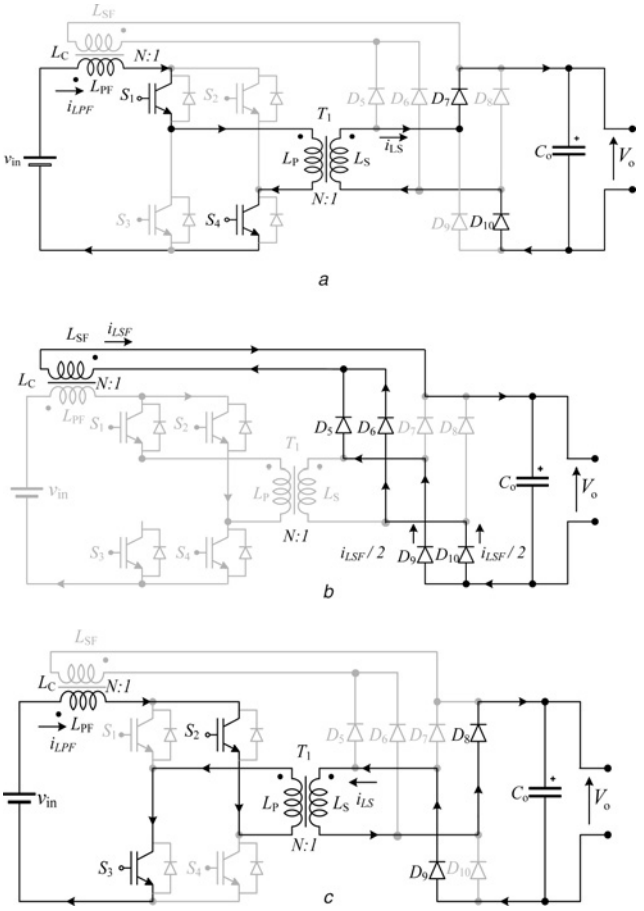

Fig. 5 *Operation stages in step-down mode*

a First stage
b Second and fourth stages
c Third stage

2.2.4 Fourth stage ($t_c + T_s/2 \leq t \leq T_s$): The fourth stage is identical to the second stage.

3 Steady-state analysis

For step-down mode, the average voltage across the primary inductor is

$$vL_{\mathrm{PF\_med}} = \frac{1}{T_s/2}\left[\int_0^{t_c}(V_{\mathrm{in}} - V_o N)\mathrm{d}t + \int_{t_c}^{T/2}(-V_o N)\mathrm{d}t\right] = 0 \tag{5}$$

From (5) the gain in step-down mode is

$$G_{\mathrm{down}} = \frac{V_o}{V_{\mathrm{in}}} = \frac{2D}{N} \tag{6}$$

For the step-up mode, the average voltage across the primary inductor is

$$vL_{\mathrm{PF\_med}} = \frac{1}{T_s/2}\left[\int_0^{t_c - T_s/2} V_{\mathrm{in}}\mathrm{d}t + \int_{t_c - T_s/2}^{T_s/2}\frac{V_{\mathrm{in}} - NV_o}{2}\mathrm{d}t\right] = 0 \tag{7}$$

From (7) the gain in step-up mode is

$$G_{\mathrm{up}} = \frac{V_o}{V_{\mathrm{in}}} = \frac{D}{N(1-D)} \tag{8}$$

Transitions between the step-up and step-down modes occur when the rectified input voltage reaches the output voltage referred to the primary side. From (6) and (8) it is possible to verify that transitions occur when $D = 0.5$, as can be seen in Fig. 6*a*, which shows the DC voltage gain curve for both modes.

In addition, the duty cycle for step-up mode can be estimated from the following expression

$$D(\omega t) = \frac{V_o'}{V_o' + |V_P \sin(\omega t)|} \tag{9}$$

where V_P is the peak value of the input voltage and $0 \leq \omega t < \theta_1$ or $\theta_2 < \omega t \leq \pi$.

On the other hand, the duty cycle behaviour for step-down mode can be obtained from

$$D(\omega t) = \frac{V_o'}{2|V_P \sin(\omega t)|} \tag{10}$$

where $\theta_1 \leq \omega t \leq \theta_2$.

Fig. 6*b* shows the duty cycle behaviour for a half-period of the utility grid, considering $N = 1$, $V_o = 200$ V and $V_P = 311$ V. Therefore one can observe that the transition

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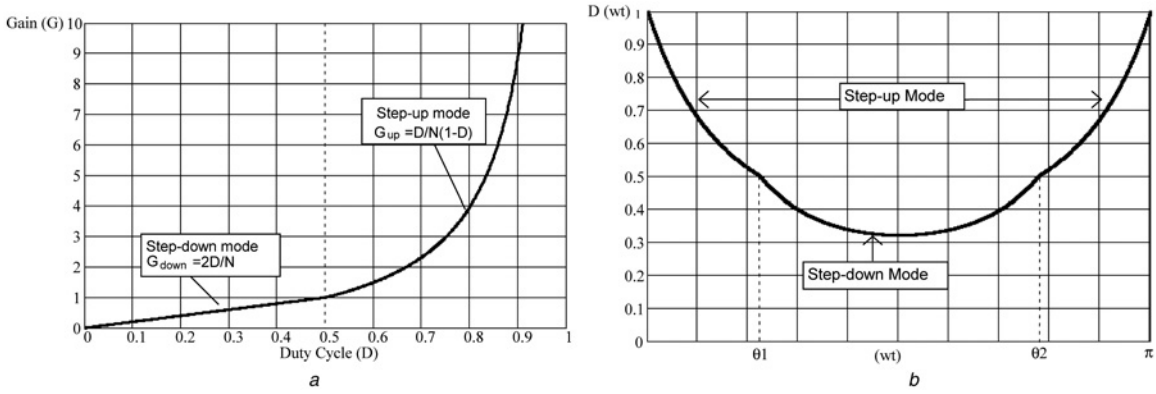

Fig. 6 *Graphs depicting DC voltage gains under both modes*

a DC voltage gain against duty cycle ($N = 1$)
b Duty cycle for a half-cycle of the utility grid

between the step-up and step-down modes is smooth for the proposed converter.

4 Design considerations

The main parameters to be designed for the proposed converter are the turn ratio of transformer and coupled inductor, the inductance of the coupled inductor and the output capacitance.

Owing to the DC voltage gain of this converter, the turn ratio can vary within a wide range and it can be computed from distinct specifications. Optimal turn ratio can be obtained to minimise the losses at the main switches or to limit the maximum voltage across the main switches. In this proposed converter, the turns ratio was chosen to minimise the voltage across the switches; from Figs. 3*a* and *b* it can be observed that maximum voltage in the main switches is directly related to the turns ratio. In order to avoid an elevation of the voltage stress in the main switches, a unitary turns ratio ($N = 1$) for both transformer and coupled inductor was adopted.

Inductance L_C can be designed to limit the maximum current ripple in the coupled inductor Δi_{LC}. The inductance should be calculated for both operation modes and choosing the largest value, ensuring the specified Δi_{LC} in both operation modes.

4.1 Inductance design in step-down mode

In the first stage for step-down mode, the inductance can be designed from the relation of the voltage applied in the primary side of the coupled inductor.

$$V_{in} - V_o N = L_C \frac{\Delta I L_{PF}}{\Delta t} \tag{11}$$

Substituting V_{in} for $V_{in}(\omega t)$ and Δt for DT_s in (11)

$$V_P \text{sen}(\omega t) - V_o N = L_C \frac{\Delta I L_{PF}}{DT_s} \tag{12}$$

Substituting (10) in (12)

$$\frac{L_C \Delta I L_{PF}}{V_o' T_s} = \frac{((V_P)/(V_o))\text{sen}(\omega t) - N}{2((V_P)/(V_o))\text{sen}(\omega t)} \tag{13}$$

The maximum ripple in (13) occurs for $\omega t = \pi/2$ then L_C can be designed by

$$L_C = \frac{N V_o T_s(((V_P)/(V_o)) - N)}{2((V_P)/(V_o))\Delta I L_{PF}} \tag{14}$$

4.2 Inductance design in step-up mode

In the first stage for step-up mode, the inductance also can be designed from the relation of the voltage applied in the primary side of the coupled inductor.

$$V_{in} = L_C \frac{\Delta I L_{PF}}{\Delta t} \tag{15}$$

Substituting V_{in} for $V_{in}(\omega t)$ and Δt for $t_c - T_s/2$ in (15)

$$V_P \text{sen}(\omega t) = L_C \frac{\Delta I L_{PF}}{t_c - T_s/2} \tag{16}$$

Substituting t_c for DT_s in (16)

$$V_P \text{sen}(\omega t) = L_C \frac{\Delta I L_{PF}}{T_s(D - 1/2)} \tag{17}$$

Substituting (9) in (17), then L_C can be designed by

$$L_C = \frac{V_P T_s(N\text{sen}(\omega t) - ((V_P)/(V_o))\text{sen}^2(\omega t))}{2\Delta I L_{PF}(N + ((V_P)/(V_o))\text{sen}(\omega t))} \tag{18}$$

4.3 Capacitance design in both operation modes

The output capacitance can be calculated from the following expression [20]

$$C_o = \frac{P_o}{4\pi f_r V_o \Delta V_o} \tag{19}$$

where P_o is the output power and f_r is the input voltage frequency.

4.4 Low-pass filter design

As can be seen in Fig. 3*b*, the input current is discontinuous in step-down mode. Owing to this, it was necessary to design a

low-pass filter to be used to reduce the ripple of the input current.

The filter capacitance can be obtained from

$$C_f = \frac{1}{2\pi f_{pi} R_{eq}} \tag{20}$$

where f_{pi} is the resonant frequency of the filter and R_{eq} is the equivalent resistance of the converter.

The resonance frequency should be between 50 times the grid frequency (f_r) and 10 times the switching frequency (f_s).

The filter inductance can be obtained from

$$L_f = \frac{1}{(2\pi f_{pi})^2 C_f} \tag{21}$$

In some cases, the grid series inductance can be used in the filter design.

5 Experimental verification

5.1 Prototype description

A prototype of the full-bridge flyback isolated current rectifier was implemented in laboratory to verify experimentally the performance of the proposed converter. Table 1 presents the design specifications, whereas Table 2 describes the circuit parameters and components used to built the experimental setup.

Clamp and snubber circuits had been included in all semiconductors to avoid overvoltage because of the transformer and the coupled inductor leakage inductances. Individual resistor-capacitor-diode (RCD) clamp circuits had been chosen to limit the voltage across the switches and diodes. For the RCD clamp of the main switches was used in 12 kΩ/10 W film resistors, 18 μF/350 V electrolytic capacitor and the ultrafast diode IR HFA16TB120. For the RCD clamp of the output diodes, a 150 kΩ/3 W film resistor, a 1.2 nF/600 V polyester capacitor and ultrafast diode MUR4100 were used. Fig. 1 also presents a simplified block diagram of the control scheme. Multiloop control scheme based on average current mode control is

Table 1 Design specifications

$P_o = 3.0$ kW	output power
$V_o = 400$ V	output voltage
$V_{ac} = 311\sin(\omega t)$ V	input voltage
$\Delta V_o = 3.5$ V	maximum output voltage ripple
$f_r = 60$ Hz	input frequency
$f_s = 100$ kHz	switching frequency
$\Delta i_{LC} = 7.7$ A	maximum input current ripple
$\eta = 90\%$	efficiency
$N = 1$	turns ratio

Table 2 Circuit parameters and components description

S_1, S_2, S_3, S_4	switches: IRGP50B60PD
D_5–D_{10}, D_{s1}–D_{s4}	diodes: HFA16TB120
D_1, D_2, D_3, D_4	bridge rectifier: SK50B08
C_o	electrolytic capacitor: 6 × 470 μF/400 V
C_f	polypropylene capacitor: 4 × 100 nF
L_c	planar inductor: I1000DC-16-16, $L = 100$ μH, 16 turns
L_f	grid series inductance ≅ 2, 5 mH
T_1	planar transformer: T1000AC-8-8, 8 turns

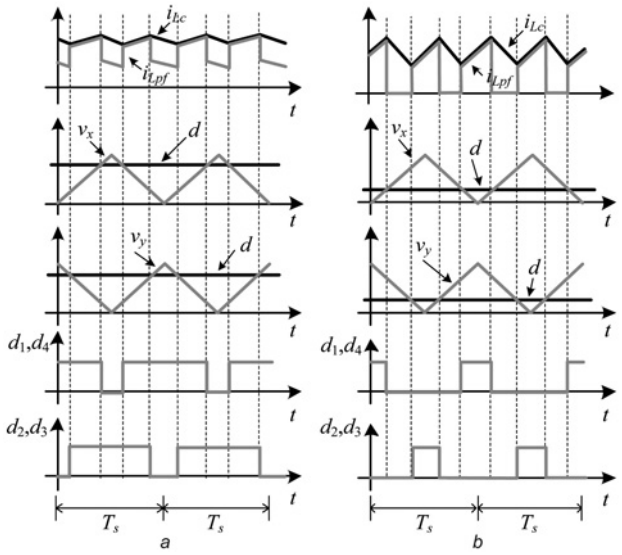

Fig. 7 *PWM strategy*

a Step-up mode
b Step-down mode

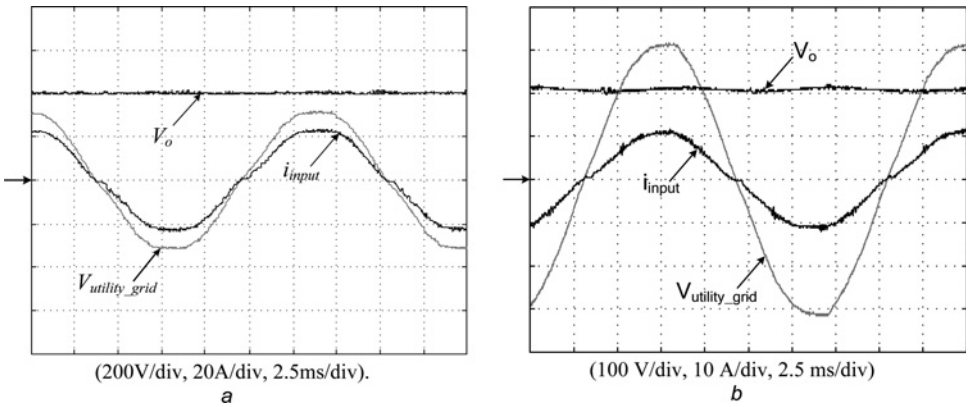

Fig. 8 *Input/output voltage and input current*

a Step-up mode
b Step-down mode

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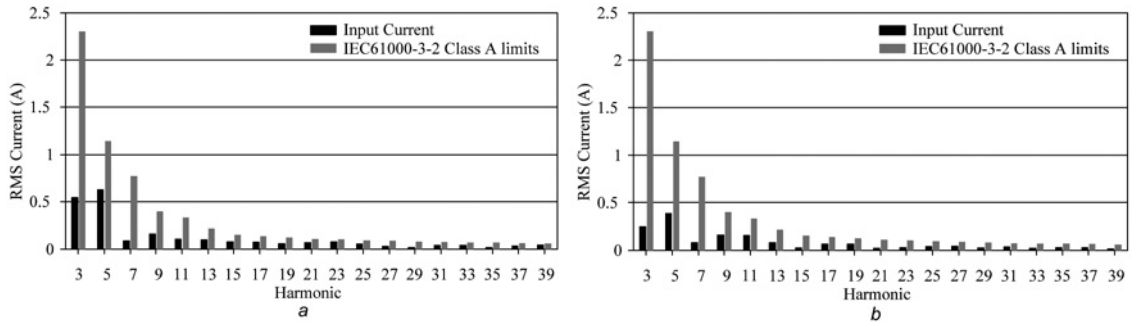

Fig. 9 *Odd harmonics of the input current waveform and the IEC61000-3-2 Class A limits*

a Step-up mode
b Step-down mode

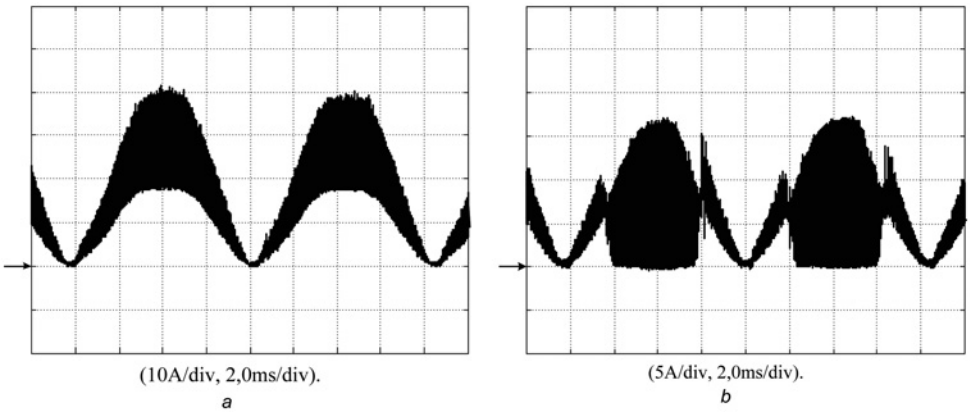

Fig. 10 *Primary inductor current*

a Step-up mode
b Step-down mode

used to control both the input current and output voltage waveforms. A complete control modelling and design are presented in [26]. The current controller forces the input current to track the reference current, although a voltage controller is used to regulate the output voltage. This control scheme has been implemented in a DSP TMS320F2812 from Texas Instruments®.

The modulation patterns for both modes are shown in Fig. 7. PWM command signals for the main switches are generated by two triangular waveforms phase-shifted between them in 180. Each triangular waveform is used to generate command signals for S_1 and S_4 and S_2 and S_3, respectively.

5.2 Experimental results

The performance of the proposed converter was investigated for both operation modes (step-up and step-down modes). Fig. 8*a* shows input voltage and input current waveforms for a resistive load of 50 Ω at nominal output and input voltages, operating in step-up mode. Fig. 8*b* shows the output and input voltages and the input current operating in step-down mode, at $V_o = 200$ V and a resistive load of 28 Ω.

Input current harmonic spectrum at the step-up mode and step-down mode is shown in Figs. 9*a* and *b*, respectively, whose values are compared with the limits of IEC61000-3-2 standard (class A) [1]. As can be seen, all current harmonics comply with the specification given in [1] for both modes. The total harmonic distortion (THD) of the input current waveform is 5.6% and the input power factor is 0.99 for the step-up mode. At the step-down mode, the THD of the input current waveform is 6.3% and the input power factor is 0.99. Fig. 10*a* shows the behaviour of the current in the primary winding of the coupled inductor in step-up mode, and Fig. 10*b* shows the same behaviour in step-down mode. In both modes, the frequency is twice the switching frequency.

Fig. 11 shows the efficiency curve for both operating points. For $V_o = 200$ V, the output power was derated to avoid overcurrents in the output stage.

Table 3 shows a comparative of the proposed converter and a classical topology using a boost PFC in series with an isolated full-bridge DC–DC converter.

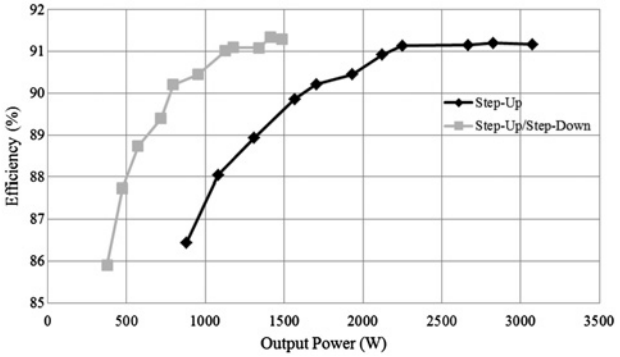

Fig. 11 *Efficiency curve of step-up mode and step-down mode*

Table 3 Comparative with the proposed converter with classical topology boost + full-bridge

Comparative	Proposed converter	Boost + full-bridge
number of switches	4	5
number of diodes	6	5
auxiliary pre-loading circuit	unnecessary	necessary
number of driver circuit	4	5
number of magnetics	2	3
maximum voltage stress	$(V_{in} + NV_o)/2$	V_o
number of sensors	2	4
efficiency	91%	$\cong$ 90%

6 Conclusions

From analysis and results presented in this paper, it was demonstrated that the isolated full-bridge flyback current rectifier satisfies the proposed specifications, which are: single-stage converter, high power factor, galvanic isolation, magnetic components operating at high frequency, output voltage control, controllable startup input current, step-up or step-down operation and reduced cost (about 40% less than the boost PFC + full-bridge DC–DC topology). Additionally, the modulation and control strategies are simple, so that they can be implemented using either analogue or digital approaches. The converter efficiency was close to 91% for a wide range of output power in both operating modes. The authors believe that the proposed topology can be very useful for isolated power factor correction AC power sources and uninterruptible power supplies.

7 References

1 International Standard, Electromagnetic compatibility (EMC)–Part 3-2–Limits for harmonic current emissions (equipment input current up to and including 16 A per phase), IEC Standard 61000-3-2, 2005

2 Wang, C.-M.: 'A new single-phase ZCS-PWM boost rectifier with high power factor and low conduction losses', *IEEE Trans. Ind. Electron.*, 2006, **53**, pp. 500–510

3 Lee, F.C., Cho, B.H., Ridley, R.B., Vlatkovic, V., Sabaté, J.A.: 'Design considerations for high-voltage, high-power, full-bridge, zero-voltage-switching PWM converter'. IEEE APEC'90, 1990, pp. 275–184

4 Redl, R., Sokal, N., Balogh, L.: 'A novel soft-switching full-bridge DC/DC converter: analysis, design considerations and experimental results at 1.5 kW, 100 kHz', *IEEE Trans. Power Electron.*, 1991, **6**, pp. 408–418

5 Zhu, L.: 'A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications', *IEEE Trans. Power Electron.*, 2006, **21**, pp. 422–429

6 Lo, Y.-K., Lin, J.-Y., Ou, S.-Y.: 'Switching frequency control for regulated discontinuous-conduction-mode boost rectifiers', *IEEE Trans. Ind. Electron.*, 2007, **54**, pp. 760–768

7 Hwu, K.I., Yau, Y.T.: 'An interleaved AC–DC converter based on current tracking', *IEEE Trans. Ind. Electron.*, 2009, **56**, pp. 1456–1463

8 Torrico Bascope, G.V., Barbi, I.: 'Isolated flyback-current-fed push–pull converter for power factor correction'. 27th Annual IEEE Power Electronics Specialists Conf., 1996, PESC '96 Record, 1996, vol. 2, pp. 1184–1190

9 Chen, J.-F., Chen, R.-Y., Liang, T.-J.: 'Study and implementation of a single-stage current-fed boost PFC converter with ZCS for high voltage applications', *IEEE Trans. Power Electron.*, 2008, **23**, pp. 379–386

10 Yim-Shu, L., Bo-Tao, L.: 'Adding active clamping and soft switching to boost-flyback single-stage isolated power-factor-corrected power supplies', *IEEE Trans. Power Electron.*, 1997, **12**, pp. 1017–1027

11 Jinrong, Q., Lee, F.C.Y.: 'A high-efficiency single-stage single-switch high-power-factor AC/DC converter with universal input', *IEEE Trans. Power Electron.*, 1998, **13**, pp. 699–705

12 Jinrong, Q., *et al.*: 'Single-stage single-switch power-factor-correction AC/DC converters with DC-bus voltage feedback for universal line applications', *IEEE Trans. Power Electron.*, 1998, **13**, pp. 1079–1088

13 Daniele, M., Jain, P.K., Joos, G.: 'A single-stage power-factor-corrected AC/DC converter', *IEEE Trans. Power Electron.*, 1999, **14**, pp. 1046–1055

14 Garcia, O., *et al.*: 'A simple single-switch single-stage AC/DC converter with fast output voltage regulation', *IEEE Trans. Power Electron.*, 2002, **17**, pp. 163–171

15 Miaosen, S., Zhaoming, Q.: 'A novel high-efficiency single-stage PFC converter with reduced voltage stress', *IEEE Trans. Ind. Appl.*, 2002, **38**, pp. 507–513

16 Moschopoulos, G.: 'A simple AC-DC PWM full-bridge converter with integrated power-factor correction', *IEEE Trans. Ind. Electron.*, 2003, **50**, pp. 1290–1297

17 Shiguo, L., Weihong, Q., Wenkai, W., Batarseh, I.: 'Flyboost power factor correction cell and a new family of single-stage AC/DC converters', *IEEE Trans. Power Electron.*, 2005, **20**, pp. 25–34

18 Wu, T.-F., Hung, J.-C., Tseng, S.-Y., Chen, Y.-M.: 'A single-stage fast regulator with PFC based on an asymmetrical half-bridge topology', *IEEE Trans. Ind. Electron.*, 2005, **52**, pp. 139–150

19 Lai, C.M., Shyu, K.K.: 'A single-stage AC/DC converter based on zero voltage switching LLC resonant topology', *IET Electr. Power Appl.*, 2007, **1**, pp. 743–752

20 Ismail, H.E., Sabzali, J.A., Al-Saffar, A.M.: 'Buck-boost-type unity power factor rectifier with extended voltage conversion ratio', *IEEE Trans. Ind. Electron.*, 2008, **55**, pp. 1123–1132

21 Agamy, M.S., Jain, P.K.: 'A three-level resonant single-stage power factor correction converter: analysis, design, and implementation', *IEEE Trans. Ind. Electron.*, 2009, **56**, pp. 2095–2107

22 Heng-Yi, L., Hung-Chi, C., Lon-Kou, C.: 'Analysis and design of a single-stage parallel AC-to-DC converter', *IEEE Trans. Power Electron.*, 2009, **24**, pp. 2989–3002

23 O'Sullivan, D.L., Egan, M.G., Willers, M.J.: 'A family of single-stage resonant AC/DC converters with PFC', *IEEE Trans. Power Electron.*, 2009, **24**, pp. 398–408

24 Ribeiro, H.S., Borges, B.V.: 'Analysis and design of a high-efficiency full-bridge single-stage converter with reduced auxiliary components', *IEEE Trans. Power Electron.*, 2010, **25**, pp. 1850–1862

25 Hung-Liang, C., Yao-Ching, H., Chi-Sean, L.: 'A novel single-stage high-power-factor AC/DC converter featuring high circuit efficiency', *IEEE Trans. Ind. Electron.*, 2011, **58**, pp. 524–532

26 Duarte, J., Rech, C., Mezaroba, M., Michels, L.: 'Digital control of a full-bridge – flyback isolated current rectifier with power factor correction'. Power Electronics Conf., 2009. COBEP'09, Brazilian, 2009, pp. 377–384

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