HIGH VOLTAGE ULTRA-FAST TURN ON FIXED ON-TIME POWER SWITCH

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***Abstract* – This paper presents a High Voltage Fixed On-Time Power Switch capable of performing ultra-fast turn on. The presented high voltage switch is obtained through the usage of low voltage switches stacked to support higher voltages. The series connection of power MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) is reviewed and practical considerations are discussed. Results on static and dynamic voltage sharing are presented for a 1500V switch built using four 400V MOSFETs. The driver circuit topology used is basically a Flyback converter. Its operation is discussed and mathematically evaluated. Due to the driver methodology developed, the gate side is isolated and the current injection assures a rise time shorter than 10ns. Safety considerations involving the printed circuit board and magnetics assembly are also discussed. Experimental results and pictures of the prototype itself are presented in order to validate the specifications.**

***Keywords* – High Voltage Switches, Series Connection of Power Switches, Ultra-Fast Turn on, Fixed On-Time.**

I. INTRODUCTION

The last decade was a decade of big improvements regarding to power semiconductors. High voltage discrete semiconductors had their voltage limits pushed to levels never expected before. IGBTs (Insulated Gate Bipolar Transistors) that operate under many kilovolts, MOSFETs switching much more than a kilovolt and so on. The same improvements occurred with current and speed limits, however, the market still suffers with the lack of components that combine all these characteristics.

Modern applications like food sterilization, biomedical drug delivery research and Electromagnetic Compatibility related standards are pushing these limits each day. Standards like the IEC61000-4-4 [1] propose the usage of Fast Transient/Burst Generators capable of generating signals with rise times about 5ns at voltage levels of 4kV. As previously mentioned, discrete semiconductors currently found on the market cannot perform such specifications.

Willing to achieve speed and voltage levels like those mentioned, companies specialized on high voltage applications managed to create semiconductor based devices that satisfy such specifications. These devices are currently found at prices higher than a thousand US dollars.

It is known that these devices are series/parallel stacks of power switches controlled in such way they share the same voltage and current among the stack and perform high speed turn on.

Academic studies related to series connection of switches have being carried for many years. The first attempts to use achieve ultra-fast switching of series connected power switches to MOSFETs occurred in the early 90's. At that time it was verified that the voltage sharing problems that occurred were a consequence of parameter variations during the fabrication process and to driver circuit and layout unbalances. In 1992 Baker and Johnson presented the Capacitive Coupling method [2] for series operation of MOSFETs. It was the first structure capable of handling higher voltages using series connected MOSFETs that allowed ultra-fast turn on. The studies related to this technique continued during several years [3][4][5] and are still being carried out. However, subsequent studies like Keith, Pringle, Rice and Birke paper [6] stated that the Capacitive Coupling method is difficult to experimentally trim the theoretical capacitance distribution needed to achieve correct operation of the circuit. The authors also verified those conclusions on a previous attempt to satisfy their project specifications and left the Capacitive Coupling method behind.

The Distributed Magnetic Coupling presented in [6] achieved both voltage balance and fast turn on. Even using very high gate currents [6] achieved rise times about 45 ns and it is still slow for applications like the IEC61000-4-4 Burst Generator.

Following the timeline, many structures and methods for achieving voltage balance on series connected IGBTs were presented. Gerster [7] proposed the synchronism of the switches using digital processors, an unviable structure to this application due to the ultra-fast turn on. Palmer and Githiari [8] proposed the active control of the gate voltage. Consoli, Musumeci, Oriti and Testa [9] proposed the control of the voltage sharing by the charge characteristics of the gate capacitance and so on.

Recent efforts published by Sasagawa, Abe and Matsube [10] used what they called Gate-Balancing Cores to synchronize IGBTs connected in series. They used one magnetic core to connect each adjacent gate inputs to synchronize the switches.

Since none of the previous studies achieved ultra-fast turn on and due to the fact that, in general, MOSFETs are faster than IGBTs and even most of the current research on this subject over the engineering community being related to series connection of IGBTs, the usage of MOSFETs in order to achieve ultra-fast turn on speed still stands.

The High Voltage Ultra-Fast Turn On Fixed On-Time Switch presented in this paper was created using series connected IRF740 MOSFETs to create a switch capable of performing at least 10ns fall time and 150ns fixed on-time.

The gate driver used to achieve such speed levels is a Flyback like driver and its design, assembly considerations and experimental results are presented. Experimental results and pictures of the develop switch are also presented at the specified voltage level.

II. HIGH VOLTAGE ULTRA-FAST TURN ON FIXED ON TIME POWER SWITCH

Focusing on the most important specification, the turn-on speed, the authors verified the possibility of using a Flyback like driver. The Flyback Mosfet Driver presented is in fact a Flyback converter that uses the switch capacitance as its output capacitor, a zener to protect the gate input and a load resistance in parallel with the output to quickly discharge the switch gate input capacitor after the inductor discharge.

Fig. 1 presents the circuit of the developed driver in the series stack configuration used to build the High Voltage switch. The presented driver has five operational stages.

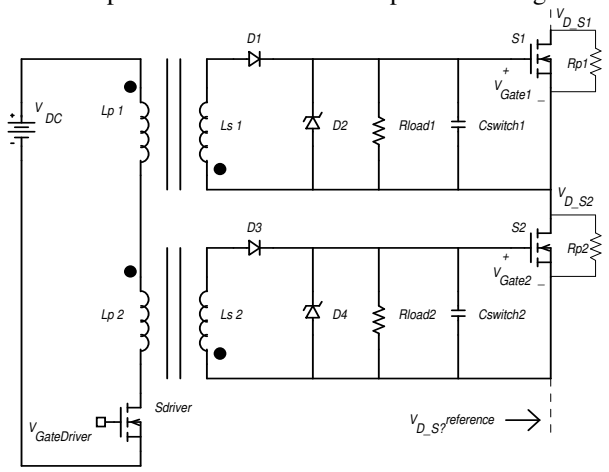

Fig. 1 Isolated Ultra-Fast Fixed On-Time Gate Driver.

A. Operational Stages

The first operational stage is shown in Fig. 2. During this operational stage the driver switch is closed and the driver is storing energy in the primary side inductor. The inductor current rises with a fixed slope and will store an amount of energy that can be easily calculated using basic physics.

The second operational stage is shown in Fig. 3. It begins when the switch is opened. Since the secondary inductance is specified to be very small, the energy previously stored in the coupled inductors is started being sent to the switch gate input capacitance at high speed until the gate input voltage reach the zener voltage. Since the application of the proposed switch will not be a ZVS (Zero Voltage Switching) application, the Miller effect should appear during the second operational stage as shown in [11]. Before the closing process starts the Drain-Source voltage is considerably high and as shown in [12] it should improve this effect. It will slow down the closing process but it is expected to have no major problems due to the current injection characteristics of the driver. The switch gate voltage rises very quickly and it is closed at a very high speed. Due to the load resistance is specified at values higher than a dozen of ohms, the energy consumed on it during this very quick stage does not affect the ultra-fast turn-on.

The third operational stage is presented in Fig. 4. After the gate voltage reaches the zener voltage, the secondary inductor current keep flowing through the zener diode and the load resistance. Since the inductor current is still higher than the load resistance current at the imposed zener voltage, the inductor current keep the switch closed until its energy is almost fully discharged by the zener diode and the load resistance. The secondary side current slope is fixed due to the fact that the secondary inductor voltage is clamped at the zener voltage. This slope will be used to calculate the fixed on-time on further sections.

When the secondary inductor current cannot maintain the load resistance voltage at the zener voltage anymore, the fourth operational stage begins. The equivalent circuit is shown in Fig. 5. Since the load resistance is specified to be smaller than a hundred ohms, the gate input capacitance is quickly discharged and the switch is opened after the fixed on-time granted by the third operational stage. The Miller effect will also occur during the fourth operational stage but it is expected no interfere due to its occurrence.

In the fifth operational stage there is no current flow in the circuit and the driver is ready for the next operational cycle. During this stage, the low load resistance also assures noise immunity.

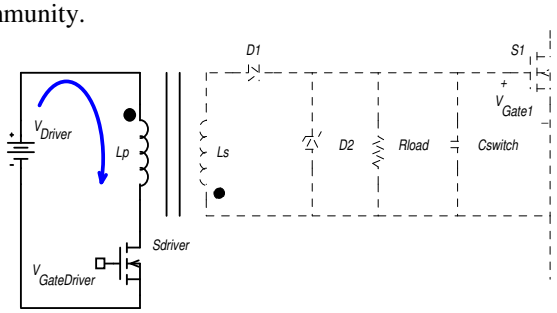

Fig. 2 First operational stage of the Flyback driver.

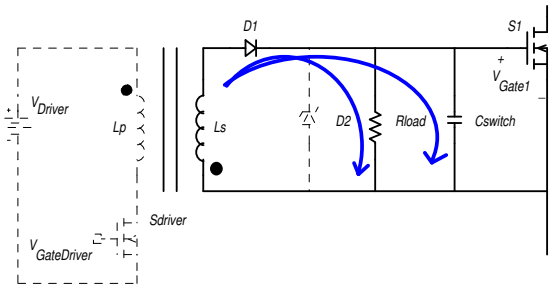

Fig. 3 Second operational stage of the Flyback driver.

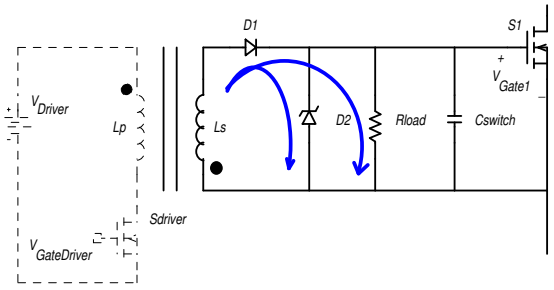

Fig. 4 Third operational stage of the Flyback driver.

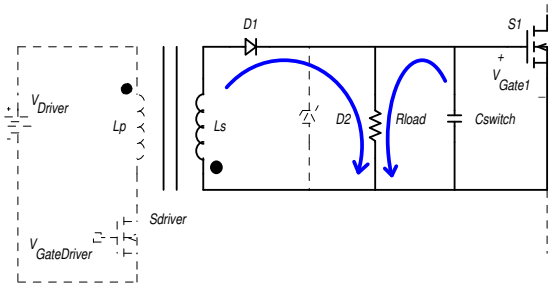

Fig. 5 Fourth operational stage of the Flyback driver.

B. Mathematical Analysis

The idealized driver behavior is shown in Fig. 6. The mathematical evaluation of the circuit used basic physics math and some information that can be found on the switches datasheet. It is worth noting that the mathematical analysis assumes ideal behavior of the circuit but as it is shown on the experimental results, parasitic effects have great influence on the ideal waveforms shape but do not interfere on the purpose of the circuit.

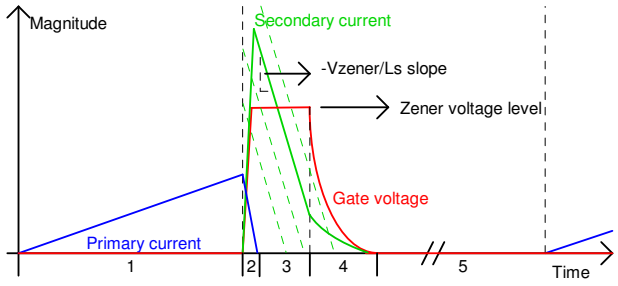

Fig. 6 Driver theoretical waveforms.

The mathematical analysis uses the following nomenclature:

L_P - Primary side inductor.
L_S - Secondary side inductor.
E_{LP} - Primary side inductor energy.
I_{LPpeak} - Primary side inductor current peak.
C_S - Switch gate input capacitor.
E_C - Switch gate input capacitor energy.
V_{Gate} - Switch gate input capacitor voltage.
V_{Zener} - Zener clamping voltage (The same as V_{Gate}).
V_{Driver} - DC voltage applied to the primary inductor.
T_{ON} - Period of time the primary inductor receives V_{DC}.
T_{Closed} - High voltage switch fixed on-time.

The basic physics relationships used during the mathematical analysis are presented below.

Primary side inductor energy can be calculated using (1).

$$E_{LP} = \frac{L_P \cdot I_{LPpeak}^{\,2}}{2} \tag{1}$$

The energy stored on the gate input capacitance is calculated using (2) and its charge using (3).

$$E_C = \frac{C_S \cdot V_{Gate}^{\,2}}{2} \tag{2}$$

$$Q_C = C_S \cdot V_{Gate} \tag{3}$$

The current peak starting from zero on the primary side inductor under a constant voltage after a period of time is calculated using (4).

$$I_{Lpeak} = \frac{V_{DC} \cdot T_{ON}}{L_P} \tag{4}$$

The design starts combining equations (1), (2), (3) and (4) to find the relationship presented in (5) that is used to calculate the primary side inductor. V_{Driver} and T_{ON} should be arbitrarily specified based on power sources available and the response time of the switch. T_{ON} is the amount of time the driver switch will be closed storing energy in the primary side inductor. A small T_{ON} is interesting since it imposes a delay between the control and the effective start of the closing process. V_{Gate} is the highest level the gate voltage will reach that correspond to the zener voltage.

Q_G is the most important value in this equation. Since power switches datasheets present the necessary charge to raise the gate input voltage to the threshold voltage. It is obtained applying a multiplicative factor M to Q_C. Power switches usually have a threshold voltage about 4 volts and a maximum gate voltage of 20V. So the necessary charge to fully close the switch is usually 5 times bigger than the one presented in the datasheet. Since the presented driver uses extra energy to maintain the switch closed indirectly applying voltage to the gate input, these factor need to be much bigger to achieve the desired fixed on-time.

The mathematical specification of Q_G is possible through the sum of the energy needed to close the switch and the amount of energy the inductor will expend on the zener diode during the fixed on-time. If the designer chooses a high capacitance zener diode, the electric charge necessary to raise its parasitic capacitance voltage should also be added to the calculated Q_G. Since the parasitic effects affect the circuit behavior, it is easier to specify an initial value and adjust it experimentally later by changing V_{DC} or T_{ON} and consequently moving the secondary side current slope up and down as desired and shown in Fig. 6.

$$L_P = \frac{\left(V_{Driver} \cdot T_{ON}\right)^2}{Q_G \cdot V_{Gate}} \tag{5}$$

Assuming an ideal system with no losses, the secondary inductor is calculated using (6). It is very important that T_{Closed} is specified small because it will result in a small secondary inductor that will allow a high current peak that is an important factor to achieve the ultra-fast turn-on.

$$L_S = \frac{\left(V_{Zener} \cdot T_{Closed}\right)^2}{2 \cdot E_{LP}} \tag{6}$$

C. Series connection of switches using the presented Driver

The feasibility of building a switch stack able to handle higher voltages was analyzed. Due to the fact that the greatest challenge regarding series connection of power switches is the voltage sharing among the switches, both dynamic and static unbalances where studied.

Part of the assembled switch stack is presented in Fig. 1. As it is shown, the series connected switches are assumed to have their gate drivers equal and series connected on the control side.

Connecting the primary side inductors in series assures that at the end of each energy storage operational stage the

energy in the drivers are equal because it depends mostly on the current as shown in equation(1).

The ultra-fast fixed on-time gate driver presented in this paper was assumed to impose no dynamic voltage unbalance to the switches during the turn on process due to the fact that the switches would receive an ultra-fast energy injection granted by the driver topology. Even variations on the magnetics assembly and component parameters should not interfere in the closing process voltage balance. This assumption was experimentally verified and the results will be shown on further section.

The turn off process was assumed to be responsible for imposing dynamic voltage unbalance because of variations on the resistances responsible for discharging the gate input capacitances, usually 10% tolerance resistors, and for variations on the gate input capacitances among the switches that is common even for switches from the same production batch. In order to control the time constant of each discharge circuit it is proposed the usage of trimming potentiometers connected in series with the load resistance to allow the individual regulation of the transient behavior of each switch on the stack. The variable resistance should be experimentally trimmed and the fixed resistance is necessary to assure a minimum resistance to allow switching and achieve the ultra-fast turn on. Experimental results for the turn off process are also presented on further section.

As already mentioned in many papers and manufacturers catalogs, the easiest way to achieve static voltage balance is to connect resistances in parallel to each of the switches. These resistances are presented in Fig. 1 and were calculated based on the leakage current of the switches. Since the switch stack will be opened during most of the time, the nominal voltage of each individual switch will be applied to its parallel resistor. So, care must be taken in order to minimize losses.

III. ASSEMBLY TIPS AND SWITCHES SPECIFICATION

A. Switches Specification.

While choosing the switches the designer must use switches with low Drain-Source inductance. It was verified through many power switches datasheets that the higher the current capability of the discrete power switches, the higher the inductances are. Tests using high current switches resulted in slower turn on transients.

Among switches with the same current capability and inductances, it is recommended to choose the one with smaller Total Gate Charge parameter that is usually represented by the symbol Q_G.

If the necessary current capability of the switch under design is higher than the ones encountered in small size switches, instead on choosing a high current switch, it is recommended to use a matrix like topology with switches in series and parallel. Some manufacturers of devices like the one presented in this paper also validate this conclusion through information they provide about their products in their datasheets.

B. Passive components and Printed Circuit Board (PCB).

It is known and was experimentally verified that the component leads and bad layout techniques impose stray inductances in the circuit. The final assembly should use diodes, resistors and switches with the shortest possible leads. Circuit layout must be well designed using the smallest and widest tracks the positioning and safety distances allow. Magnetics should be coated since the movement of the core in the bobbin can slightly change the inductance resulting on voltage unbalance even after the switch stack trimming process.

C. Safety considerations

PCB layout must use appropriate safety distances for the voltage levels in the circuit. The dielectric strength of air is approximately 3 kV/mm and it is a good option as an isolator if the PCB uses chinks to assure dust deposits do not interfere with the isolation. FR4 PCB material has the impressive isolation of 20kV/mm meaning that high voltage tracks can move around in different layers on two layers PCBs with no problems. The transformer assembly can be done in many physical configurations. The authors opted to use windings separated by FR4 material as shown in the experimental results section. The usage of Polyester tape like Tecktape:160 that has an isolation of 4kV per layer is also a good option for transformers with windings assembled on top of each other. The isolation between primary and secondary windings of each gate transformer should support the greatest voltage on the switch stack.

D. Experimental trimming

As previously stated the turn off process should be experimentally trimmed. Using appropriate measurement equipments the trimming process should be initially done using a circuit in which the voltage does not exceed the rupture voltage for an individual device. This process assures that none of the switches will be damaged while the voltage unbalance is still in dangerous levels.

IV. DESIGN SAMPLE

The design sample presents the creation of a 1500V switch stack using 4 IRF740 mosfets with a fixed on-time around 150ns.

From the specifications and the chosen switch datasheet the designer has the following data.

V_{Zener} : 20V $\quad Q_C$: 63nC $\quad V_{DC}$: 36V

T_{ON} : 2.5us $\quad T_{Closed}$: 300ns $\quad M$: 180

Using the presented design methodology it is found the following inductors.

L_P : 2.23uH $\quad L_S$: 160nH

The coupled inductors were assembled using an EE20 Ferrite core as shown in Fig. 7. Since the authors did not have smaller cores like the EE14 that was the indicated for this specific case, the secondary inductance was increased to about 1uH in order to have at least 4 turns and improve the energy balance among the drivers.

The driver side switch is an IRF740 using a MC33151P driver, the output diodes are 1N4936, the zener diodes are 1N4747A and the load resistance is a 22Ω resistor is series with a 200Ω trimming potentiometer from *BOURNS*. A large electrolytic capacitor was used on the driver side power source in order to maintain the voltage level while storing

energy in the driver. The resistances in parallel to each of the switches are 235kΩ that support a maximum power of 0.5W.

V. EXPERIMENTAL RESULTS

The high voltage switch assembly is shown in Fig. 7.

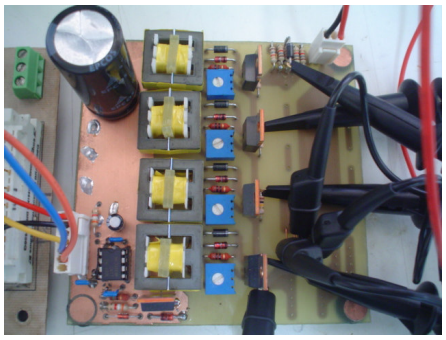

Fig. 7 High Voltage Fixed on-time switch prototype.

To test the developed switch the authors used a step-down converter with resistive load draining about 5A when closed. The resistance to achieve 5A at 1500V is 300Ω and was obtained using 5 resistances of 1500Ω in order to minimize the parasitic inductance and improve di/dt in the circuit.

The circuit was tested using a TMS320LF2401A Digital Signal Controller (DSC) to generate the desired pulse profile. It is a burst like control signal containing 75 pulses at 100kHz each 300ms. It was created in order to validate the speed of the switch and allow both static and dynamic voltage balance verification.

Fig. 8 presents the gate voltage of the driver side switch and the current flowing through the primary side inductors.

Fig. 9 present the second operational stage in which the primary side current falls and the secondary rises. It is worth noting the secondary does not assume the primary side current instantaneously due to parasitic inductances in the coupled inductors, other discrete components and printed circuit board. The driver side switch drain-source parasitic capacitance charging process that occurs when it is opened also contributes to slow down this process.

It is also verifiable through Fig. 9 time scale that the closing process, which takes about 10ns, is occurring while the current is still rising. It means the turn on speed can be improved if the parasitic elements were minimized.

Gate voltage and secondary side inductor current are presented in Fig. 10. As previously stated, the expected behavior is strongly damaged by the parasitic effects but the fixed on time was achieved.

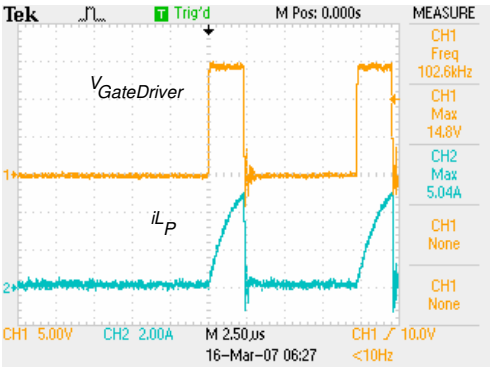

Fig. 8 Driver side gate voltage and primary side current.

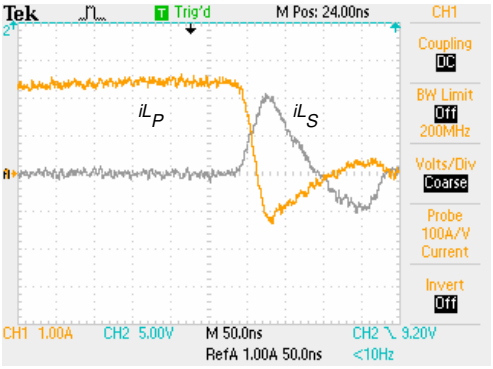

Fig. 9 Current behavior during the transition from energy storage to energy delivery operational stages.

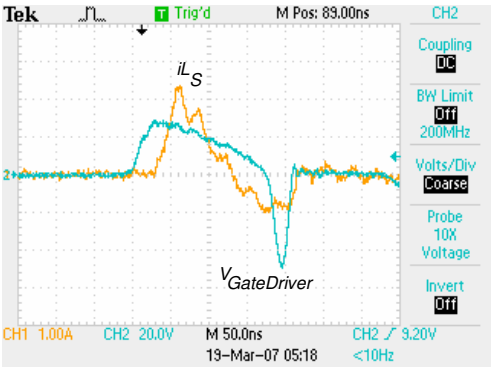

Fig. 10 Gate voltage and secondary side inductor current, which has a small delay (about 35ns) due to the probe amplifier.

In order to validate both static and dynamic voltage balance Fig. 11 presents the drain voltage of each switch in the stack referenced to the emitter of the switch stack after the trimming process. Captures at higher voltages are not presented due to the number of high voltage probes available.

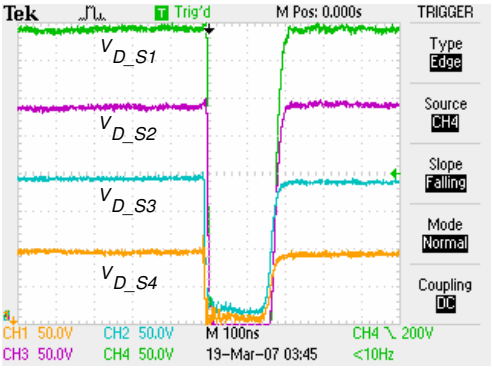

Fig. 11 Static and dynamic voltage balance validation.

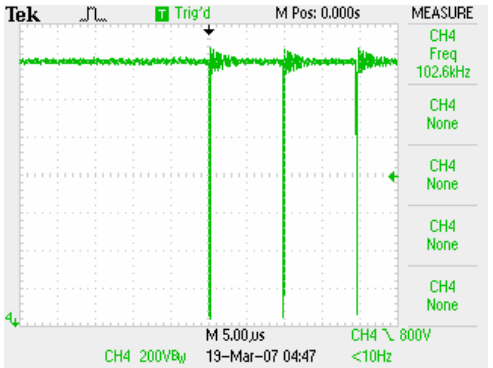

Fig. 12 Switch voltage along three switching cycles.

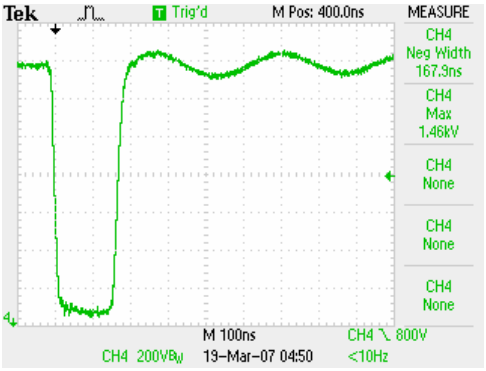

Fig. 13 Switch voltage during one fixed on-time transient.

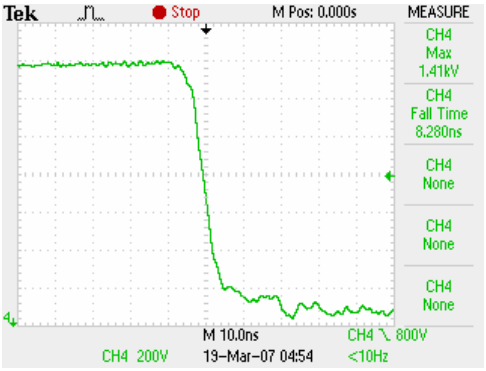

Fig. 14 Switch voltage fall-time.

CONCLUSION

The development of a low cost High Voltage Fixed On-Time Power Switch was presented and experimentally verified. Ultra-fast turn-on, fixed on-time and static and dynamic voltage sharing were achieved. It was verified that the presented structure is a good alternative to obtain a High Voltage Fixed On-Time device using small power MOSFETs.

The authors verified that lowering the voltage and current capability of the discrete devices used on the switch stack produces faster fall/rise times. In case the designer needs a high current switch, the usage of low power devices in parallel should be considered.

Due to the characteristics of the developed device, it can be used in biomedical research and many other applications that need short high voltage pulses. "Cells membrane electroporation for drug delivery in cancer therapy", "Bacterial decontamination of liquids with pulsed electric fields" and "Human cells apoptosis induced by high intensity pulsed electric fields" are some of the research projects being carried in the area of Biomedical research that can benefit from the information in this article.

Future studies will focus on the study of the magnetics in order to minimize parasitic effects and on the consideration of such non-idealities on the developed circuit. The extension to higher voltage levels and the usage of paralleled small power devices in order to improve speed, current capability and circuit condensation will also be verified.

ACKNOWLEDGEMENT

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