# DIGITAL CONTROL OF A HALF BRIGDE NEUTAL POINT THREE PHASE PWM INVERTER IMPLEMENTED IN A TMS320F2812 DSC

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***Abstract* – This paper presents the design and implementation of the digital instantaneous averaged values control for output voltages of the half bridge neutral point three phase inverter. All needed block models for the design of the control are shown, as well as the project methodology of frequency response control based. The transfer functions of circuit blocks, the controller's bode diagram and open-loop system will be presented. Experimental results of control's performance completes the paper.**

***Keywords* – Digital Control, DSC, Three Phase Inverter.**

## I. INTRODUCTION

The possibility of use Digital Signal Controllers (DSC) to control switch-mode converters is growing altogether the processing capacity and semiconductor integration capability. The use of digital controller offers many advantages, like more flexibility in code modification; less sensibility to noise and aging effect; and allows the implementation of complex algorithms that can't be done in analog controllers. However, is necessary a careful signal conditioning before the digital signal conversion. Sampling time delay, resolution of A/D converter, word length of DSC and instructions cycle time are disadvantages over analog control. Nowadays, control optimized DSC's deliver high performance, great code efficiency and optimal peripheral integration for digital control. Presents too, high level on-chip integration to deliver system cost reduction, and powerful computational abilities that enable software innovation.

There is many ways to control the output voltage of inverters. The most simple is control of the RMS value of output voltage, changing the amplitude of a sinusoidal reference. The response time in this kind of controller is about some reference's cycles [1], presenting low performance to non-linear loads and transient loads. The repetitive control [2, 3] changes the reference based in periodic output error. This controller has good regulation to non-linear loads, but need some output cycles to reach good results. The theoretical fastest controller is named Dead Beat [4, 5]. This controller present good responses but is very susceptible to plant variations, like load changes, complicating your use.

The project of digital controllers can be fulfilled by many different ways. But for all ways, is needed the acknowledgment of system's plant and the project specifications. This paper will present the step-by-step design of a digital instantaneous controller, the transfer functions of circuit elements. Experimental results will be presented too.

## II. CIRCUIT PRESENTATION

The basic schematic of three phase inverter is well known in literature and presents a neutral point that allow neutral current flow in presence of unbalanced signals, unbalanced loads or signals with harmonic content. Figure 1 shows the three phase inverter power schematic. When the system had an analog output voltage controller, the simplified bloc diagram has the configuration presented in figure 2. Since all three phases have independent controllers, they will present the same blocs with identical characteristics. So, the controller design can be made to one phase and replicated to other phases without any extra consideration.

## III. CONTROL DIAGRAM GENERAL VIEW

Since you want to do a digital controller, some changes need to me made in the control block diagram. A particularity of digital systems is the necessity of convert analog signals in discrete signals to use them internally in DSP. Thus, appear in the diagram, samplers, zero order holders and converter gains blocks. To conclude the structure transfer from analog to digital, it's needed anti-aliasing filters, that have the purpose of limiting the frequency spectrum of sampled signal, avoiding sub sampling and aliasing, that can cause a wrong interpretation of the sampled data.

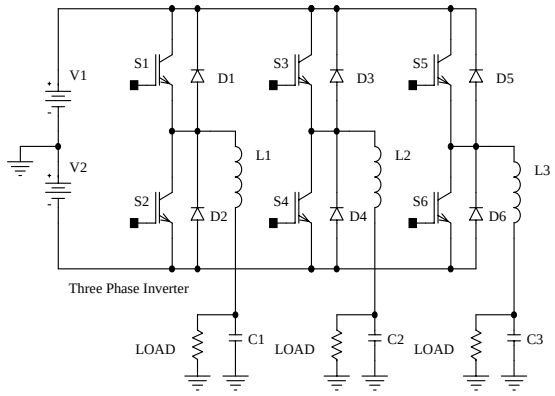


Fig 1. Three phase inverter power scheme.

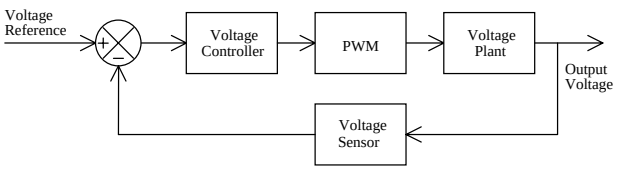


Fig 2. Block diagram with analog controller

The filter cutoff frequency need to be at least twice the sampling frequency, according to Nyquist theorem. More information about anti-aliasing filters can be found in references [6, 7]. Adding needed filters and converters, it's get the block diagram presented in figure 3.

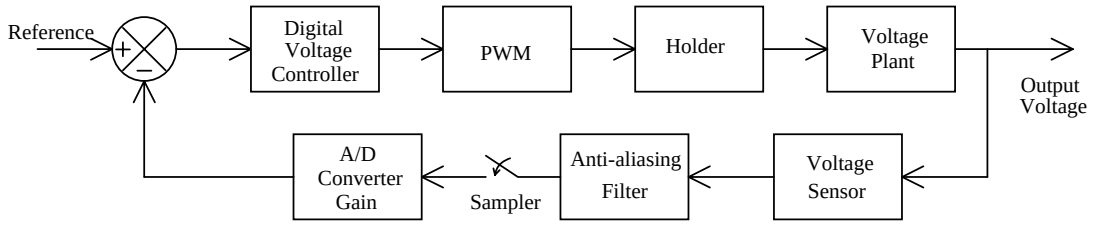


Fig. 3. Single phase block diagram of digital voltage controller.

## IV. DSC TMS320F2812

Before designing the controller, it's need to know the device that will be used to implement the controller. Spectrum Digital provides a kit called eZdsp to TMS320F2812 DSC, from Texas Instruments. Some characteristics of this DSC board are:

- Operating frequency: 150MHz;
- JTAG Boundary Scan Support;
- High performance 32 bits CPU;
- 16 channel 12-bit Analog/Digital converter;
- 3x 32-bit timers;
- PWM module, up to 16 outputs.
- Serial port peripheral;
- Up to 56 pin general purpose I/O;

The controller design will consider the characteristics of DSC, allowing better representation of real system.

## V. CONTROLLER DESIGN

As proposed by Tomaselli [8], the controller design is composed by two fundamental subparts. First, to get a mathematic model that describes the process, gived by plant analysis, and second, the controller design, so that the system arrive the project requirements. So, the first step is to define the transfer functions of each block in figure 3.

### *A. Voltage plant model:*

It's be assumed that the switches act as controlled voltage sources, with averaged voltage value equal at average voltage in a switching period. Assuming that *V1 = V2 = E/2*, and evaluating the instantaneous averaged voltage value applied to output filter and applying the principle of small signal analysis, where the variables can be considered as a constant part plus a small variation, it's arrived (1), that is the voltage plant transfer function.

$$\frac{\Delta Vc_1(s)}{\Delta D(s)} = \frac{E}{L_1 \cdot C_1} \cdot \frac{1}{s^2 + \frac{1}{R_1 C_1} s + \frac{1}{L_1 C_1}} \tag{1}$$

### *B. PWM model*

The transfer function is obtained using the considerations presented by Barbi [6], notwithstanding, it's used a triangular carrier, with null low level and peak value equal to $V_T$. The duty cycle is defined as the time in that the control voltage (*Vref*) is greater that carrier value, according to (2).

$$\frac{D(s)}{V_{ref}(s)} = \frac{1}{V_T} \tag{2}$$

Where:

$$V_T = \frac{1}{2} . \frac{T_S}{T_{CK}} = \frac{1}{2} . \frac{f_{CK}}{f_s} \tag{3}$$

And:

- $T_S$ → Switching period;
- $f_S$ → Switching frequency;
- $T_{CK}$ → Processor clock period;
- $f_{CK}$ →Processor clock frequency.

### *C. Anti-aliasing filter model*

The anti-aliasing filter is inserted in design to reduce the amplitude of harmonic components greater that a half of sampling frequency, So, the anti-aliasing filter is an analog low pass filter that limits the sampled signal's frequency spectrum. Its transfer function is presented in (4).

$$\frac{Vout(s)}{Vin(s)} = \frac{fa/2}{s + fa/2} \tag{4}$$

### *D. A/D converter model*

To correctly digitalize the sampled signals, they must be conditioned to the levels compatible with DSC's needs. The DSP have an A/D converter that digitalizes analog signals with voltage range between 0V and up to a $V_{HI}$ voltage. Inside this range, the DSP convert the signal to a value of 0 and up to $2^n$, where "n" is the number of bits of the A/D converter. Equation (5) represents the A/D converter's gain.

$$K_{AD} = \frac{V_{DIG}}{V_{IN}} = \frac{2^n}{V_{HI}} \tag{5}$$

### *E. Voltage Sensor Model*

The voltage sensor is make by a voltage divider, so that voltage's relation is appropriate to A/D converter's needs. So, the voltage sensor is a gain *Kv*.

### *F. Voltage Controller Design*

Considering that the sampling frequency is high enough to allow the choice of a high anti-aliasing filter cutoff frequency so that is possible to consider that the filter will not change the system response in the interest frequency range, so the

anti aliasing filter can be suppressed of analysis. Moreover, the PWM block and voltage plant can be simplified to a unique block, generating the $G_v(s)$ function presented in (6).

$$G_V(s) = \frac{E}{V_T \cdot L_1 \cdot C_1} \cdot \frac{1}{s^2 + \frac{1}{R_1 \cdot C_1} s + \frac{1}{L_1 \cdot C_1}} \quad (6)$$

From the same way, the blocks of voltage sensor and A/D converter gain can be simplified to a unique block too.

In the next step, it's needed to convert the functions of continuous plane "s" to the discrete plane "z". This transformation it's made using the relation $z = e^{s \cdot Ta}$. So, $G_v(z)$ can be defined as follows:

$$G_V(z) = \mathbb{Z}\left\{ \frac{E\left(1 - e^{-sTa}\right)}{V_T \cdot L_1 \cdot C_1} \cdot \frac{1}{\left(s^2 + \frac{1}{R_1 \cdot C_1} s + \frac{1}{L_1 \cdot C_1}\right) s} \right\} \quad (7)$$

Evaluating the Z transform:

$$G_V(z) = \frac{E}{V_T}\left(1 - z^{-1}\right)\left\{ \frac{z}{z-1} - \frac{z^2 - z \cdot e^{-a \cdot Ta} \cdot \left[\cos\left(b \cdot T_a\right) + \text{sen}\left(b \cdot Ta\right)\right]}{z^2 - 2z \cdot e^{-a \cdot Ta} \cdot \cos\left(b \cdot Ta\right) + 2e^{-2a \cdot Ta}} \right\} \quad (8)$$

Where:

$$a = \frac{1}{2 \cdot R_1 \cdot C_1} \quad (9)$$

$$b = \sqrt{\frac{1}{L_1 \cdot C_1} - \frac{1}{4R_1^2 \cdot C_1^2}} \quad (10)$$

To allow the use of frequency response method design, it's must to do the conversion of $G_v(z)$ transfer function from "z" plane to "w" plane, using the bilinear transform, as shown in (11).

$$z = \frac{1 + {}^{Ta}\!/_{2}\, w}{1 - {}^{Ta}\!/_{2}\, w} \quad (11)$$

From where comes:

$$G_v(w) = \frac{E}{b \cdot V_T} \frac{Ta \cdot k_1 \cdot w^2 - \left(2b \cdot Ta \cdot k_2 + 2k_1\right) w + 4b \cdot k_2}{w^2 + k_3 \cdot w + 4k_2} \quad (12)$$

Where:

$$k_1 = \frac{1}{Ta} \cdot \frac{b \cdot e^{-2a \cdot Ta} + 2a \cdot e^{-a \cdot Ta} \cdot \sin\left(b \cdot Ta\right) - b}{1 + 2e^{-a \cdot Ta} \cdot \cos\left(b \cdot Ta\right) + e^{-2a \cdot Ta}} \quad (13)$$

$$k_2 = \frac{1}{Ta^2} \cdot \frac{1 - 2e^{-a \cdot Ta} \cdot \cos\left(b \cdot Ta\right) + e^{-2a \cdot Ta}}{1 + 2e^{-a \cdot Ta} \cdot \cos\left(b \cdot Ta\right) + e^{-2a \cdot Ta}} \quad (14)$$

$$k_3 = \frac{1}{Ta} \cdot \frac{4\left(1 - e^{-2a \cdot Ta}\right)}{1 + 2e^{-a \cdot Ta} \cdot \cos\left(b \cdot Ta\right) + e^{-2a \cdot Ta}} \quad (15)$$

The block diagram of the system, in the "w" plane is shown in figure 4, where $Fv(w)$ is the controller transfer function.

The next step is to get the voltage open loop transfer function that is presented in (16).

$$FTMA_V = F_V(w) \cdot G_V(w) \cdot H_V(w) \quad (16)$$

Where:

$$H_V(w) = Kv \cdot K_{AD} \quad (17)$$

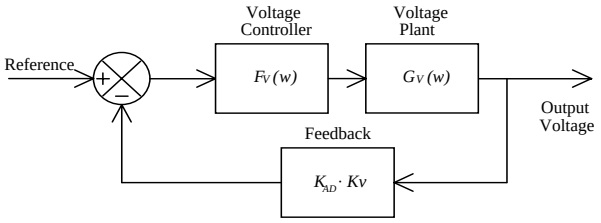


Fig. 4. Voltage loop – "w" plane

To execute the controller design beyond this point, it's need attribute numeric values to elements that take part of $FTMA_v$. So, based on the design parameters, is obtained the data presented in table 1.

**Table 1**
**Project parameters**

| | |
|---|---|
| fa = 100kHz | Sampling Frequency |
| fs = 50kHz | Switching Frequency |
| E = 640V | DC link voltage |
| Kv = 4.594mV/V | Voltage sensor gain |
| KAD = $2^{12}$/3.0 | A/D converter gain |
| $L_1$ = 566µH | Output filter inductance |
| $C_1$ = 5µF | Output filter capacitance |
| $R_1$ = 10kΩ | Load resistance (open circuit); |
| fck = 150MHz | DSP clock frequency |
| $V_T = \frac{1}{2} \cdot \frac{fck}{fs} = 1500$ | Peak value of triangular waveform form PWM |
| fc = fs/6 = 8.33kHz | FTMAv intended crossing frequency |

So:

$$FTMA_V = G_V(w) \cdot \frac{-1,2563 \cdot 10^{-7} \cdot w^2 - 758,2646 \cdot w + 1,5166 \cdot 10^8}{w^2 + 20,1777w + 3,55448 \cdot 10^8} \quad (18)$$

Before tracing a parallel between functions in planes "s" and "w", it's need to have in mind that the digitalization process generate a distortion in the response of system in "w" plane, mostly pronounced in frequencies near and above the sampling frequency. Figure 5 presents a comparison between the voltage plant transfer function $Gv(s)$, (6), and digitalized plant $Gv(w)$, (12). Can be noted that the frequency response presents conformity up to 3kHz, when the phase error go by substantial. This effect is caused by the zero added by digitalization process.

From $Gv(w)$ transfer function, it's be concluded that the system presents "non-minimal phase", with zeroes $w_{zp1} = -5.99 \cdot 10^6\ krad/s$ and $w_{zp2} = 2 \cdot 10^2\ krad/s$ and poles located in $w_{pp1} = (0.01 + j18.853)\ krad/s$ and in $w_{pp2} = (0.01 - j18.853)\ krad/s$. However the crossing frequency, where the gain is 0dB, is around 3,5kHz, lower that desired. The desired crossing frequency is six times lower that switching frequency, in other words, 8,33kHz.

To obey the null static error characteristic, it's needed that $FTMA_V$ presents an integrator in its loop. Including an origin pole, the $FTMA_V$ will have a decline rate of -60dB/dec at frequencies above the plant pole frequency, where is found the crossing frequency.

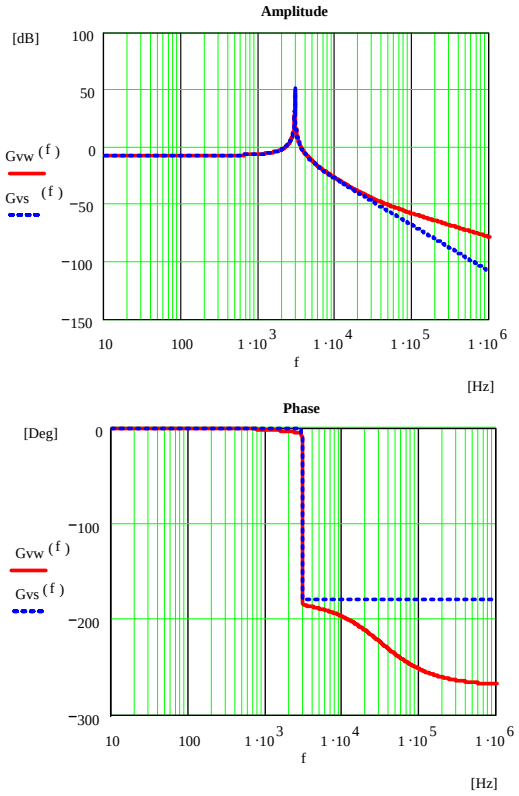


Fig 5. Frequency response of the system before and after digitalization

To obey the decline rate of -20dB/dec characteristic, it's needed the inclusion of two zeroes at some point lower that crossing frequency. An interesting choice is to allocate this zeroes in the same frequency of plant's zeroes (output filter poles), canceling its effect. Besides, is a common practice to include a pole above switching frequency, increasing the decline rate in high frequencies and, in this case, obtaining a higher attenuation in high frequencies and a better noise immunity. So, the transfer function of controller will be:

$$F_V(w) = k_{Fv}\frac{(w+\omega_{zc1})(w+\omega_{zc1})}{w(w+\omega_{pc1})} \qquad (19)$$

Where:

- $k_{Fv}$ is the controller gain;
- $\omega_{zc1} = \omega_{zc2} = 18.853\,krad/s$;
- $\omega_{pc1} = 40\omega_o = 754.134krad/s$;
- $\omega_o = 18.853krad/s$ is the output filter cutoff frequency;

Doing $k_{Fv} = 1$, the $FTMA_V$ will present -31.4 dB at crossing frequency. So, the $k_{Fv}$ gain must be chosen so that controller presents a gain of 31.4dB. So:

$$k_{Fv} = 10^{31,4/20} = 37,186 \qquad (20)$$

Betimes, it's determined:

$$F_v(w) = \frac{37,186w^2 + 1,40214\cdot10^6 w + 1,32172\cdot10^{10}}{w^2 + 754134w} \qquad (21)$$

Figure 6 presents the bode diagram of $FTMA_V$ without controller, of controller alone and of $FTMA_v$ with controller. The $FTMA_V$ with designed controller presents phase margin greater that 31,7°, obeying the desired design value.

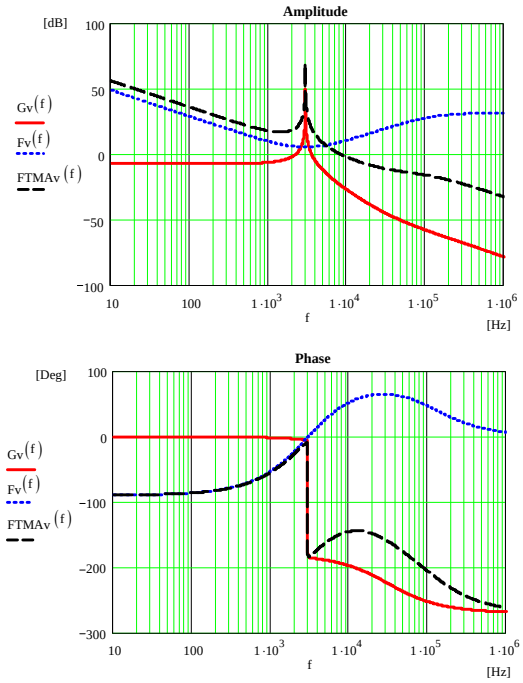


Fig 6. Controller influence in voltage loop.

Using *Fv(w)*, from (21), and the definition of (11) it's be determined *Fv(z):*

$$F_V(z) = \frac{9,3335z^2 - 15,4509z + 6,3944}{z^2 - 0,41923z - 0,58077} \qquad (22)$$

The transfer function of *Fv(z)* can be represented by yours input and output's parameters, as shown in figure 7.

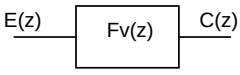


Fig 7. Block representation of voltage controller.

So:

$$F_v(z) = \frac{C(z)}{E(z)} = \frac{9,3335z^2 - 15,4509z + 6,3944}{z^2 - 0,41923z - 0,58077} \qquad (23)$$

Rewriting (23) in differences equation form:

$$c_{(k)} = 9,3335e_{(k)} - 15,4509e_{(k-1)} + 6,3944e_{(k-2)} + \\ + 0,41923c_{(k-1)} + 0,58077c_{(k-2)} \qquad (24)$$

## VI. EXPERIMENTAL RESULTS

To verify the designed controller, was build a three-phase inverter, with power output up to 4500VA, even as a signal conditioning board to interface with eZdsp board and a three phase rectifier with capacitive filter, to provide the CC link to inverter. The system has an auxiliary supply yet. Figure 8 presents the implemented system diagram. Even as the inverter have the loads connected to the neutral point, the input rectifier have too the neutral point connected to neutral point of source line. This connection assures that unbalanced loads will not unbalance the CC bus.

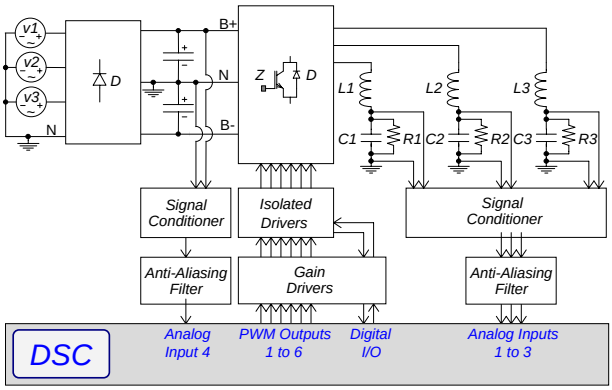


Fig. 8. System diagram.

Figure 9 shows a picture of the full system with all boards.

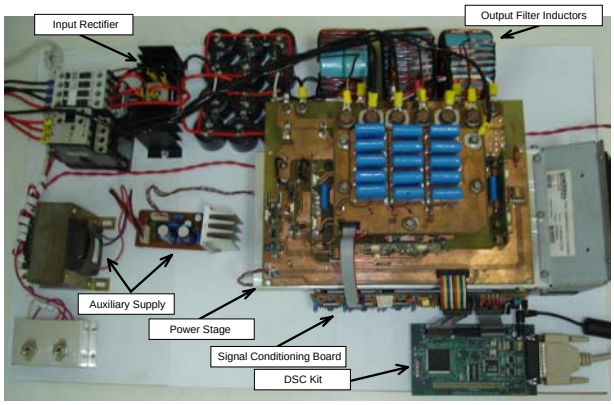


Fig 9. Developed system.

The most important waveforms was obtained in various operational conditions and will be presented as follow. Figure 10 presents the output voltage of inverter, referenced to neutral point, with no output load. The RMS value is 127V with 60Hz. It's evident the sinusoidal shape for all output signals and the peak value of 185V.

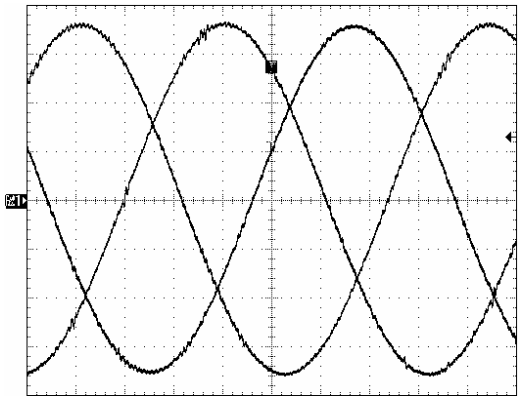

Fig. 10. Three-Phase output voltages – 127V
(50V/div, 2ms/div)

To verify the control dynamics and the behavior of power stage, was applied load steps, from 50% to 100% of nominal output power and observed the output voltage transient. Figure 11 shows the output voltage and output current to a load step change. Figure 12 presents in details the transient of voltage and current. Can be see that the instantaneous value of voltage is quickly controlled and the signal return to its correct value after a short time, confirming the sinusoidal comportment and the correct reference follow.

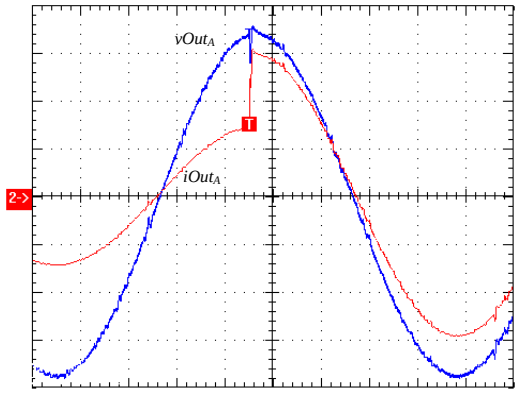


Fig.11. Load step change from 50% to 100% of nominal power
(50V/div, 10A/div, 2ms/div)

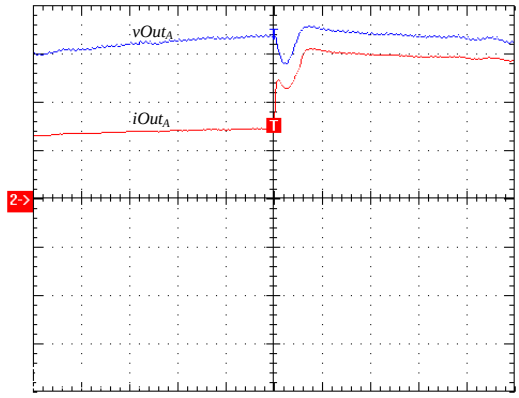


Fig. 12. Detail of load step change form 50% to 100%
(50V/div, 10A/div, 200µs/div)

To evaluate the dynamics in front of non-linear loads, was connected a three-phase non-controlled rectifier with capacitive output filter, presenting current crest factor equal to 3. Figure 13 shows output voltage and current of inverter to output phase "A", when the output power was 4,4 kVA. Can be observed the robustness of the controller, presenting low harmonic distortion even when the current is non-linear and assumes high peak values. In this condition, the output voltage was 150V RMS and the THD was 1,278%.

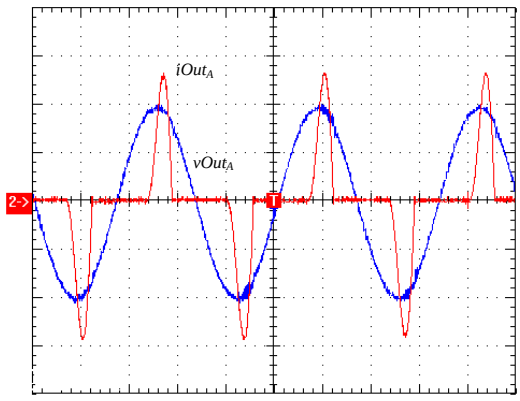


Fig. 13. Output voltage and current with non-linear load
(100V/div, 10A/div, 5ms/div)

Was used too a voltage reference with high harmonic content and was observed the output signal of inverter with this reference. Figure14 presents the output voltage when the reference was a triangular waveform, with 300V of peak value and 60Hz of frequency. Figure 15 demonstrate the comparative of harmonic content of reference and inverter output voltage. Can be see that there is a great coherency between the signals, even when the signal presents a high harmonic content.

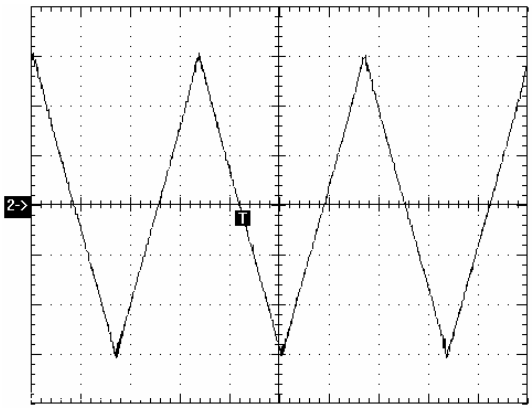


Fig.14. Inverter output voltage with triangular reference (100V/div, 5ms/div)

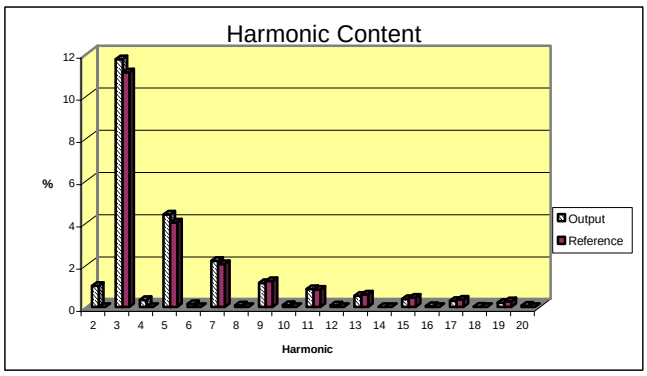


Fig. 15. Comparative of harmonic content to triangular waveform.

## VII. CONCLUSIONS

The controller design following the presented method is very simple because is based in frequency response to analog controllers, that is much known in literature.

Must be seen that plant's digitalization cause a phase and frequency distortion, as was shown in graphics of frequency response of continuous and digitalized systems. Beyond that, the specified phase margin only was arrived using a sampling frequency twice bigger that switching frequency. Increasing the sampling frequency, the phase delay caused by plant's digitalization was sufficiently minimized and the intended phase margin was reached. The controller performance was satisfactory and your capacity of reference follow is good even when the reference have a high harmonic content or when the load presents non-linearity and high crest factors. The calculus involved are quite simple and the equations have low complexity, ensuring a easy project methodology.

This paper is about domain technology. Its main contribution is in the implementation of this control technique in a new high performance processor and the experimental verification of the performance through the obtained results.

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