SINGLE PHASE ZVS PWM NPC INVERTER

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***Abstract* – This paper presents a zero-voltage, pulse width modulated, NPC inverter, with active voltage clamping using only two auxiliary switches. The structure is particularly simple and robust. It is very attractive for high-power applications, single or multiple phases, due to neutral point accessible at the NPC topology. Switching losses are reduced due to implementation of the simple active snubber circuit that provides zero-voltage-switching conditions for all switches, which includes the snubber auxiliary ones. When applied to NPC, the soft commutation allows high frequency commutation even for high voltage input, which reduces output filter size and improve the pass-band frequency. Its main features are simple modulation strategy, robustness, low weight and volume, low harmonic distortion of the output current and high efficiency. The principle of operation for steady-state conditions, mathematical analysis, and experimental results from a 1.5kVA laboratory prototype are presented.**

***Keywords* – NPC, Active Clamping, Soft Commutation, Multilevel Inverter.**

I. INTRODUCTION

With the objective of reducing the audible noise of the high power static inverters, increase the signal pass band, and also reduce the inverter size, by reducing the size of magnetic parts and filter elements, researchers are searching for solutions that could increase the switching frequency, without compromising efficiency and electromagnetic emissions.

Passive and active techniques have been proposed to be used in inverters to minimize commutation losses. The active solutions have a controlled auxiliary switch to achieve soft commutation that increases the overall system complexity [1]. The conventional passive techniques, like RCD snubbers, have the disadvantage to cause unbalance in the voltages at the switches in the NPC topology, where the voltage at the switches close to load becomes significantly higher compared to the switches close to DC-Link voltage [2]. Others passive techniques are variations of the traditional RCD snubber, like the Undeland and the Mc Murry circuits [3]-[7], which were developed to minimize this unbalance effect. The Undeland disadvantage is the high power losses, which lead to studies to regenerate this wasted energy, like the one proposed by Sperb [8] and Bendien [9]. The active solutions are based on ARCPI (Auxiliary Resonant Commutated Pole Inverter) or RLDC (Resonant DC Link Converter), where capacitors, inductors and switches provide an instant DC link shift that allows the switches to be closed at zero volts (ZVS) [10]-[12]. But, when these techniques are applied to NPC inverter, the number of additional switches makes it unfeasible.

The NPC static converter/ inverter is being widely used in medium voltage applications. That is because the amount of energy that needs to be processed is increasing. This converter is well suited for power distributions systems, motor drivers, active filters, and recently wind generation systems, when the input voltage could be higher compared to traditional two level inverters.

The NPC architecture allows the reduction of the voltage applied on each transistor, which in turn reduce the amount of voltage variation during commutation. Because of that, the operating frequency could be increased, and the inverter size could be reduced. Also, the voltage divisions between these transistors are optimized, as well as the output voltage harmonic content, when working as inverter [10]-[11].

This paper presents the theory and implementation of the active snubber such as in [1] applied to a three level NPC inverter [12]-[15]. It is organized such as follow: section II explains the operation principle of a three level NPC inverter with the auxiliary switches to provide the ZVS commutation; section III presents the operation stages and waveforms in the switches; a mathematical analysis is described at section IV; a design example, experimental results and conclusion are presented in sections V, VI and VII.

II. THREE LEVEL NPC ZVS PWM INVERTER

The proposed converter is shown in Figure 1. Q_1 and Q_4 are the main switches, responsible to apply the DC link voltage to load, Q_2 and Q_3 are the secondary switches, responsible to keep the null voltage at load, and Q_A and Q_B are the auxiliary switches. C_1 to C_4, C_A and C_B are the commutation capacitance.

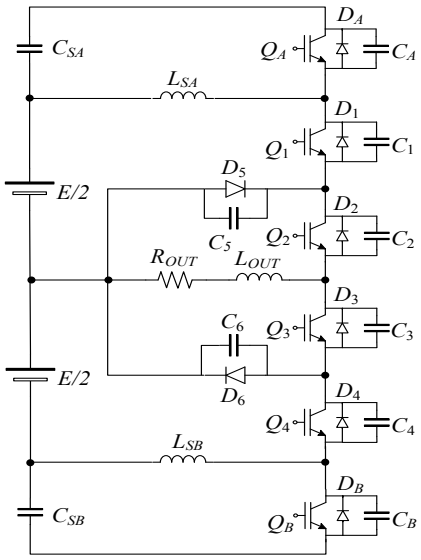

Fig. 1. Three level NPC ZVS PWM inverter.

The snubber circuit is constituted by two auxiliary switches, Q_A and Q_B, the anti-parallel diodes D_A and D_B, two small inductors, L_{SA} and L_{SB}, and two capacitors C_{SA} and C_{SB}. The capacitors are used for voltage clamping, and also to store the reverse recovery energy from D_5 and D_6. The inductors L_{SA} and L_{SB} control the di/dt on the diodes during reverse recovery. The auxiliary switches control the ZVS for all switches, including themselves. They work with constant pulse width and constant frequency at any load and modulation condition.

The linear modulation of the topology is not considerably affected by the auxiliary circuit because the voltage across the auxiliary capacitors vC_{SA} and vC_{SB} have small ripple and small amplitude when compared to DC link voltage. The modulation range is also maintained because the instantaneous output voltage (before the output filter) is the sum of the DC link voltage, and vC_{SA} and vC_{SB}.

III. OPERATION STAGES

To simplify the analysis, all components are assumed ideal; the circuit is operating in steady state condition and the reverse recovery characteristics of all diodes, except D_5 and D_6 are excluded. The output current is considered constant during switching period and in phase with the output voltage for a cycle period. The parameter E represents the DC link voltage, and vC_{SA} and vC_{SB} are the voltage across the clamping capacitors C_{SA} and C_{SB}. In the following paragraphs, the operation of the first half-cycle is described in details. For the second half cycle, negative, the stages are analogous, but using the switches Q_3, Q_4 and Q_B, and the passives C_{SB} and L_{SB}. The main operation stages are shown in Fig 2 and the main waveforms in Fig. 3.

First stage ($t_0 - t_1$): During this interval, the switch Q_2 is closed and the current pass through D_5 and Q_2, causing a null voltage across the load. At the same time, the auxiliary switch Q_A is closed applying vC_{SA} voltage to L_{SA} inductor. The current at this inductor increases according to (1).

$$iL_{SA} = \frac{vC_{SA}}{L_{SA}} \cdot t \tag{1}$$

Second stage ($t_1 - t_2$): This stage starts when switch the Q_A is blocked. The current $iLSA$ then charge the capacitor C_A from zero to $E/2 + vC_{SA}$ and discharge the capacitors C_1 from $E/2 + vC_{SA}$ to zero.

Third stage ($t_2 - t_3$): When the voltage across C_1 reaches zero, the diode D_1 is forward biased and the current iL_{SA} pass through it. At this moment, the switch Q_1 is commanded to turn-on. Because the voltage across the inductor L_{SA} is $E/2$, the inductor has the current decreased quickly. This stage ends when iL_{SA} invert its direction.

Fourth stage ($t_3 - t_4$): The current flowing through D_5 decreases and the current flowing through Q_1 increases. When current at Q_1 and L_{SA} reaches i_{OUT}, the reverse recovery at D_5 begins. The inductor L_{SA} limits the di/dt. This stage ends when D_5 finishes its reverse recovery phase.

Fifth stage ($t_4 - t_5$): When D_5 finishes the reverse recovery, the remaining current at L_{SA} inductor discharges C_A capacitor from vC_{SA} to zero and charges C_5 capacitor from zero to $E/2 + vC_{SA}$. This is also the moment when the load voltage changes from zero to $E/2 + vC_{SA}$. At the end of this voltage equalization, D_A conducts and the next stage begins.

Sixth stage ($t_5 - t_6$): The remaining current from L_{SA} flows through D_A and charges the capacitor C_{SA}. The current iL_{SA} decreases, according to equation 1. When iL_{SA} becomes equal to i_{OUT}, the current flowing through D_A is zero and Q_A transistor conducts, which is the beginning of the next stage.

Seventh stage ($t_6 - t_7$): When iL_{SA} is less than i_{OUT}, Q_A transistor conducts. The current iL_{SA} continues to decrease at and the current flowing through Q_A increases. The next stage begins when iQ_A is equal to i_{OUT}, and consequently iL_{SA} is zero.

Eighth stage ($t_7 - t_8$): The current iL_{SA} reverses its polarity and the inductor is charged according to (1). The current at Q_A is the sum of i_{OUT} and iL_{SA}. This stage finish when switch Q_1 opens.

Ninth stage ($t_8 - t_0$): When Q_1 opens, C1 is charged from zero to $E/2 + vC_{SA}$, and C_5 is discharged from $E/2 + vC_{SA}$ to zero. This stage ends when all capacitors voltages are equalized.

IV. MATHEMATICAL ANALYSIS OF THE CIRCUIT

A. Modulation Factor

The inverter output voltage is controlled by the modulation factor – *ma* – which is obtained through the relation between the peak value of the sinusoidal reference and the sawtooth waveform shown at Fig. 4 or the relation between the output voltage value, and half of the DC-link voltage, per (2).

$$ma = \frac{v_{REFpk}}{v_{SAWpk}} = \frac{v_{OUT}}{E/2} \tag{2}$$

According to Fig. 4 also, the following was defined for the duty cycle: For $D > 0$, the reference signal is greater than zero, the switch Q_2 is closed and Q_1 is being commanded. The instantaneous load voltage can be 0 or $+E/2$; For $D < 0$, the reference signal is lower than zero, the switch Q_3 is closed and Q_4 is being commanded. The instantaneous load voltage can be 0 or $-E/2$. The value range acceptable for D is -1 to 1, where -1 means 100% duty cycle and $-E/2$ applied to load, and 1 means 100% duty cycle and $+E/2$ applied to load.

The output voltage for one switching period is:

$$v_{OUT} = \frac{E \cdot D}{2} \tag{3}$$

From (3), it is obtained the duty cycle D:

$$D = \frac{2 \cdot v_{OUT}}{E} \tag{4}$$

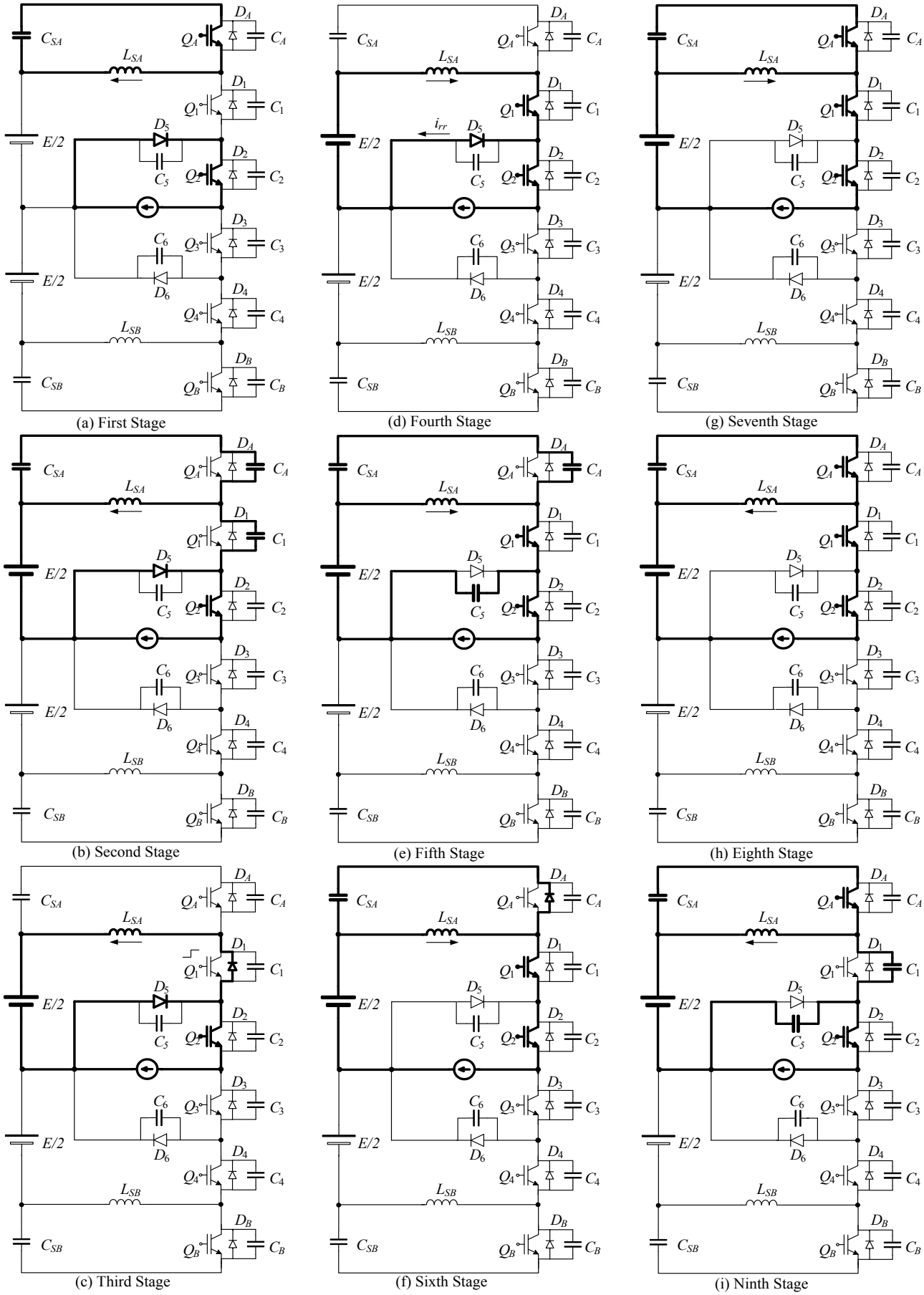

Fig. 2 Operation stages. (a) First stage ($t_0 - t_1$); (b) Second stage ($t_1 - t_2$); (c) Third stage ($t_2 - t_3$); (d) Fourth stage ($t_3 - t_4$); (e) Fifth stage ($t_4 - t_5$); (f) Sixth stage ($t_5 - t_6$); (g) Seventh stage ($t_6 - t_7$); (h) Eighth stage ($t_7 - t_8$); (i) Ninth stage ($t_8 - t_0$).

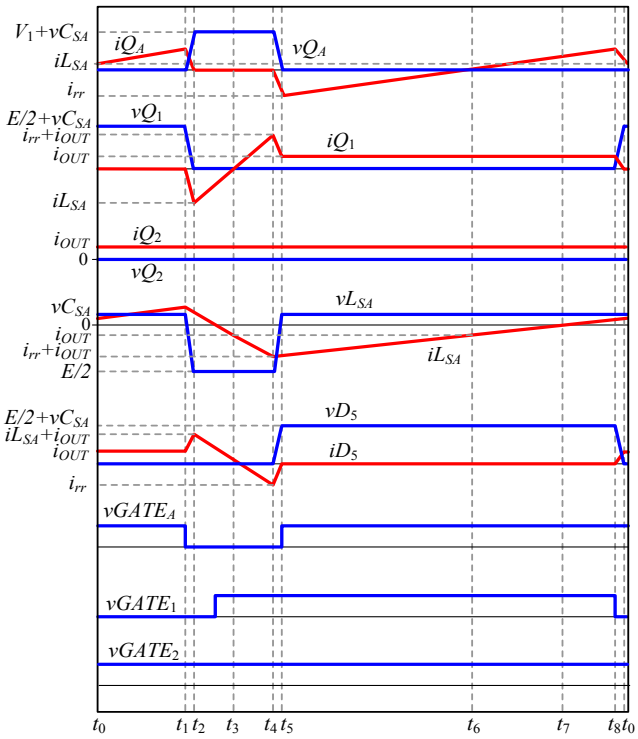

Fig. 3. *Main waveforms, upper side of the NPC.*

The inverter output voltage for an output period is given by

$$v_{OUT}(\omega t) = \sqrt{2} \cdot v_{OUTrms} \cdot \sin \omega t \tag{5}$$

where $\omega = 2 \cdot \pi \cdot f$, and f is the inverter output frequency. The maximum output voltage is given by (6).

$$v_{OUT_{pk}} = \frac{E \cdot ma}{2} \tag{6}$$

The root-mean-square (rms) output voltage is obtained from

$$v_{OUT_{rms}} = \frac{E \cdot ma}{2 \cdot \sqrt{2}} \tag{7}$$

The duty cycle can be obtained from (3), (4) and (7), i.e.,

$$D(\omega t) = ma \cdot sen\omega t \tag{8}$$

B. Soft Commutation

In order to guarantee the ZVS condition, the energy stored at inductor L_{SA} must be sufficient to charge and discharge the intrinsic capacitances C_A and C_1, respectively, during second stage. Thus, by inspection, for each switching cycle, the following condition should be met:

$$L_{SA} \cdot i^2{}_f \geq (C_{SA} + C_1) \cdot \left(\frac{E}{2} + vC_{SA} \right) \tag{9}$$

Assuming that $vC_{SA} << E/2$ them

$$i_{f_{MIN}} \geq \frac{E}{2} \cdot \sqrt{\frac{C_1 + C_{SA}}{L_{SA}}} \tag{10}$$

This equation shows the minimum i_f current to ensure soft commutation for a given cycle.

It's necessary to understand also, the voltage vC_{SA} behavior in order to determine the maximum voltage across the switches. The clamping voltage average current must be zero. Thus,

$$iC_{SA} = \frac{1}{T_S} \left[\int_{t_0}^{t_1} \left(\frac{vC_{SA}}{L_{SA}} t - i_{rr} - i_{OUT} \right) \cdot dt + \int_{t_5}^{t_8} \left(\frac{vC_{SA}}{L_{SA}} t - i_{rr} \right) \right] \tag{11}$$

where T_S is the switching period.

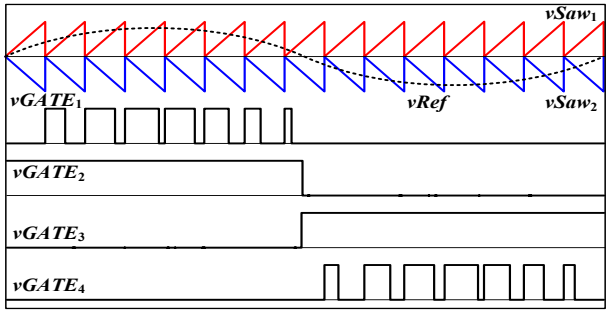

Fig. 4. *NPC Modulation strategy.*

Comparing to the switching period, the commutation time is very short. Then it could be simplified according to the following:

$$t_1 = t_5 = 0 \tag{12}$$

$$t_7 - t_5 = D \cdot T_S \tag{13}$$

$$t_8 = T_S \tag{14}$$

From (12) and (13), (11) can be written as follows:

$$iC_{SA} = \frac{1}{T_S} \left[\int_{D \cdot T_S}^{t_5} \left(\frac{vC_{SA}}{L_{SA}} t - i_{rr} - i_{OUT} \right) \cdot dt + \int_{0}^{D \cdot T_S} \left(\frac{vC_{SA}}{L_{SA}} t - i_{rr} \right) \right] \tag{15}$$

Solving the integral equation and considering $iC_{SA} = 0$, the steady state vC_{SA} is defined by

$$vC_{SA} = \frac{2 \cdot L_{SA}}{T_S} \left[i_{rr} + (1 - D) \cdot i_{OUT} \right] \tag{16}$$

Considering that the load current is a sinusoidal function, in phase with the output voltage, it leads to:

$$i_{OUT}(\omega t) = \frac{E \cdot ma}{2 \cdot Z_{OUT}} \cdot \sin \omega t \tag{17}$$

where *ma* was defined in (2) and Z_{OUT} is the load impedance

From (8), (16) and (17), it's obtained the capacitor voltage vC_{SA}:

$$vC_{SA}(\omega t) = \frac{2 \cdot L_{SA}}{T_S} \left[i_{rr} + \frac{E \cdot ma}{2 \cdot Z_{OUT}} \cdot \sin \omega t \cdot (1 - ma \cdot \sin \omega t) \right] \tag{18}$$

where i_{rr} is the diode D_5 reverse recovery peak current, defined by:

$$i_{rr} = \sqrt{\frac{4}{3} \cdot Qrr \cdot \frac{E}{2 \cdot L_{SA}}} \tag{19}$$

where Q_{rr} is diode reverse recovery charge.

The i_f current expression can be obtained from C_{SA} current behavior analysis:

$$i_f(\omega t) = \frac{vC_{SA}(\omega t)}{L_{SA}} \cdot T_S - i_{OUT}(\omega t) - i_{rr} \tag{20}$$

Combining the equations (17), (18) and (20), it's obtained the expression that represents the i_f current behavior.

$$i_f(\omega t) = i_{rr} + \frac{E \cdot ma}{2 \cdot Z_{OUT}} \cdot \sin \omega t - \frac{E \cdot ma^2}{Z_{OUT}} \cdot \sin^2 \omega t \tag{21}$$

By inspection, it could be observed that the critical condition will happen when $\omega t = \pi/2$. At this condition, (21) can be simplified to

$$i_{f\,MIN} = i_{rr} + \frac{E \cdot ma}{2 \cdot Z_{OUT}} \cdot (1 - 2 \cdot ma) \quad (22)$$

and them, according to (10) and (22), the soft commutation is guaranteed if

$$i_{rr} + \frac{E \cdot ma}{2 \cdot Z_{OUT}} \cdot (1 - 2 \cdot ma) \geq \frac{E}{2} \cdot \sqrt{\frac{C_1 + C_{SA}}{L_{SA}}} \quad (23)$$

V. DESIGN EXAMPLE

A. Specification

The main project specifications are shown at Table 1.

TABLE 1
Inverter Specifications

E = 900V	Nominal DC bus voltage
v_{OUTmax} = 300 Vrms	Output phase to neutral voltage
i_{OUTmax} = 12 Arms	Output current
P_{OUT} = 1.5kVA	Output power
f_S = 200kHz	Switching frequency
f = 60Hz	Output frequency
L_{OUT} = 2.5mH	Output filter inductance
C_{OUT} = 5µF	Output filter conductance
Cp = 1nF	Commutation capacitances

B. Auxiliary Inductors Calculation

The auxiliary inductors limit the *di/dt* during turn off of the main diodes, D_5 and D_6. The *di/dt* is directly related to the reverse recovery peak current, i_{rr}, of this diodes.

Considering a *di/dt* of 40A/μs, the inductors L_{SA} and L_{SB} can be obtained from the expression:

$$L_{SA,B} = \frac{E}{2 \cdot \frac{di}{dt}} = \frac{900}{2 \cdot 40} = 11{,}25\mu H \quad (24)$$

C. Load Impedance

It's obtained from

$$Z_{OUT} = \sqrt{60^2 + (2 \cdot \pi \cdot 60 \cdot 2{,}5m)^2} \cong 60\Omega \quad (25)$$

D. Diode Selection

The selected diode is the APT15D100K fast/ soft recovery diode from Advanced Power Technology. The selection was made considering the slow recovery characteristics, desired for the application. The diode characteristics are show in Table 2.

TABLE 2
Diode Characteristics

V_{rrm} = 1000V	Maximum Reverse Voltage
I_{AV} = 15A	Diode Average Current
Q_{rr} = 3µC	Reverse Recovery Charge

E. Switching Period

$$T_S = \frac{1}{f_S} = \frac{1}{200000} = 5\mu s \quad (26)$$

F. Reverse Recovery Current

The reverse recovery current is given using (19)

$$i_{rr} = \sqrt{\frac{4}{3} \cdot 3\mu C \cdot \frac{900}{2 \cdot 11.25\mu H}} = 12.65A \quad (27)$$

G. Clamping Voltage Capacitor Behavior

Based on calculated values for L_{SA}, i_{rr}, T_S and E, the behavior of C_{SA} capacitor voltage can be determined using (18), for a load from 10% to 100%.This behavior is shown in Fig. 5.

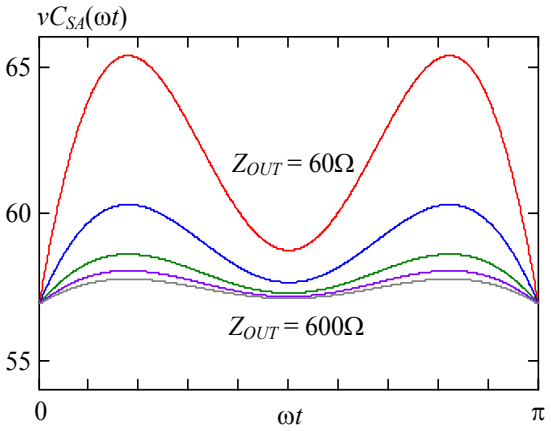

Fig. 5. Capacitor clamping voltage behavior.

H. Behavior of the Current i_f

The i_f current behavior, which is obtained from (22) is shown at Fig. 6.

According to it, the minimal i_f value occurs at π/2, for 60Ω load. To guarantee the ZVS condition in all load range, the minimum i_f value, which is obtained from (22), should be higher than the minimum required i_f, obtained from (10), thus:

$$i_{f\,MIN} = 12.65 + \frac{900 \cdot 0.95}{2 \cdot 60} \cdot (1 - 2 \cdot 0.95) = 6.23A \quad (28)$$

$$i_{f\,MIN} \geq \frac{900}{2} \cdot \sqrt{\frac{1n + 1n}{11{,}25\mu}} = 6A \quad (29)$$

$$6.23A \geq 6A \quad (30)$$

VI. EXPERIMENTAL RESULTS

A 1.5kW NPC ZVS PWM inverter prototype was developed to validate the proposed circuit. The simplified block diagram of this prototype is shown at Fig. 7. The main specifications and components are listed at Table 3.

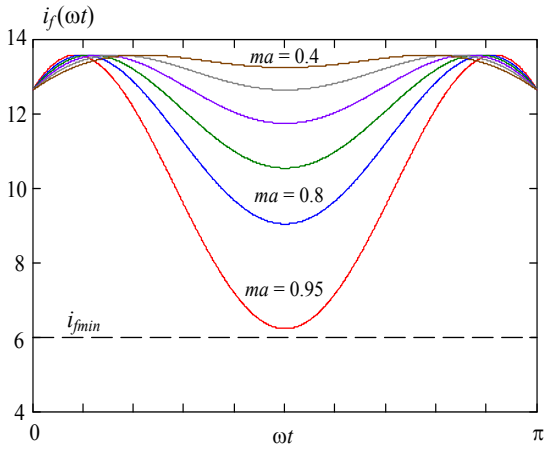

Fig. 6. i_f current behavior.

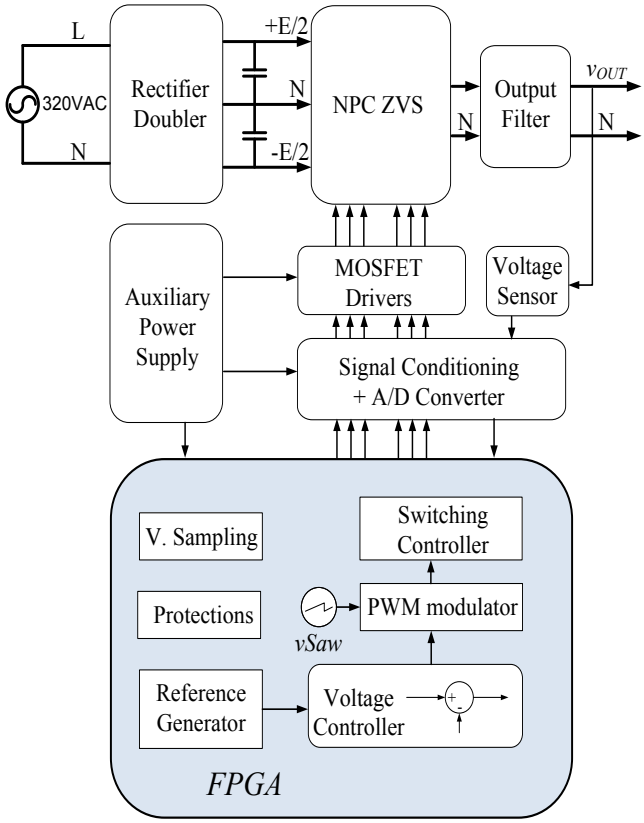

Fig. 7. NPC ZVS PWM Prototype.

TABLE 3
Prototype Specifications

$Q_1 - Q_4$, Q_A, Q_B	(STW42N65) Manufactured by ST
D_5, D_6	(APT15D100K) Manufactured by Advanced Power Technology
$C_1 - C_6$, C_A, C_B	(Component's intrinsic capacitance)
C_{S1}, C_{S2}	(12 x 470µF/400V; electrolytic capacitor)
L_{SA}, L_{SB}	(11.25µH, EE30/15/7 core)
L_{OUT}	(2.5mH; Output Inductor)
R_{OUT}	(60Ω; Output Resistor)

A. Experimental Waveforms

The main waveforms obtained from the laboratory prototype are show in the next figures. Figs. 8 to 11 show the voltage and current at Q_A, Q_1, Q_2, and D_5. It's observed that for all switches, including the auxiliary switch Q_A the ZVS condition occurs, according to theoretical analysis. The current at L_{SA} auxiliary inductor can be observed at Fig. 12. The output voltage and current, when operating in open loop, are shown in Fig. 13. The Fig. 14 shows the NPC efficiency for 220V and 127V output for the soft commutation technique (ZVS) and also the efficiency for the same topology, using the same switches, but without the auxiliary circuits (hard switching).

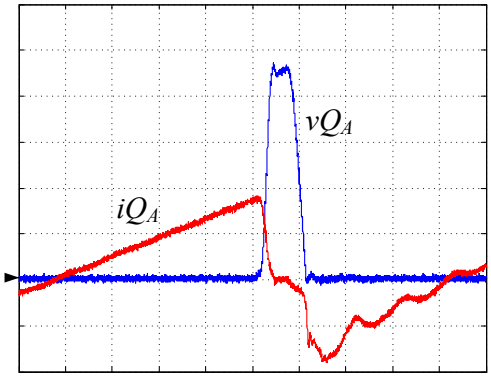

Fig. 8. Voltage and current in Q_A, including D_A and C_A. (100V/div, 2A/div, 400ns/div).

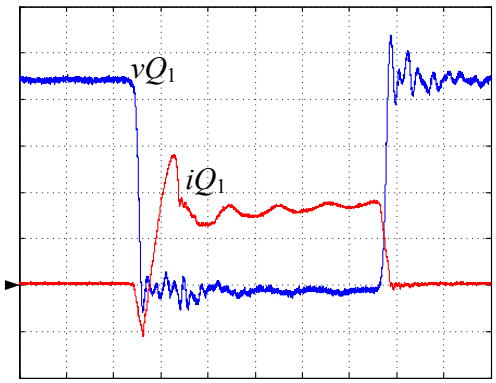

Fig. 9. Voltage and current in Q_1, including D_1 and C_1. (100V/div, 2A/div, 400ns/div).

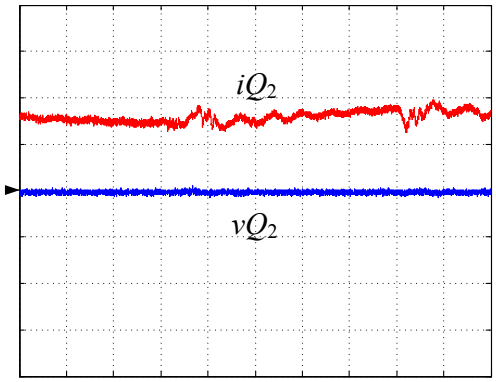

Fig. 10. Voltage and current in Q_2, including D_2 and C_2.(100V/div, 2A/div, 400ns/div).

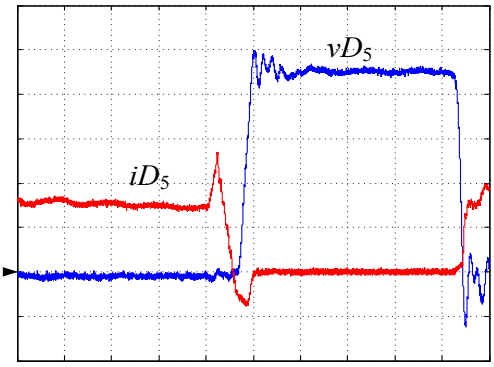

Fig. 11. Voltage and current in D_5, including C_5.(100V/div, 2A/div, 400ns/div).

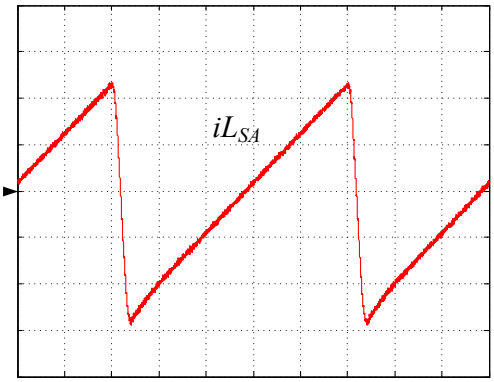

Fig. 12. Current in L_{SA},.(2A/div, 1µs/div).

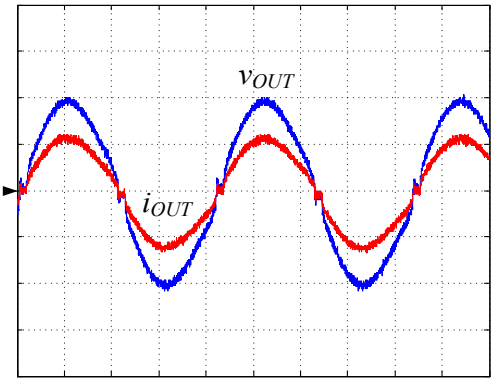

Fig. 13. Output voltage and current .(200V/div, 5A/div, 4ms/div).

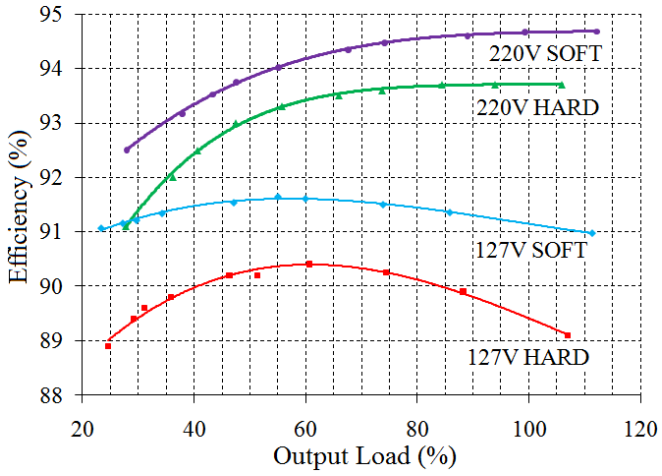

Fig. 14. Inverter efficiency for soft (ZVS) and hard commutation for 220V and 127V output.

VII. CONCLUSION

A PWM NPC inverter with active clamping using the reverse recovery energy of the freewheeling diodes to obtain ZVS commutation was developed. The main operation stages, the main waveforms and the experimental results were presented. The commutation losses were reduced due to the use of the simple snubber using only two switches, with simple control strategy, to assure soft commutation for all the switches in the circuitry.

The voltages across the switches were properly balanced under all load conditions, and the maximum currents observed were not significantly increased because of the auxiliary capacitors voltage, since this voltage is much lower compared to the DC-Link voltage.

The ripple observed at the output was very low because of the high commutation frequency, and because of the three-level topology, even for small output capacitors and magnetic. The pass-band frequency was also very high.

The overall efficiency, when compared to non ZVS NPC inverter, is higher for all output loads and voltage.

Possible applications for this circuit includes: wind generation inverters, Uninterrupted Power Supply (UPS), frequency converters, motor drive systems.

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