Three-Phase Hybrid Multilevel Inverter Based on Half-Bridge Modules

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***Abstract*—A novel three-phase hybrid multilevel converter is proposed for medium-voltage applications. The converter employs a conventional three-phase voltage source inverter (VSI) linking series connected half-bridge modules at each phase. With the proposed connection, a large portion of energy can be processed by the VSI by employing a single multi-pulse rectifier, while smaller power shares are processed within the half-bridge modules. Thus, the requirements for galvanically insulated dc sources are reduced. Modularity is naturally achieved. A modulation scheme for a four-level version is proposed and analyzed in detail. This scheme allows unidirectional power flow in all dc sources and, consequently, enables diode bridges to be employed in the rectification input stage for unidirectional applications.**

***Index Terms*—Hybrid converters, multilevel converters, PWM modulation, three-phase inverters.**

I. Introduction

POWER electronics applications requiring medium-voltage high-power converters have been steadily growing in fields such as power quality, power systems control, adjustable speed drives, uninterruptible power supplies (UPS), equipment testing, and co-generation. Most applications demand three-phase multilevel inverters. Various topologies have been proposed in the literature [1]–[16] to improve performance, adapt to requirements and avoid proprietary technologies.

Some topologies find more widespread use in industrial multilevel inverters. Among these are the neutral clamped converters, the capacitor clamped converter, the cascaded full-bridge converter, the hybrid voltage source inverter (VSI)/neutral point clamped (NPC) plus cascaded full-bridge converter, and the active NPC (ANPC).

The diode clamped converter, commonly named NPC, [1], [2], [10], [17] is a multilevel topology, which is widely employed in three-phase power conversion. There is a single dc-link that is split into two or more equal voltages which clamp the maximum voltage of the main switches through fast switching diodes. A high number of diodes is observed as the number of levels increase. Stabilization of the dc-link voltages for NPC converters with four or more levels is typically complex and is achieved by posing limitations at the output voltages or loads [18].

The capacitor clamped converter, also known as flying capacitor (FC) converter [5], provides the clamping of the voltages across the switches through capacitors. The stabilization of the clamping voltages is achieved due to the higher number of switching possibilities. Even though the number of clamping diodes is reduced, the number of capacitors increases rapidly with the number of levels, increasing the number of isolated voltage sensors.

The ANPC present a single dc-link for a three-phase inverter. The three-level version is introduced in [19] and shows improved performance regarding losses distribution. Five or more level ANPC topologies, which integrate some advantages of the NPC and FC converters, are analyzed in [7], [20], [21]. These topologies also present a single dc-link and the voltage clamping is achieved with the control of the dc-link and floating capacitors voltages. Thus, the single dc-link of the NPC and the flexibility for voltage stabilization of the FC are observed in these topologies. However, the number of active switches is increased or the voltage ratings of some of them must be higher. The capacitors precharge process is complex. The ANPC topologies are proprietary technologies [22], [23].

Cascaded H-Bridge (CHB) converters [3], [4] employ dc-side isolated series connected full-bridge modules at each phase allowing high modularity and the lower total number of components when compared to NPC, ANPC, or FC. These characteristics make them widely employed in industrial applications. As single-phase full-bridge modules are employed, the pulsating power in each dc-source presents a high low frequency ripple, increasing the storage effort. In addition, all modules and input rectifiers must process their share of the total power, increasing the demands for the rectifier stage transformers. Furthermore, the CHB is proprietary technology for many applications [1], [4], [24]–[26].

Cascaded half-Bridge (C1/2B) converters [27]–[31] employ half-bridge modules connected in series instead of the full-bridge ones. These converters are an alternative to the conventional cascaded full-bridge converters. The modular multilevel converter (MMC or M2C) [27]–[30] employ series connections of pairs of half-Bridge modules. These modules are connected in double-Y forming a three-phase system and the capacitors of dc links do not need isolated dc supplies [27], [28] since

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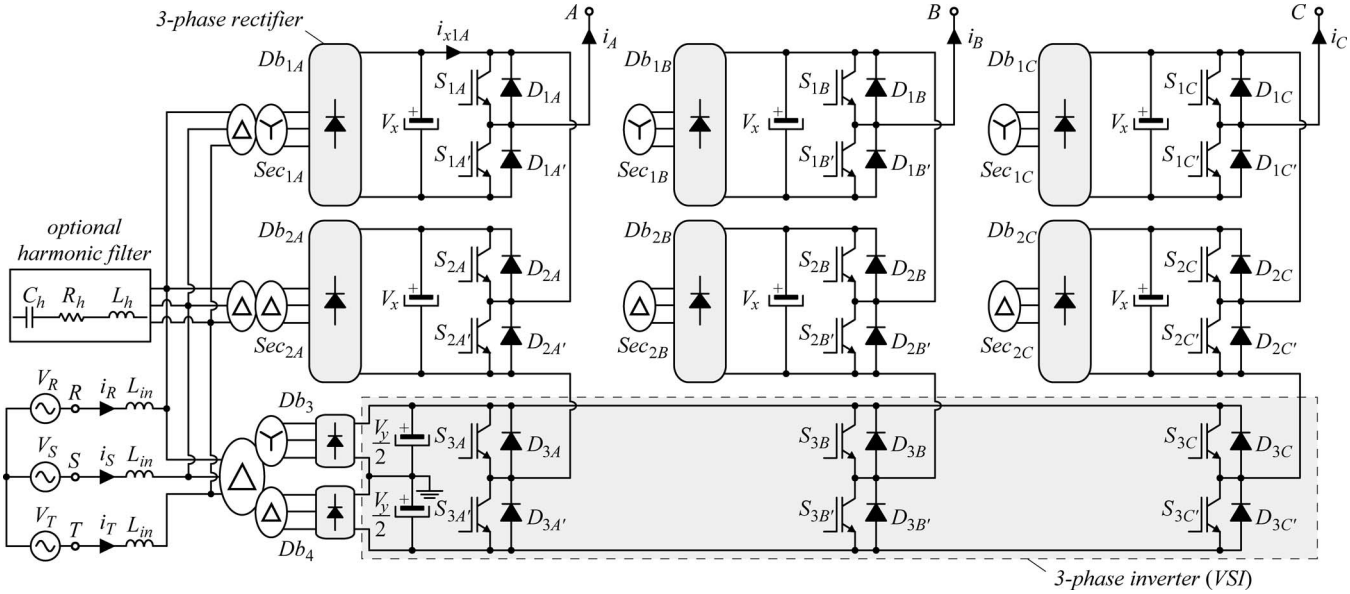

Fig. 1. Circuit schematic of the proposed hybrid multilevel converter employing half-bridge modules and a three-phase inverter. Further pairs of half-bridge modules can be connected in series at each phase-leg. The three-phase inverter can be replaced by other three-phase voltage source inverter topologies, for instance, an NPC converter. With an NPC 3-phase inverter five levels in the output phase voltage is reached with the symmetrical version.

the voltage across each half-bridge module dc-link capacitor can be actively controlled. The C1/2B converter [31] uses an alternative connection of half-bridge modules to eliminate the output dc level. The three-phase system is reached through a Y connection. The modules are also connected in pairs and the converter is able to provide just odd levels in the output phase voltages. This type of converter requires a higher number of insulated dc sources for the same number of levels of a CHB. However, lower active power levels are processed in the dc sources.

Hybrid topologies employing three-phase two-level VSI or NPC cascaded in each phase with series connected H-bridge modules (HCHB) have been proposed [8], [12], [32]–[34] as an alternative to the CHB. The number of components can be the same as for the CHB given the same number of voltage levels, while the three-phase converter can be directly fed without insulation. Thus, the requirements for the insulation transformers and for the main capacitive dc-link storage are lessened. Both HCHB and CHB have their asymmetric versions [12], [35], presenting advantages and drawbacks depending on the specific application and available switch technology. Hybrid topologies are mainly proprietary technology as well [32], [34].

This work presents a novel hybrid topology, here named Hybrid Cascaded Half-Bridge converter (HC1/2B), that makes use of a three-phase inverter (shown as a VSI in Fig. 1), where each output is series connected to a pair, or multiple pairs (cascade), of half-bridge converters connected with inverse polarity as shown in Fig. 1. There, the special connection of the half-bridge modules [31] guarantees that no dc level is observed at the output voltages. In the symmetrical version the modularity is preserved. The connection of the 12-pulse rectifier that generates the isolated dc sources (cf. Fig. 1) leads to low-input current harmonics and well-distributed current efforts for the rectifying diodes and windings of the transformers. Even though the number of insulated sources is increased, for the same number of voltage levels as for the CHB or HCHB, the proposed converter lowers the ratings of these devices since the average current that is drawn from each six-pulse rectifier feeding a half-bridge module is lower when compared to an H-bridge-based converter; thus, higher power levels can be achieved for a given transformer/rectifier technology.

The possible operation modes for the proposed HC1/2B are discussed in Section II, where the asymmetric versions of the topology are addressed and the symmetric four-level converter is presented in detail. Unidirectional power flow is required in many applications, such as high power UPS, co-generation, and others. In this context, the operation of the converter is optimized to achieve unidirectional power flow in all dc sources and, thus, reduce costs associated to bi-directional rectifiers. A modulation scheme is presented in Section III to achieve this goal. Based on the proposed modulation, the output voltage is analyzed in Section V regarding its harmonic spectrum and total harmonic distortion (THD). The theoretical analysis is verified in Section VI through experimental results based on a four-level inverter prototype.

Circuit simulations of the complete four-level converter employing the 12-pulse rectifier (cf. Fig. 1), dc voltage sources maximum ripple $\Delta V_o \leq 4\%$, grid-side input inductors $L_{in,p.u.} \cong 5\%$ and transformer leakage inductances of $L_{\sigma,p.u.} \cong 0.2\%$ have been carried out. The inverter load was kept constant regardless the modulation index. Two ac-grid operating conditions have been analyzed, namely: 1) balanced grid voltages; and, 2) grid supply voltages presenting unbalances of $\pm 3\%$. The achieved THD values are presented in Fig. 2. Ac-grid unbalances lead to higher distortion, including triplen harmonics, and different RMS current values in each phase. The harmonic distortion may be further reduced with the use of an appropriately sized filter. The input phase currents and their spectrum for the LM and HM modulation are shown in Fig. 2 for both grid conditions. Fig. 2(a) presents the input

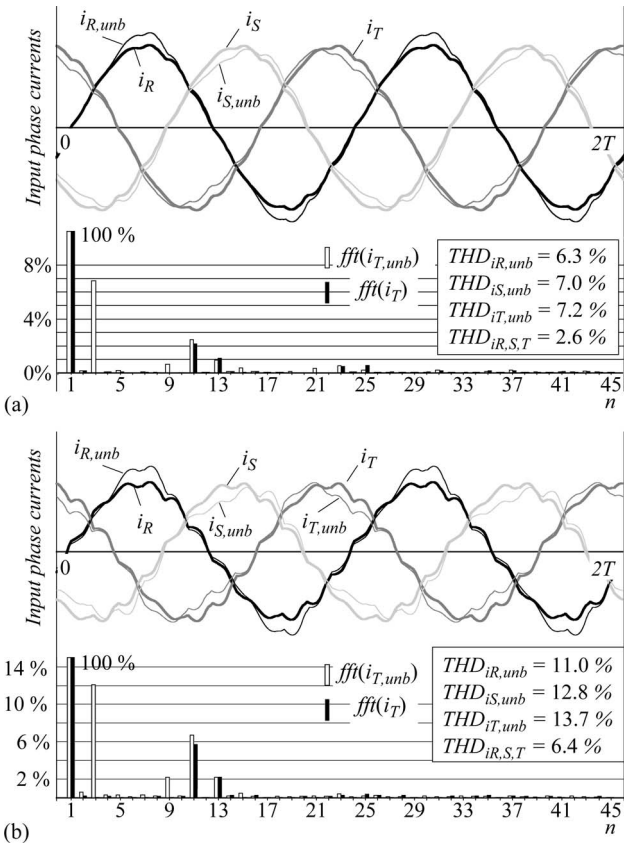

Fig. 2. (a) Input phase currents and phase T spectrum for LM modulation with modulation index $M = 0.5$. (b) Input phase currents and phase T current spectrum with respect to the fundamental current RMS amplitude for HM modulation with $M = 0.9$. Simulation conditions: dc voltage sources maximum ripple $\Delta V_o \leq 4\%$, inductors $L_{in,p.u.} \cong 5\%$ and transformer leakage inductances of $L_{\sigma,p.u.} \cong 0.2\%$. Grid supply voltages unbalances of $\pm 3\%$ (subscript unb) and 0%.

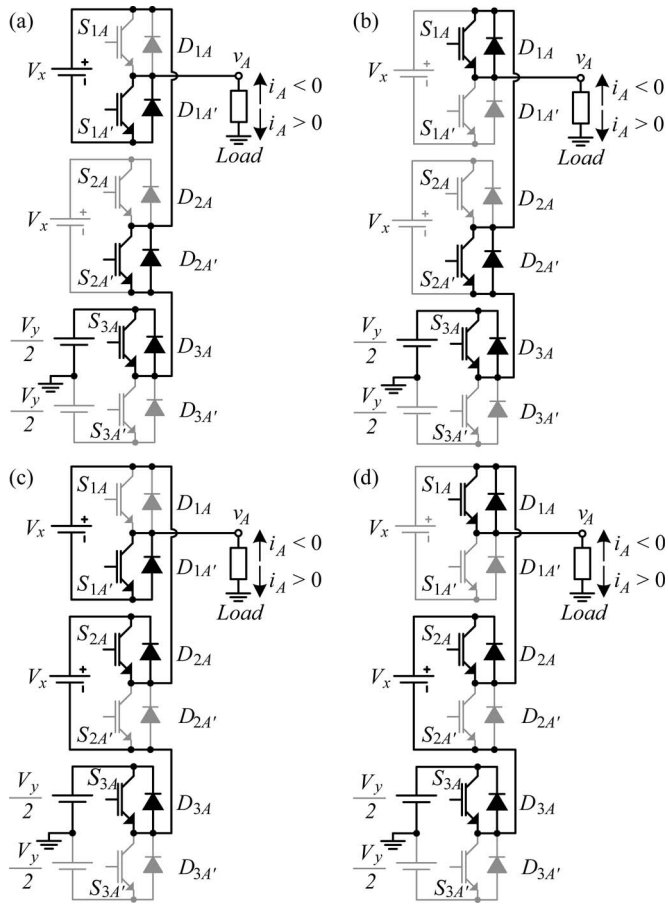

Fig. 3. Operation stages for a phase-leg of the proposed hybrid multilevel converter employing half-bridge modules for a positive output voltage. Switching stages are: (a) $S_{1A'}$, $S_{2A'}$ and S_{3A} are on and $v_a = V_y/2 - V_x$; (b) S_{1A}, $S_{2A'}$ and S_{3A} are on and $v_a = V_y/2$; (c) $S_{1A'}$, S_{2A} and S_{3A} are on and $v_a = V_y/2$; (d) S_{1A}, S_{2A} and S_{3A} are on and $v_a = V_y/2 + V_x$. The output voltage v_a is referred to the virtual reference shown in the center point of V_y source.

currents for LM modulation with modulation index $M = 0.5$ and Fig. 2(b) shows the same variables for HM modulation with modulation index $M = 0.9$. The same amount of energy is processed by each half-bridge cell under all operating conditions. The 12-pulse rectifier that feeds these modules does not have its performance degraded by changes in the modulation pattern. This is achieved because the 12-pulse rectifier is actually split into two parts, one that feeds the two-level VSI and the other, whose secondary supply energy for all half-bridge modules. Therefore, each part of the 12-pulse rectifier operates with balanced processed powers, thus, leading to the same behavior of a conventional 12-pulse rectifier supplying two secondaries with balanced loads.

II. Multilevel Operation

The following assumptions are made for the analysis: 1) the switching devices are ideal; 2) the dc sources are constant positive voltages; 3) parasitics are neglected; 4) the virtual center point of the VSI's dc-link (drawn in Fig. 1) is assumed as reference for the voltages. Considering a phase-leg composed of a pair of half-bridge modules and a phase-leg of the VSI, the possible operation stages of the proposed converter are depicted in Fig. 3 for phase A positive values. It is observed that the output voltage v_A can assume six different values, which are given for v_o, with $o = A, B, C$, in Table I. These output voltage levels depend on the dc sources voltages V_x and V_y and on the states of switches S_{jo} and $S_{jo'}$, with $j = 1, 2, 3$. Based on these results, the HC1/2B can be operated with a number of levels N_{level} varying from four to six given that

$$N_{level} = \begin{cases} 4, & \text{if } V_{\rm x} = V_{\rm y} \\ 5, & \text{if } V_{\rm x} = V_{\rm y}/2 \\ 6, & \text{if } V_{\rm y} \neq V_{\rm x} \neq V_{\rm y}/2. \end{cases} \quad (1)$$

Based on the possible operation stages for a phase-leg and the considerations given in Table I, the available space vectors can be found as shown in Fig. 4(a) for a four-level HC1/2B employing symmetric dc sources with $V_y = V_x$. The resulting state space is a composition of the vectors generated by the VSI with the allowable combination of vectors generated by the half-bridge cascades. This is highlighted in Fig. 4(b) for the symmetric case where $V_y = V_x$ and in Fig. 4(c) for the asymmetric case where $V_y > V_x$. Within each half-bridge space it is not necessary to switch the VSI state to generate any voltage vector contained in it. It is seen in Fig. 4(c) that relatively increasing the dc voltage for the VSI expands the

TABLE I

RESULTING OUTPUT PHASE VOLTAGE (v_o, WITH $o = A, B, C$) AS A FUNCTION OF THE SWITCHING STATES AND OF THE DC SOURCES VALUES V_x AND V_y, WHERE s_{jo} ($j = 1, 2, 3$) CORRESPONDS TO THE STATE OF SWITCH S_{jo} AND $s_{jo'} = \overline{s_{jo}}$. (SWITCH ON: 1, SWITCH OFF: 0.)

s_{1o}	s_{2o}	s_{3o}	v_o	Case 1 $V_x = V_y = V_{cc}$	Case 2 $V_x = V_y/2 = V_{cc}$	Case 3 $V_x = V_y/3 = V_{cc}$
0	0	0	$-V_x - \frac{V_y}{2}$	$\frac{-3V_{cc}}{2}$	$-2V_{cc}$	$\frac{-5V_{cc}}{2}$
1	0	0	$-\frac{V_y}{2}$	$\frac{-V_{cc}}{2}$	$-V_{cc}$	$\frac{-3V_{cc}}{2}$
0	1	0	$-\frac{V_y}{2}$	$\frac{-V_{cc}}{2}$	$-V_{cc}$	$\frac{-3V_{cc}}{2}$
1	1	0	$V_x - \frac{V_y}{2}$	$\frac{+V_{cc}}{2}$	0	$\frac{-V_{cc}}{2}$
0	0	1	$-V_x + \frac{V_y}{2}$	$\frac{-V_{cc}}{2}$	0	$\frac{+V_{cc}}{2}$
1	0	1	$+\frac{V_y}{2}$	$\frac{+V_{cc}}{2}$	$+V_{cc}$	$\frac{+3V_{cc}}{2}$
0	1	1	$+\frac{V_y}{2}$	$\frac{+V_{cc}}{2}$	$+V_{cc}$	$\frac{+3V_{cc}}{2}$
1	1	1	$+V_x + \frac{V_y}{2}$	$\frac{+3V_{cc}}{2}$	$+2V_{cc}$	$\frac{+5V_{cc}}{2}$

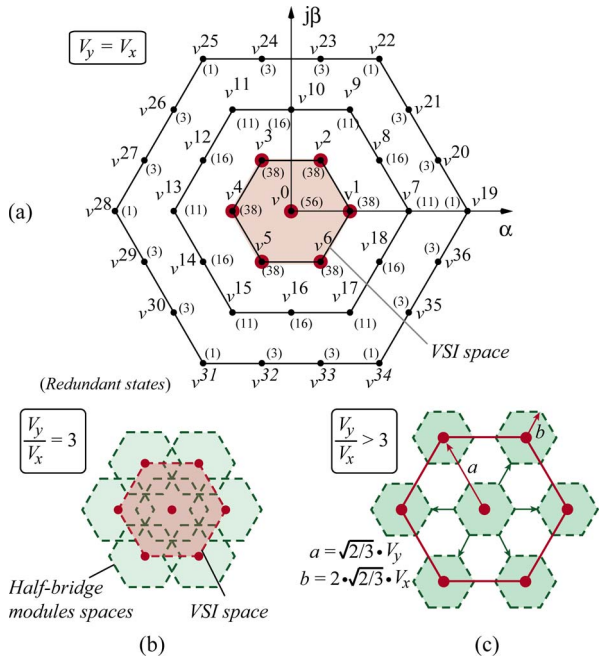

Fig. 4. Space vectors for the proposed converter: (a) space vectors for the four-level converter employing $V_y = V_x$; (b) contributions for the modulation domain for $V_y = 3V_x$, and; (c) contributions for the modulation domain for $V_y > 3V_x$.

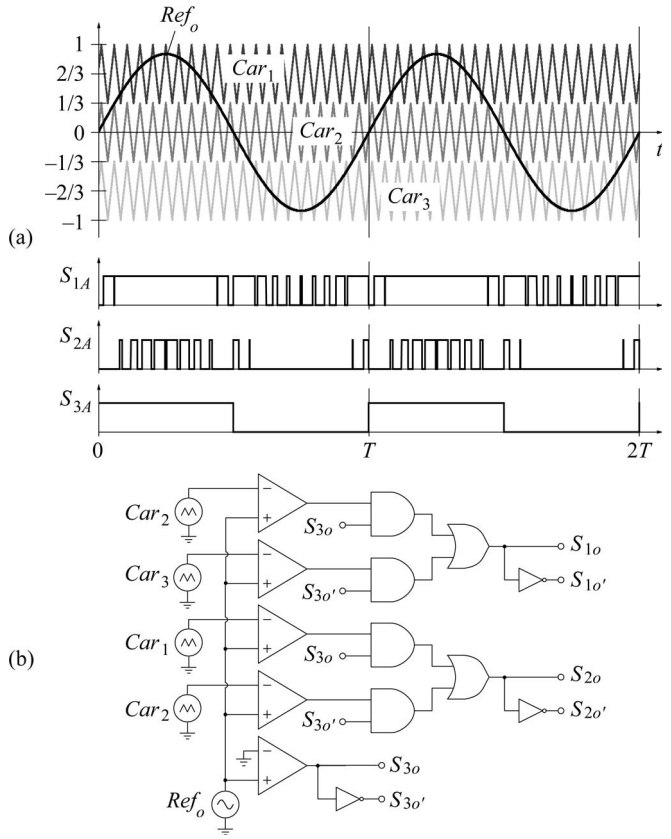

Fig. 5. Modulation strategy HM: (a) timing diagram for the four-level operation and (b) PWM generation logic.

VSI space and creates a higher number of levels. However, the voltage ratings for the semiconductors is changed accordingly. The number of redundant switching states is also presented in Fig. 4(a) for the four-level converter.

III. MODULATION SCHEME FOR THE FOUR-LEVEL CONVERTER

This section presents a modulation scheme for the four-level operation of the HC1/2B where the switches of the three-phase VSI switch at low frequency to transfer the switching losses to the half-bridge modules. This feature allows to use low-speed switches in the three-phase inverter reducing the conduction losses in the VSI [36], while keeping the switching losses at the same level, although shifted to the half-bridge modules. Even though non-uniform losses distribution among the power switches occur, the modulation scheme is able to better distribute losses among the power modules (comprising two IGBTs and their anti-parallel diodes). The half-bridge modules are switched at high frequency. Switches S_{jo} and $S_{jo'}$, with $o = A, B, C$ and $j = 1, 2, 3$, are switched in a complementary way. The first modulation pattern, is based on the level shifted in-phase disposition PWM [37]. However, the three-phase VSI switching signals are not directly derived from the modulator/carrier comparison and demand logic to be generated at the output frequency. Thus, the first strategy is configured as a hybrid modulation. As it is used with high modulation indexes it is here named HM. The half-bridge modules are derived from sinusoidal modulating signals Ref_o compared to three synchronized triangular carriers Car_j as shown in Fig. 5(a)

TABLE II
OUTPUT PHASE VOLTAGE v_o $(o = A, B, C)$ AND ACTIVE POWER DIRECTION AT THE DC SOURCES AS A FUNCTION OF THE SWITCHING STATES AND OUTPUT CURRENTS i_o DIRECTION. P_{1o} AND P_{2o} ARE THE AVERAGE POWERS PROCESSED BY THE UPPER AND THE LOWER DC SOURCES, RESPECTIVELY, FEEDING THE HALF-BRIDGE MODULES AT PHASE o. THE PLUS SIGNAL $(+)$ INDICATES THAT THE SOURCE IS FEEDING POWER. THE MINUS SIGNAL $(-)$ INDICATES THAT THE SOURCE IS SINKING POWER. THE EMPTY SIGNAL $(\varnothing)$ INDICATES THAT NO CURRENT FLOWS IN THE SOURCE

s_{1o}	s_{2o}	s_{3o}	v_o	P_{1o}	P_{2o}	i_o
0	0	0	$\frac{-3V_{cc}}{2}$	$-/+$	Ø/Ø	$i_o > 0/i_o < 0$
1	0	0	$\frac{-V_{cc}}{2}$	Ø/Ø	Ø/Ø	$i_o > 0/i_o < 0$
0	1	0	$\frac{-V_{cc}}{2}$	$-/+$	$+/-$	$i_o > 0/i_o < 0$
1	1	0	$\frac{+V_{cc}}{2}$	Ø/Ø	$+/-$	$i_o > 0/i_o < 0$
0	0	1	$\frac{-V_{cc}}{2}$	$-/+$	Ø/Ø	$i_o > 0/i_o < 0$
1	0	1	$\frac{+V_{cc}}{2}$	Ø/Ø	Ø/Ø	$i_o > 0/i_o < 0$
0	1	1	$\frac{+V_{cc}}{2}$	$-/+$	$+/-$	$i_o > 0/i_o < 0$
1	1	1	$\frac{+3V_{cc}}{2}$	Ø/Ø	$+/-$	$i_o > 0/i_o < 0$

for a generic phase o, with $o = A, B, C$. The VSI switches are driven by the direct comparison of the modulating signals Ref_o to zero. The logic employed to generate the modulation pattern is presented in Fig. 5(b). For the four-level converter, the modulation index is defined as $M = 2V_p/(3V_{cc})$, where V_p is the peak value of the sinusoidal PWM generated output phase voltages.

The phase shift modulation pattern, applied in the proposed converter, allows that all switches have the same conduction and switching losses. However, these losses and the distortion at the output line voltage are greater than it is achieved with the proposed modulation [36].

Focusing in unidirectional applications, it is desirable that all dc sources supply an unidirectional power flow, so that uncontrolled rectifiers can be employed. Table II shows that positive or negative power flow at some of the insulated dc sources does not depend only on the switching states, but also on the direction of the phase currents. Thus, it is not possible to control the power flow at all dc sources only by choosing proper switching states. The modulation pattern previously described is not able to guarantee unidirectional power flow in the dc sources for the half-bridge modules for a modulation index ranging from null to unity. The output voltages of the VSI are kept constant during each half period and this forces the half-bridge modules to process more power and regenerate it to the source for low modulation indexes. This is clearly observed in Fig. 6, where the power flow at an insulated dc source V_x becomes negative for $M < 0.42$ and the active power handled by all dc sources is extremely high at low modulation indexes when compared to the total active power transferred to the load. This characteristics prevents the employment of modulation HM for the entire modulation index range.

One way to avoid the regenerative power flow in the insulated dc sources is to switch the three-phase VSI at high frequency, generating output PWM voltages with a sinusoidal behavior proportional to the modulation index. Nevertheless, switching losses at the VSI would increase accordingly. Thus, a modification of the modulation logic is proposed. The VSI high side or low side switches are kept turned-on during the whole period whenever $M < 1/2$. The modulation pattern for $M < 1/2$ is presented in Fig. 7 and is named modulation LM. The LM modulation is a variation of the unipolar PWM [37]. In the LM modulation the command signals of the three-phase inverter do not change and the command of the half-bridge modules are the same as for the unipolar PWM.

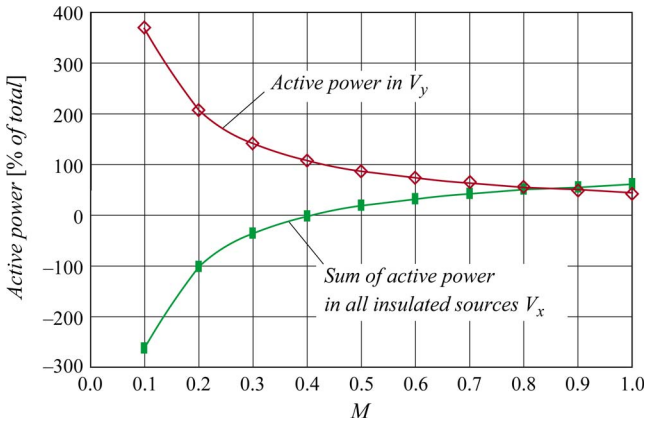

Fig. 6. Active power handled by the dc sources as a percent of the total load power for modulation pattern HM.

The modulation scheme basic algorithm is as follows [37].

- $\mathbf{0 \leq M \leq 1/2}$ (LM): the VSI has all switches either clamped to the positive or to the negative rail. The clamping can be changed at every modulation cycle to balance the losses at all semiconductors or, whenever possible a bypass mechanical switch can be driven to reduce conduction losses. The half-bridge modules process all the active power transferred to the load.
- $\mathbf{M > 1/2}$ (HM): each VSI leg switches a single time per modulation period (cf. Fig. 5) and the half-bridge modules handle a smaller power share.

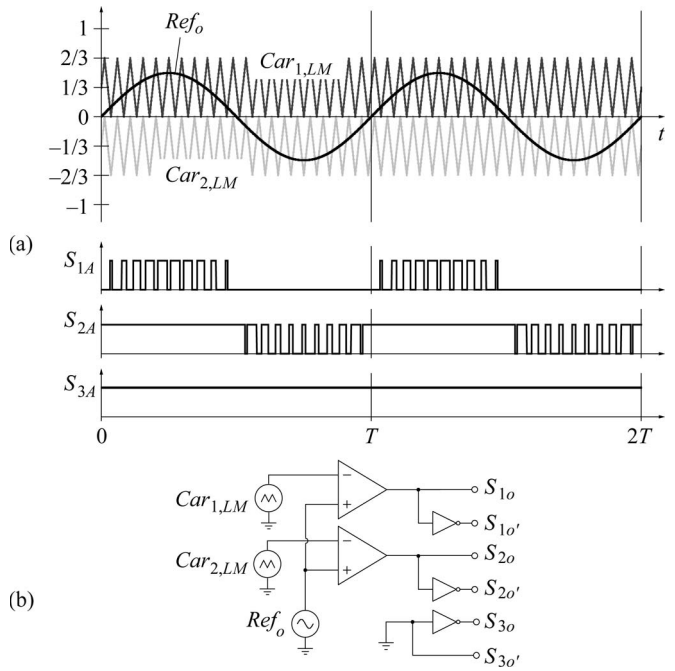

Fig. 7. Modulation strategy LM: (a) timing diagram for the three-level operation and (b) PWM generation logic.

This modulation scheme is able to generate three-phase sinusoidal PWM modulated voltages under any modulation index. It presents the advantage of processing larger power levels by the three-phase VSI, which does not require an insulated dc source and switches at low frequency. Furthermore, as seen in Section VI, it guarantees that active power levels equal or lower than the total load active power are processed within the multilevel sub-converters.

Both modulation patterns are able to produce line-to-line voltages with five-level while all dc sources supply positive active power for the range $4/(3\pi) < M < 2/3$. Therefore, any modulation index within this range can be achieved and a hysteresis control can be used to switch between the two methods without resulting in oscillations. For instance, when modulation index is to be reduced, the pattern change takes place for $M = 0.45$, while it happens for $M = 0.55$ when M increases. To verify modulation pattern transition, Fig. 8 shows simulation results for voltages and currents during a modulation change from HM to LM at a modulation index $M = 1/2$. It is observed that the modulation pattern change is smooth and does not cause any oscillation at the line voltages and, more importantly, at the phase currents. It is also important to notice that just some of the redundant states have been used with the proposed modulation pattern.

IV. Extension for More Than Two Half-Bridge Modules

This section presents an extension of the proposed multilevel hybrid converter for four half-bridge modules per phase. Employing the symmetric configuration shown in Fig. 9(a) allows to achieve six levels in the phase voltages. Fig. 9(b) shows the converter phase voltages (v_A, v_B, v_C) and line voltage (v_{AB}) for the multilevel inverter in Fig. 9(a). An adaption of the

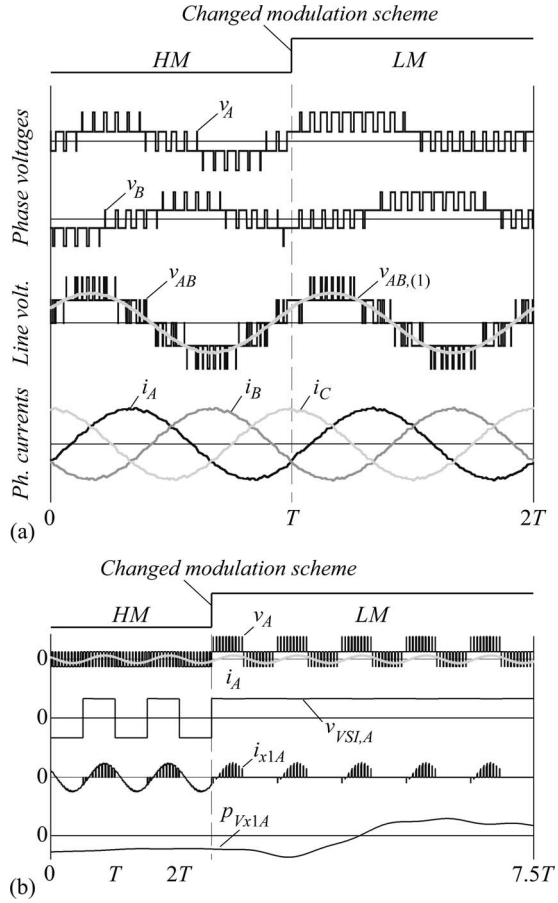

Fig. 8. Waveforms for $M = 0.5$ during a change from HM to LM modulation: (a) phase voltages v_A and v_B, line-to-line voltage v_{AB} and its fundamental component, and phase currents i_A, i_B and i_C; (b) phase voltage v_A and current i_A, output voltage of the VSI $v_{VSI,A}$, dc source current i_{x1A} and power p_{Vx1A}.

proposed HM modulation was used to drive the inverter. The phase and line voltages present low harmonic distortion, where the line voltage synthesizes up to 11 levels. It should be noticed that more transformers (or more secondaries) and their rectifiers must be added to the converter to supply the additional half-bridge modules with insulated dc sources.

V. Output Voltage Analysis

The output voltage analysis for the four-level HC1/2B employing the proposed modulation is performed based on [37] and consists in expressing the output phase voltages as functions of harmonic components of the fundamental and carrier frequencies. Inverter phase voltages can be expressed by

$$\begin{aligned} f(t) = \frac{A_{00}}{2} &+ \sum_{n=1}^{\infty} \left[A_{0n}\cos(n\cdot y) + B_{0n}\sin(n\cdot y)\right] \\ &+ \sum_{m=1}^{\infty} \left[A_{m0}\cos(m\cdot x) + B_{m0}\sin(m\cdot x)\right] \\ &+ \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty} \left[A_{mn}\cos(m\cdot x + n\cdot y)\right. \\ &\qquad \left. + B_{mn}\sin(m\cdot x + n\cdot y)\right] \end{aligned} \tag{2}$$

with $x = \omega_c t + \theta_c$ and $y = \omega_o t + \theta_o$.

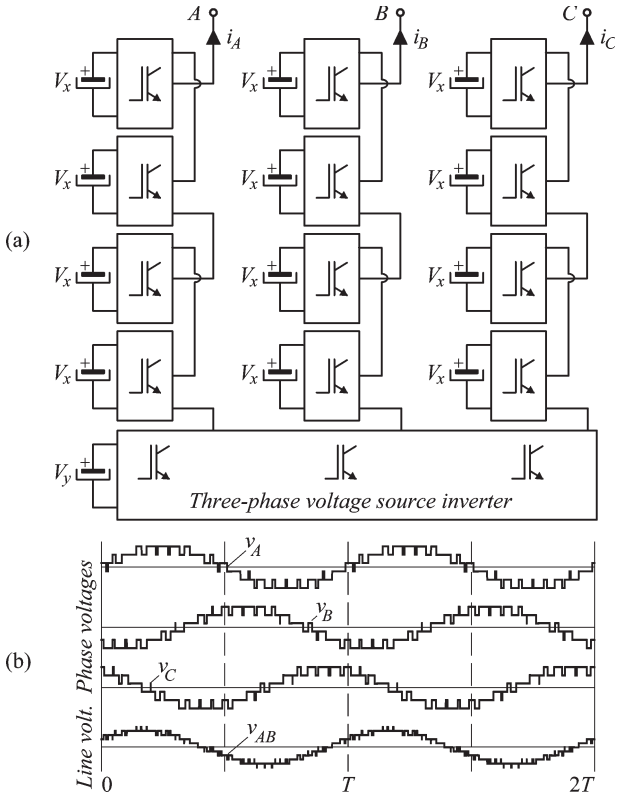

Fig. 9. Extension of the proposed structure to include more half bridge cells in a cascade configuration: (a) symmetrical topology (i.e., $V_x = V_y$) for a six-level converter and (b) phase and line voltages for six levels in phase voltage.

In (2), variables x and y represent the angular carrier frequency and the angular fundamental frequency, respectively, and the terms A_{mn} and B_{mn} express the amplitude of each harmonic component. The harmonic components are obtained through the double Fourier integral

$$\overline{C_{mn}} = A_{mn} + j \cdot B_{mn} = \frac{1}{2 \cdot \pi^2} \cdot \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) \cdot e^{j \cdot (m \cdot x + n \cdot y)} \, dx \, dy \qquad (3)$$

where $f(x,y)$ is the output phase voltage synthesized by the inverter. For the computation of the double Fourier integral it is necessary to determine the integration limits for variables x and y. Those limits are obtained equaling the expression that represents the reference modulating signals with the expressions that represent the ramps that generate the three carrier signals. This mathematical manipulation follows the concepts presented in [37], from where a unitary cell with all integration limits is derived. This unitary cell for the inverter operation with four levels at the phase voltage is shown in Fig. 10. This figure shows variable x integration limits, from $x_{1,\ldots,6}$ and axis y integration limits y_1 and y_2, which are

$$y_1 = \text{acos}\left(\frac{1}{3 \cdot M}\right)$$
$$y_2 = \pi - \text{acos}\left(\frac{1}{3 \cdot M}\right). \qquad (4)$$

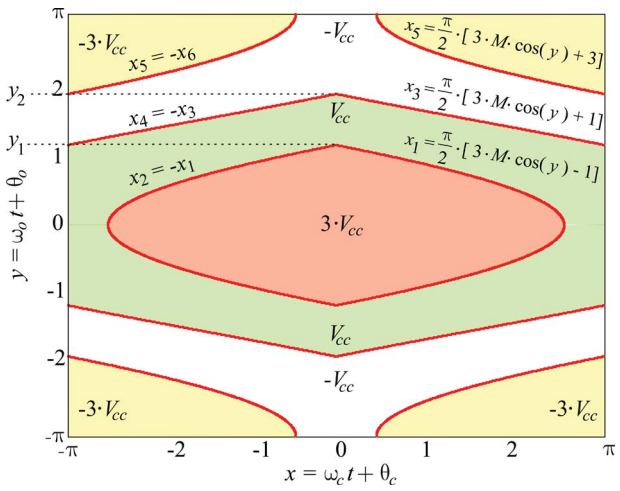

Fig. 10. Unitary cell for four-level output phase voltage v_a.

TABLE III
INTEGRATION LIMITS FOR ANALYTICAL OUTPUT VOLTAGE CALCULATION

Limit / i =	1	2	3	4	5	6
a_i	0	0	y_1	y_2	y_2	y_2
b_i	y_1	y_1	y_2	π	π	π
c_i	0	x_1	0	x_3	0	x_5
d_i	x_1	π	x_3	π	x_5	π
$f_i(x,y)$	3	1	1	-1	-1	-3

The aforementioned integration limits lead to twenty four integrals that are solved to find the amplitude of each harmonic component. Equation (3) is rewritten as

$$\overline{C_{mn,i}} = \frac{V_{cc}}{2\pi^2} \int_{a_i}^{b_i} \int_{c_i}^{d_i} f_i(x,y) \cdot e^{j \cdot (m \cdot x + n \cdot y)} \, dx \, dy \qquad (5)$$

which shows the integration limits a_i, b_i, c_i, d_i and function $f_i(x,y)$ that is the generated voltage level. Integration limits are given in Table III for positive values of x and y axis. Further eighteen integral limits exist by employing similar procedures. All twenty four integrals are solved to find the amplitude of each harmonic component. This is shown exemplarily in Fig. 11 with a comparison to experimental results. Simulation results have led to negligible error values and, thus, are not presented. The theoretical harmonic amplitudes are in good accordance with the experimental results except from the fact that the low frequency voltage ripple at the dc sources, the interlock delay times and the switching intervals generate harmonic components that are not theoretically computed and, thus, lead to the errors given in Fig. 11.

VI. EXPERIMENTAL VERIFICATION

Experimental verification is carried out in a small scale IGBT-based prototype that implements a symmetrical four-level ($V_x = V_y$) converter as drawn in Fig. 1. The prototype

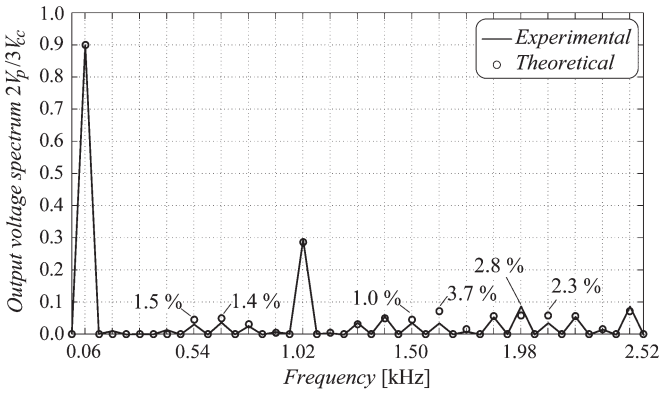

Fig. 11. Harmonic spectral results for $M = 0.9$, $f_{vo} \cong 60$ Hz and $f_s \cong 1.02$ kHz—HM modulation: experimental and theoretical results along with the absolute error values for the harmonic components that presented absolute errors higher than 1%.

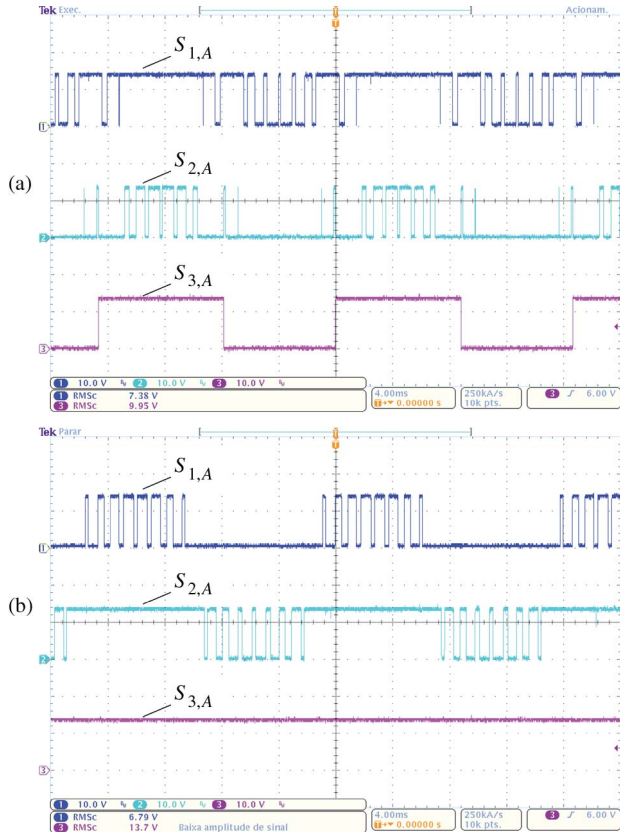

Fig. 12. Implemented gate signal patterns for (a) HM modulation and (b) LM modulation. The switches $S_{jA'}$ are driven by complementary signals with a dead-time of 4 μs. Scales 10 V/div, 4 ms/div.

presents all dc sources with galvanic insulation through three-phase transformers, which are fed by the mains with a three-phase auto-transformer to achieve control of the input voltages. Three-phase diode bridges rectify the voltages in the secondary side of the transformers and electrolytic capacitors smooth the rectified voltages to achieve low ripple dc voltages in all dc sources with an average value of approximately 400 V. A total of nine IGBT half-bridge modules implement the four-level converter. The employed IGBTs are manufactured by Semikron in half-bridge modules (SKM75GB063D) rated for 600 V and 75 A. The switching frequency for the half-bridge converters is set to 1.02 kHz, while the output fundamental voltage is 60 Hz. The hardware has been built to offer safe operation margins and flexibility and, thus, is not optimized for specific operation conditions. The employed RL load presents $R = 60\ \Omega$ and $L = 111$ mH delta connected, leading to a current displacement angle around 34° at 60 Hz.

The practical implementation of both modulation patterns, LM and HM, is performed in a DSP, model TMS320F2812, where the gate signals are generated in an open-loop scheme. The modulation employs the DSP's event manager (EVA and EVB) and a few I/O pins. The high frequency PWM pulses are produced by the DSP's PWM modules, while the low frequency signals are software generated by comparing the modulating signals to zero. The sinusoidal references are internally computed through a routine that calculates 60 Hz sinusoidal signals displaced by 120°. A zero crossing detector is virtually implemented to compare the polarity of the sinusoidal references. Depending on the instantaneous value of the modulating function an algorithm adapts the function levels to the DSP's PWM modulator. The modulation patterns generated by the implemented logic are observed in Fig. 12.

The command signals for both modulation patterns (HM and LM) are shown in Fig. 12. In Fig. 12(a) the command signals for HM strategy and a modulation index $M = 0.9$ are presented, while Fig. 12(b) shows the implemented gate command signals for LM modulation for a modulation index $M = 0.5$. In these figures the switching frequency are reduced to improve visualization.

Applying a modulation index $M = 0.9$ leads to the phase voltages, i.e., voltages between the load terminals A, B, C and the mid-point of the VSI's dc-link, as shown in Fig. 13. Fig. 13(a) presents voltages v_A, v_B and v_C. It is observed that the phase voltages closely follow the simulated patterns and are displaced by $2\pi/3$ from each other. The measured line voltage v_{AB} is given in Fig. 13(b) together with phase current i_A (Δ-connected RL load). Once again the experimental waveforms verify the theoretical analysis demonstrating a seven-level line voltage with low harmonic distortion.

Applying a modulation index $M = 0.5$ leads to the phase voltages depicted in Fig. 14. It is observed that the three-level phase voltages follow the theoretical LM modulation pattern with the dc offset (≅200 V) due to the measurement from the phase terminals to the center point of the VSI's dc-link. The line voltage v_{AB} is shown in Fig. 14(b) with the phase current i_A. The line voltage presents five-levels as expected.

Fig. 15 shows the output line voltage v_{AB} and the output phase current i_A during two modulation pattern changes from HM to LM and back to LM to HM. There is no synchronism scheme to perform the changes and it is observed that there are no significant change in the voltage/current applied to the load. Small oscillations in the modulation signals might be present in a closed loop system. Such oscillations may lead to fast changes from a modulation pattern to the other. This will be reduced by employing a hysteresis band that profits from the modulation index range where both patterns can be employed. This issue would need to be considered carefully when applied as part of a closed loop control system.

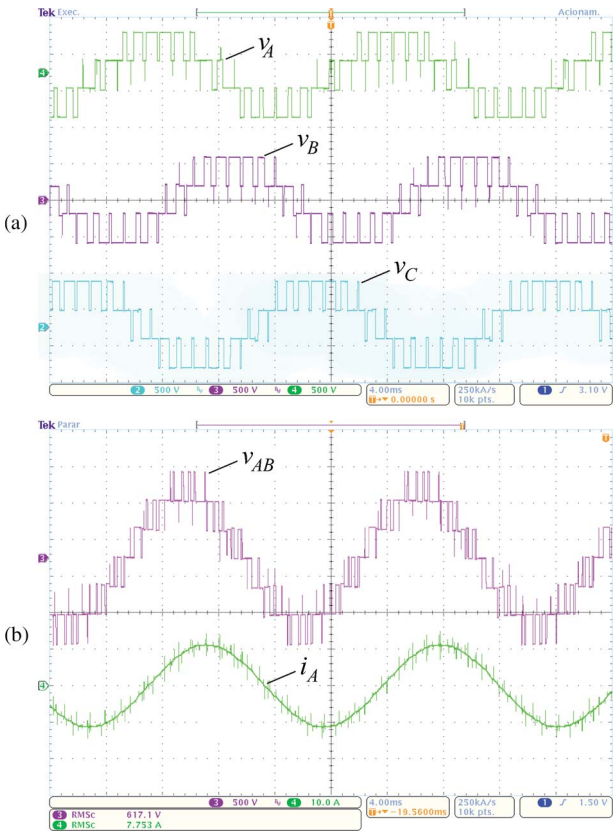

Fig. 13. Experimental results for $M = 0.9$, $f_{vo} \cong 60$ Hz and $f_s \cong 1$ kHz—HM modulation: (a) phase voltage at phase A, B and C and (b) line voltage v_{AB} and phase current i_A. Scales are 500 V/div, 10 A/div, 4 ms/div.

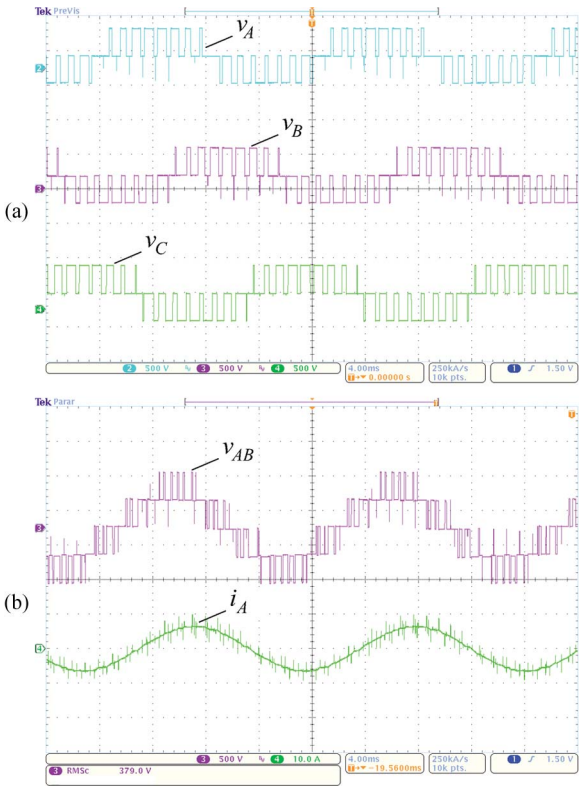

Fig. 14. Experimental results for $M = 0.5$, $f_{vo} \cong 60$ Hz and $f_s \cong 1$ kHz—LM modulation: (a) phase voltage at phase A, B and C and (b) line voltage v_{AB} and phase current i_A. Scales are 500 V/div, 10 A/div, 4 ms/div.

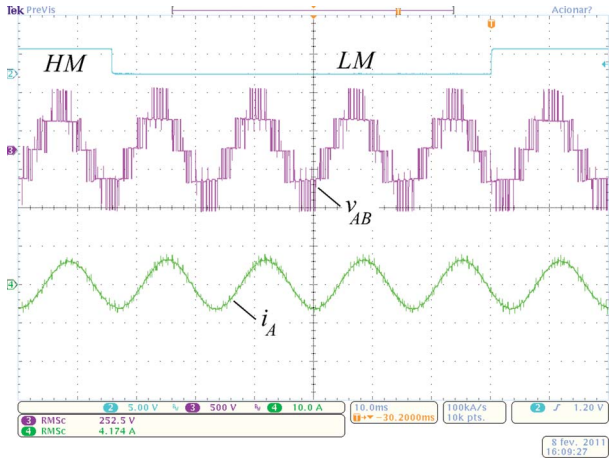

Fig. 15. Modulation pattern logic signal where HM modulation $= 5$ V and LM modulation $= 0$ V; output line voltage v_{AB} and phase current i_A during modulation schemes changed from LM to HM and back. Scales are 500 V/div, 10 A/div and 10 ms/div.

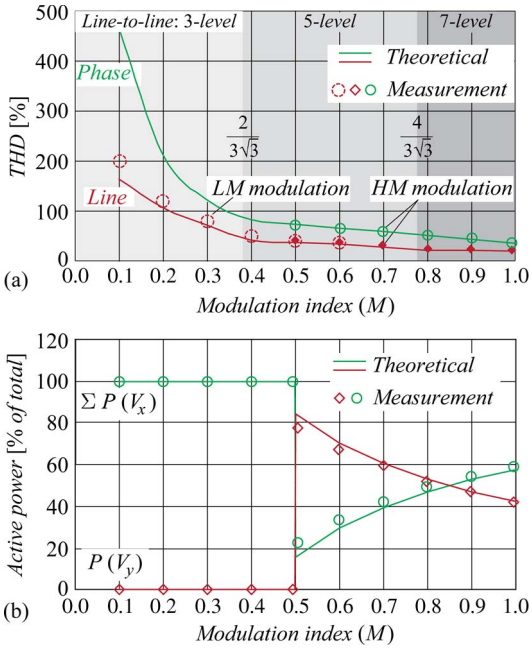

Fig. 16. Measured and theoretical. (a) THD for line and phase voltages according to the modulation index M and (b) active power for the VSI dc source $P(V_y)$ and for the sum of the sources for the half-bridge modules $\sum P(V_x)$. The THD values are computed considering harmonics from 2 to 1000.

The modulation index has been varied from close to unity to close to null to verify the active power distribution between the insulated dc sources and to measure the THD of line and phase voltages. The HM modulation pattern was employed from $M = 1$ down to $M = 0.5$, while the LM was used for lower modulation index values. The measurement results are summarized in Fig. 16 along with the theoretical results reported in Section III. Regarding voltage THDs, both, theoretical and experimental results are very well matched. Errors lower than 10% are observed at the power distribution curves, which do verify the simulation results and show the importance of the modulation scheme for this type of multilevel converter.

VII. Conclusion

A novel hybrid multilevel converter able to achieve four, five or six level operation has been proposed. The main advantage for this solution is the possibility of reduction of the power ratings for insulated dc sources compared to the CHB and to other hybrid solutions such as the VSI cascaded with full-bridge converters. The operation principle of the converter has been clarified and the achievable space vector spaces presented. A four-level hybrid modulation scheme has been presented, which allows unidirectional power flow in all dc sources for any modulation index and, thus, lowers the power demand on the insulated dc sources for high modulation indexes. A pair of 12-pulse rectifiers to supply the converter is proposed to minimize input current harmonics. The theoretical analysis of the output voltages has been presented and experimentally verified. Furthermore, the modulation scheme is able to generate, both, phase and line voltages with low THD. Experimental results based on a built prototype have validated the performed analysis and shown the relevant operating characteristics of the proposed converter.

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