# Step-Up/Step-Down DC–DC ZVS PWM Converter With Active Clamping

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***Abstract*—This paper presents a regenerative step-up/step-down dc–dc zero-voltage-switching pulsewidth-modulation converter with active clamping. The switch losses are reduced due to the implementation of a simple active snubber circuit that provides soft commutation in all the switches of the converter. The theoretical analysis, basic equations, design methodology, and experimental results are shown in this paper. A control methodology to assure the output voltage regulation is also proposed. The main advantages of the proposed power converter are the small number of components, simplicity of the controller, robustness, small weight and size, and high efficiency.**

***Index Terms*—Active clamping, dc–dc converters, soft commutation, step-up/step-down.**

## I. Introdution

DURING the last several years, continuous current (dc) machines have largely lost their popularity in the industry environment to the ac machines. There is a clear preference for induction machines due to low maintenance, durability, and reduced costs.

However, in certain applications, it is not easy to replace dc machines. Automatically guided vehicles (AGVs) and electrical forklift trucks used in a great part of the industrial environment are some examples.

Some of the current problems found on AGVs are the low autonomy of its batteries and the use of special machines and converters that cost high and are more difficult to find on the market.

This paper introduces a new driving alternative for battery-based vehicles. The new proposal uses ac machines that are easily found on the market at accessible prices, i.e., a simple step-up converter and a regular voltage inverter.

The classic AGV and the alternative driving topology are shown in Fig. 1. Willing to use regular ac machines that are easily found on the market, the structure presented in Fig. 1(b) must step up the voltage before a voltage inverter is used to drive the machine.

In addition to the topological difference, it is known that regular dc–dc converters used in the classical topology do not use appropriate commutation techniques, resulting in higher losses and higher electromagnetical interference. As an example, in leg converters, at the moment that the main switch turns on, it provokes the reverse recovery phenomenon of the antiparallel diode of the complementary switch.

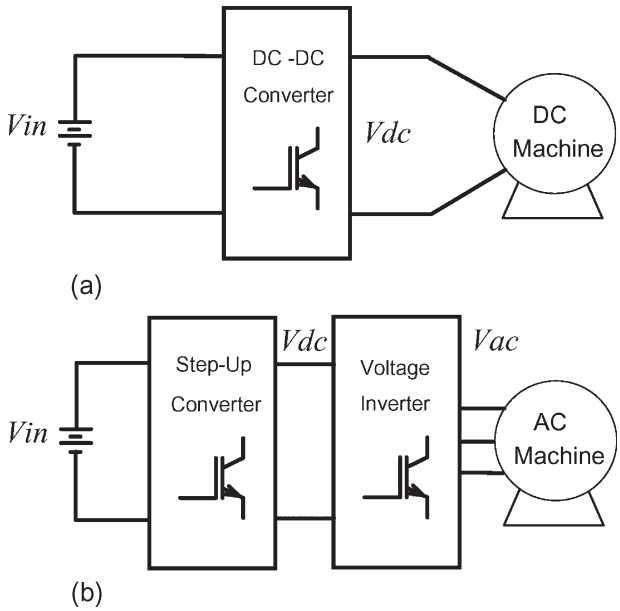


Fig. 1. (a) Classic power topology of an AGV. (b) Alternative power topology of an AGV.

During this stage, the switches are submitted to a high current ramp rate $(di/dt)$ and a high peak of reverse recovery current. As mentioned, both effects significantly contribute to increase commutation losses and electromagnetic interference.

Regarding this issue, many studies have been carried out by the scientific community in order to improve the commutation techniques and minimize its effects; these studies can be divided into two groups: active and passive techniques. The main difference between these two techniques is that the active technique uses controlled switches to achieve soft commutation, whereas the passive technique does not use controlled devices.

The most known among passive techniques is the Undeland snubber [1]. This technique provides a good performance in most of its applications, but it is not capable of regenerating the energy lost during the switching. To solve this problem, some researchers improved this technique, as presented in [2]–[5].

Most of active techniques uses pulsewidth modulation (PWM) since it does not require complex control circuits. An

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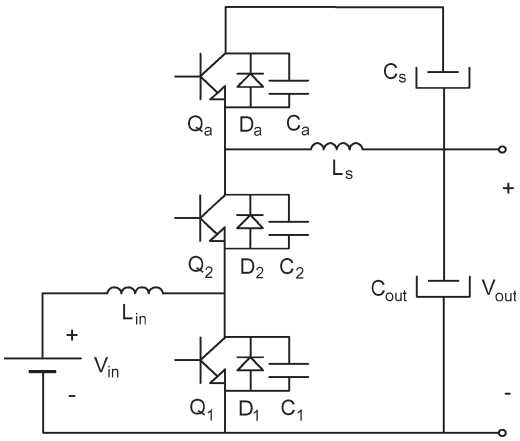


Fig. 2. Regenerative ZVS converter circuit.

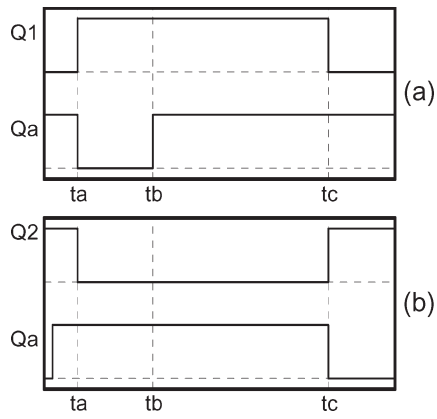


Fig. 3. (a) Switch commands in the "step-up" mode. (b) Switch commands in the "step-down" mode.

important work that uses this technique is the auxiliary resonant diode pole inverter [6]. This topology uses PWM and soft commutation by a simple circuit, but as a negative point, it needs a high current that is about 2.5 times higher than the load current, resulting in high stress on the switches. A similar topology is the auxiliary resonant pole inverter [7]. In theory, this circuit reduces the necessary current to provide soft commutation; in practical experiments, the soft commutation does not occur, because the resonant current, which is responsible for the soft commutation, had been attenuated due to parasitic resistances. Another important topology is the auxiliary resonant commutated pole inverter [8]–[10]. In this topology, the auxiliary switches just turn on when the load current is not high enough to provide soft commutation, so the control circuit is complex and needs current sensors.

Recently, a new inverter using zero-voltage switching (ZVS) turn-on and zero-current switching turnoff was proposed [14]. A good performance was acquired, but the number of components significantly increased.

Many other papers presented topologies that use the reverse recovery energy from the diodes to obtain soft commutation [11]–[18].

In this paper, a step-up/step-down dc–dc ZVS PWM converter with active clamping technique is proposed. The structure uses the reverse recovery energy from the diodes to obtain soft commutation in the switches of the circuit, including the auxiliary one.

## II. Presentation and Analysis of Circuit

The proposed circuit is shown in Fig. 2. This topology is similar to the classic current reversible converter, plus an auxiliary switch, a capacitor, and an auxiliary inductor. Capacitor $C_s$ is responsible for the storage of the diode reverse recovery energy and for clamping the switches voltage. Inductor $L_s$ is responsible for the control of the $di/dt$ during the diode reverse recovery time. Fig. 3 illustrates the switch command signals for the "step-up" and "step-down" modes. A microcontroller is used to create the command pulses and to detect whether the converter is working as a step-up or step-down converter to correctly synchronize the switches.

## III. Operation Stages (Positive Half Cycle)

The operation of the proposed converter is symmetrical. Thus, the analysis will be made only for the step-up operational mode. Some simplifications to facilitate the operation stage analysis of the converter will also be considered: The voltage in capacitors $C_{\rm out}$ and $C_s$ and the current in inductor $L_{\rm in}$ will be considered constant during a switching period. Input voltage $V_{\rm in}$ and inductance $L_{\rm in}$ will also be considered as a current source called $I_{\rm in}$.

- *First stage* $(t_0{-}t_1)$: This interval initiates with input current $I_{\rm in}$, delivering energy to source $V_{\rm out}$ via diode $D_2$ and inductor $L_s$. At the same time, the additional current $i_{\rm Cs}$ flows around the loop formed by $Q_a$, $L_s$, and $C_s$. At the end of this operational stage, current $i_{\rm Cs}$ will reach its maximum value called $I_f$.
- *Second stage* $(t_1{-}t_2)$: This operational stage starts when auxiliary switch $Q_a$ is blocked. Current $i_{\rm Cs}$ begins to charge capacitor $C_a$ from *zero* to $V_{\rm out}+V_{\rm Cs}$ and discharges $C_1$ from $V_{\rm out}+V_{\rm Cs}$ to *zero*.
- *Third stage* $(t_2{-}t_3)$: At this stage, the voltage across $C_1$ reaches *zero*, and it is clamped by antiparallel diode $D_1$. Thus, switch $Q_1$ conducts on a *ZVS* condition. At this moment, voltage $V_{\rm out}$ is applied across inductor $L_s$, and current $i_{\rm Ls}$ linearly decreases. Diode $D_1$ conducts current $i_{\rm Ls}$, whereas $D_2$ conducts current $i_{\rm Ls}+I_{\rm in}$.
- *Fourth stage* $(t_3{-}t_4)$: This stage begins when current $i_{\rm Ls}$ inverts its direction and flows through switch $Q_1$. The current in $D_2$ continues to decrease until it inverts its direction, starting its reverse recovery phase, while inductor $L_s$ limits $di_{\rm Ls}/dt$. At the end of this operational stage, the current in $L_s$ is equal to $I_r$.
- *Fifth stage* $(t_4{-}t_5)$: This stage starts when diode $D_2$ finishes its reverse recovery phase. Current $i_{\rm Ls}$ begins to charge capacitor $C_2$ from *zero* to $V_{\rm out}+V_{\rm Cs}$ and discharge capacitor $C_a$ from $V_{\rm out}+V_{\rm Cs}$ to *zero*.
- *Sixth stage* $(t_5{-}t_6)$: At this stage, the voltage across capacitor $C_a$ reaches *zero*, and it is clamped by diode $D_a$. Thus, auxiliary switch $Q_a$ conducts with ZVS. Current $i_{\rm Ls}$ increases due to the application of voltage $V_{\rm Cs}$ across inductor $L_s$. This stage finishes when the current in $L_s$ reaches *zero*.

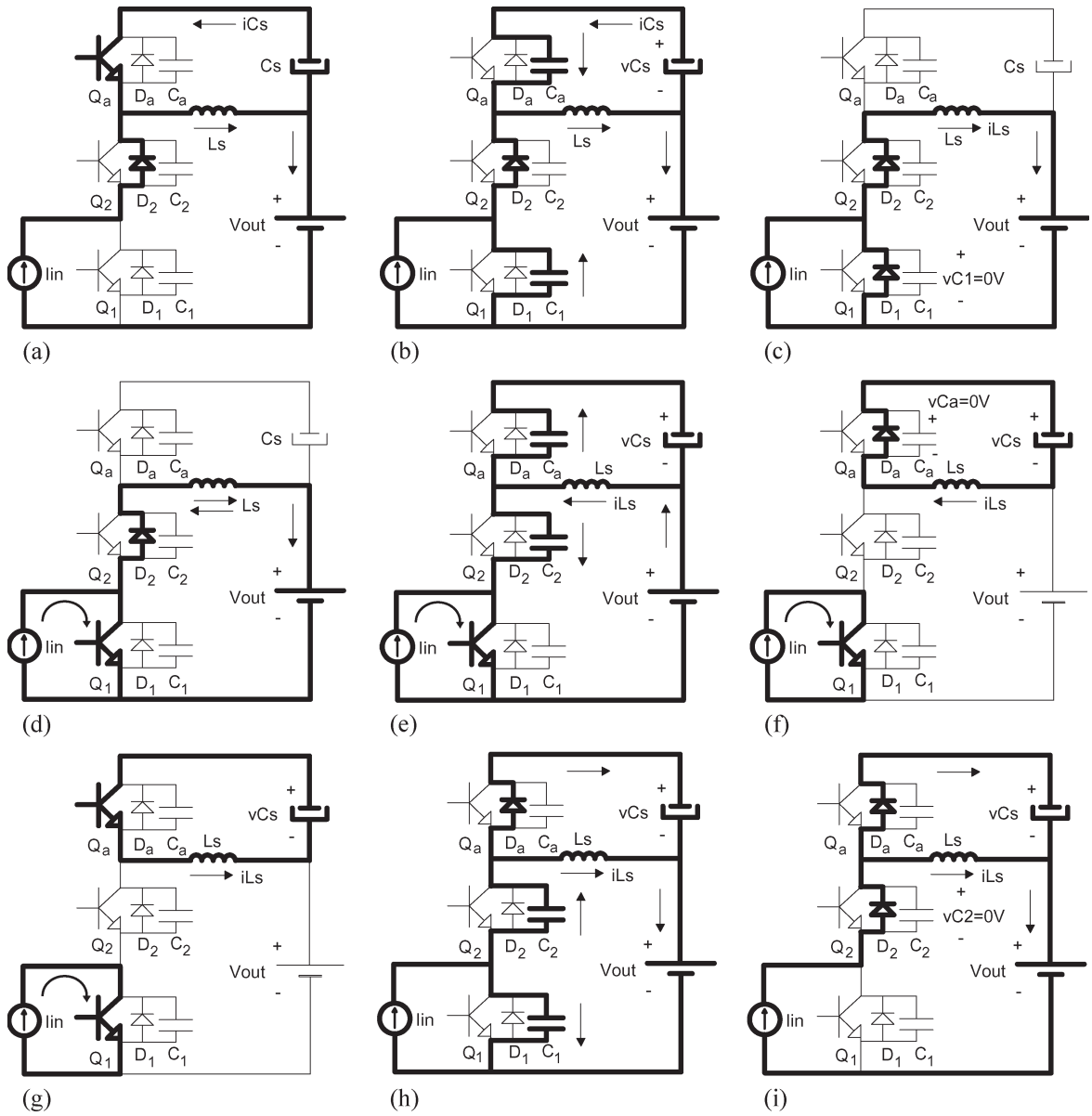


Fig. 4. Operation stages. (a) First stage $(t_0{-}t_1)$. (b) Second stage $(t_1{-}t_2)$. (c) Third stage $(t_2{-}t_3)$. (d) Fourth stage $(t_3{-}t_4)$. (e) Fifth stage $(t_4{-}t_5)$. (f) Sixth stage $(t_5{-}t_6)$. (g) Seventh stage $(t_6{-}t_7)$. (h) Eighth stage $(t_7{-}t_8)$. (i) Ninth stage $(t_8{-}T_s + t_0)$.

- *Seventh stage* $(t_6{-}t_7)$: This stage begins when current $i_{\rm Ls}$ changes its direction and flows through switch $Q_a$. Current $i_{\rm Ls}$ continues to linearly increase.
- *Eighth stage* $(t_7{-}t_8)$: At this stage, switch $Q_1$ is blocked, and the current in $C_s$ inverts its direction and flows through diode $D_a$. Capacitor $C_1$ is charged from *zero* to $V_{\rm out} + V_{\rm Cs}$, and capacitor $C_2$ is discharged from $V_{\rm out} + V_{\rm Cs}$ to *zero*.
- *Ninth stage* $(t_8{-}T_s + t_0)$: This stage begins when the voltage across capacitor $C_2$ reaches *zero*, and it is clamped by diode $D_2$. Current $i_{\rm Ls}$ continues to increase. This stage finishes when $i_{\rm Ls}$ is equal to $I_{\rm in}$ and flows through auxiliary switch $Q_a$, restarting the first operation stage.

The circuits of the mentioned operational stages and the respective waveforms can be visualized in Figs. 4 and 5, respectively.

## IV. Mathematical Analysis of Soft-Switching Circuit

One of the most important characteristics of the presented converter is the voltage clamping capability over all the switches. The quantitative analysis is given as follows.

The average instantaneous current in $C_s$ is calculated using the following expression:

$$iCs_{\rm av} = \frac{1}{T_s}\left[\int_0^{t_7}\left(\frac{V_g}{L_s}\cdot t - I_r\right)dt + \int_{t_7}^{t_1}\left(\frac{V_g}{L_s}\cdot t - I_{\rm in} - I_r\right)dt\right] \quad (1)$$

where

$T_s$ switching period;

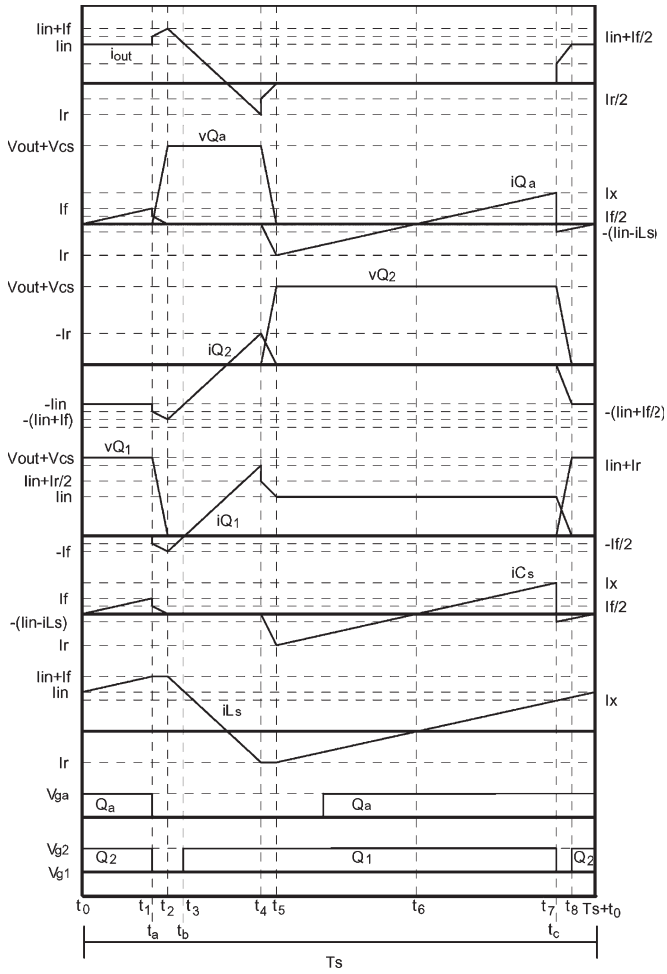


Fig. 5. Theoretical waveforms.

$V_g$ clamping voltage;
$I_r$ reverse recovery current peak on the diode.

In relation to the switching period, the commutation time is very short. Making a displacement to $t_1$ to facilitate the integral of $iCS_{\text{av}}$ and also defining $t_1 = 0$, one can consider that $t_5$ and $t_1$ are practically the same point, i.e., interval time $t_5 - t_1$ is almost zero; therefore, $t_7$ can be considered equal to $D \cdot T_s$, i.e.,

$$t_5 = t_1 = 0 \tag{2}$$

$$t_7 - t_5 = D \cdot T_s \tag{3}$$

$$t_7 = D \cdot T_s \tag{4}$$

where $D$ is the duty cycle to the switching period.

The evaluation result is the clamping voltage $V_g$ presented in the following:

$$V_g = \frac{2L_s}{T_s}\left[I_r + I_{\text{in}}(1-D)\right]. \tag{5}$$

The input current is given by

$$I_{\text{in}} = \frac{P_{\text{out}}}{\eta \cdot V_{\text{in}}} \tag{6}$$

where $\eta$ represents the converter efficiency.

Combining (5) and (6), the clamping voltage over $C_S$ can be expressed using

$$V_g = \frac{2 \cdot L_s}{T_s}\left[I_r + \frac{P_{\text{out}}(1-D)}{\eta \cdot V_{\text{in}}}\right]. \tag{7}$$

$I_r$ is the reverse recovery current peak on the diode in parallel with the switch. It is calculated using

$$I_r = \sqrt{\frac{4}{3} \cdot Q_{\text{rr}} \cdot \frac{V_{\text{out}}}{L_s}} \tag{8}$$

where $Q_{\text{rr}}$ is the necessary reverse recovery charge.

To assure commutation over zero voltage, it is necessary during the second operational stage that the current in inductor $L_s$ is high enough to assure the discharge of $C_1$ and the charge of $C_A$.

The following relationship describes this condition:

$$L_s \cdot I_f^2 \geq (C_a + C_1) \cdot (V_{\text{out}} + V_g)^2 \tag{9}$$

where $I_f$ is expressed by

$$I_f = \frac{V_g}{L_s} \cdot T_s - \frac{I_{\text{in}}}{2} - I_r. \tag{10}$$

Considering $V_g \ll V_{\text{out}}$, the relationship presented in

$$I_{f\,\min} \geq V_{\text{out}} \cdot \sqrt{\frac{C_1 + C_a}{L_s}} \tag{11}$$

can be found.

Thus, to assure soft commutation over all the operation range for a given load, the relationship presented in (11) should be true.

The value of $L_s$ is then calculated using

$$L_s = \frac{V_{\text{out}}}{di/dt}. \tag{12}$$

## V. Design Example

### A. Input Data

The prototype specifications can be observed in Table I. The input current given by (6) becomes

$$I_{\text{in}} = \frac{1000\ \text{W}}{0.95 \cdot 48\ \text{V}} \cong 22\ \text{A}. \tag{13}$$

### B. Calculation of Auxiliary Inductor

The auxiliary inductor is responsible for the $di/dt$ limit during the turnoff of the main diodes. $di/dt$ is directly related to the peak reverse recovery current $I_r$ of the antiparallel diodes. A "snappy" $di/dt$ produces a large amplitude transient voltage and significantly contributes to electromagnetic interference.

In the design procedure, a $di/dt$ that is usually found in the diode data sheet was chosen. This is a simple way to obtain the

TABLE I
SPECIFICATIONS

| | |
|---|---|
| $V_{in}$ = 48Vdc | Input Nominal Voltage |
| $V_{out}$ = 200Vdc | Output Nominal Voltage |
| $P_{out}$ = 1000W | Output Nominal Power |
| $\eta$ = 95% | Efficiency |
| $F_s$ = 40kHz | Switching Frequency |
| $L_{in}$ = 830µH | Input Inductor |
| $C_{out}$ = 475µF | Output Capacitor |

TABLE II
DIODE SPECIFICATIONS

| | |
|---|---|
| $V_{rrn}$ = 500V | Maximum Reverse Voltage |
| $I_{av}$ = 47A | Diode Average Current |
| $Qrr$ = 14.7µC | Reverse Recovery Charge |
| $C_{oss}$ = 1.4nF | Output Capacitance |

diode's fundamental parameter for the design of the inverter. In this case, the $di/dt$ chosen for the example was 20 A/$\mu$s. We know that the current ramp rate is determined by the external circuit; thus

$$L_s = \frac{200\ \text{V}}{20\ \text{A}/\mu\text{s}} = 10\ \mu\text{H}. \tag{14}$$

### C. Diode Selection

For satisfactory performance of the inverter, it is important to choose a slow diode. Therefore, we opted to use the body diode of MOSFET APT5010B2VR, whose characteristics are presented in Table II.

### D. Switching Period

$$T_S = \frac{1}{40\ \text{kHz}} = 25\ \mu\text{s}. \tag{15}$$

### E. Reverse Recovery Current

The reverse recovery current given by (8) becomes

$$I_r = \sqrt{\frac{4}{3} \times 14.7\ \mu\text{C} \times \frac{200\ \text{V}}{10\ \mu\text{H}}} = 19.8\ \text{A}. \tag{16}$$

### F. Clamping Voltage Capacitor Behavior

The clamping voltage given by (7) becomes

$$V_g = \frac{2 \cdot 10\ \mu\text{H}}{25\ \mu\text{s}} \left[19.8\ \text{A} + \frac{1000\ \text{W}(1-0.75)}{0.95 \cdot 48\ \text{V}}\right] = 20.2\ \text{V}. \tag{17}$$

### G. Soft Switching Condition

To guarantee a ZVS condition in all load ranges, the minimum value of current $I_f$, which was obtained from (10), must be greater than the value obtained from (11), i.e.,

$$I_f = \frac{20.2\ \text{V}}{10\ \mu\text{H}} \cdot 25\ \mu\text{s} - \frac{22\ \text{A}}{2} - 19.8\ \text{A} = 19.7\ \text{A} \tag{18}$$

$$I_{f\,\min} \geq 200\ \text{V} \cdot \sqrt{\frac{1.4\ \text{nF} + 1.4\ \text{nF}}{10\ \mu\text{H}}} = 3.3\ \text{A}. \tag{19}$$

## VI. CONTROL

To assure a good performance of the control methodology, the use of two feedbacks, i.e., a current feedback and a voltage feedback, is proposed. The use of a microcontroller to create the complementary PWM signals and to synchronize the auxiliary switch is also proposed.

The voltage control chosen was a proportional–integral control and should have a low response. The cutoff frequency is 12 Hz. Otherwise, the current control is a fast control. It is a leak and leg control, whose cutoff frequency is 4 kHz. Both of the controls have a phase margin between 30° and 90°. The control block diagram is shown in Fig. 6.

The voltage model transfer function is given by

$$G_v(s) = \frac{R_{\text{out}} \cdot (1-D)}{1 + s \cdot C_{\text{out}} \cdot R_{\text{out}}} \tag{20}$$

where

$V_o$ output voltage;
$I_{\text{Lin}}$ input inductor current;
$R_{\text{out}}$ load resistor;
$D$ duty cycle;
$C_{\text{out}}$ output capacitor.

The proposed voltage controller is shown in Fig. 7, and its transfer function is given by

$$C_v(s) = \frac{-(1 + s \cdot R \cdot C)}{s \cdot R_i \cdot C}. \tag{21}$$

The voltage loop frequency response is shown in Fig. 8.

The voltage loop with the designed controller presents a phase margin that is greater that 30°, obeying the desired design value.

The current model transfer function during the step-up operation is given by

$$G_i(s) = \frac{V_o}{s \cdot L_{\text{in}}}. \tag{22}$$

The proposed current controller is shown in Fig. 9, and its transfer function is given by

$$C_i(s) = \frac{-(1 + sR_2C_1)}{sR_1(C_1 + C_2) \cdot \left(1 + \frac{sR_2C_2C_1}{C_1 + C_2}\right)}. \tag{23}$$

The current loop frequency response is shown in Fig. 10.

The current loop with the designed controller presents a phase margin that is greater that 30°, obeying the desired design value.

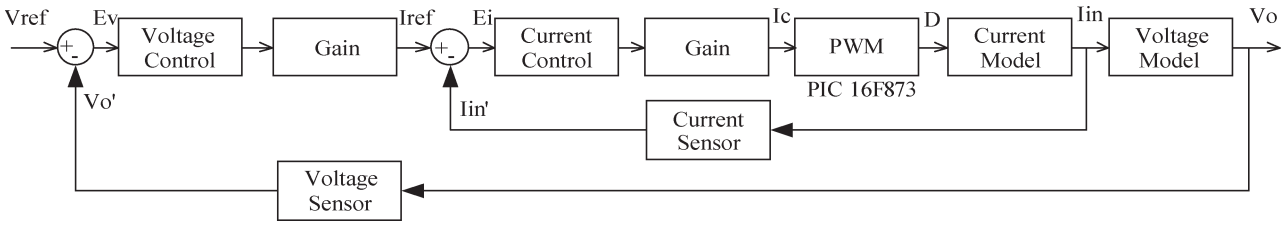


Fig. 6. System block diagram.

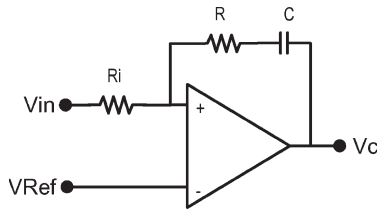


Fig. 7. Voltage controller.

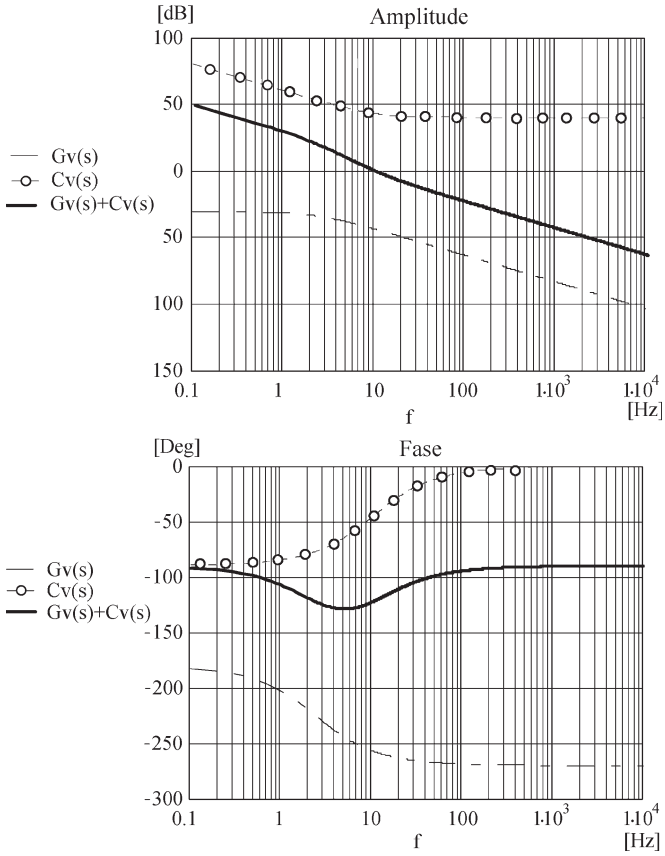


Fig. 8. Voltage loop frequency response.

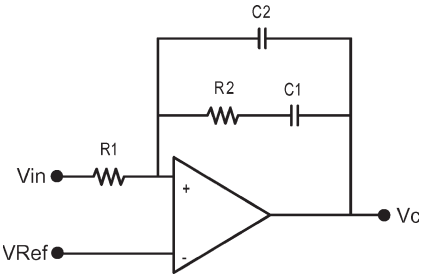


Fig. 9. Current controller.

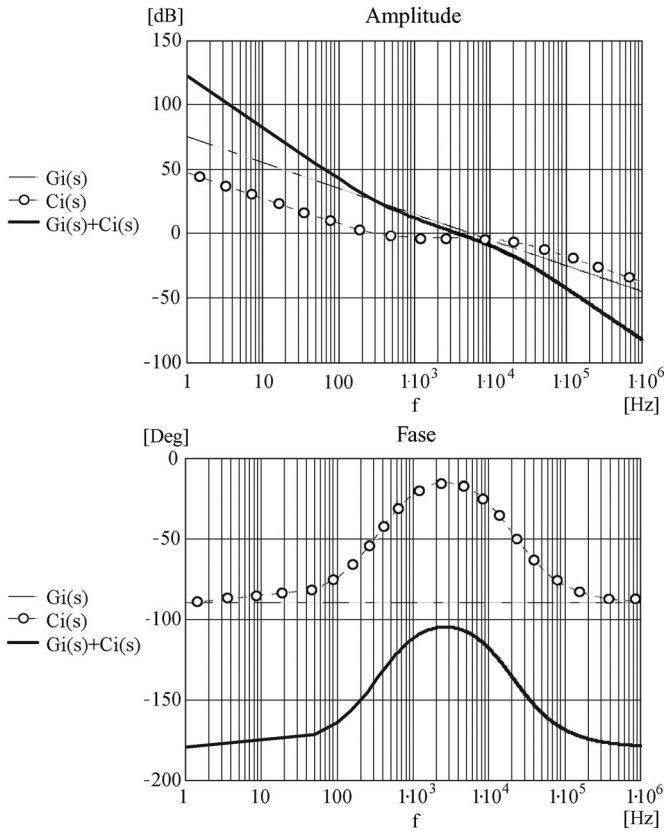


Fig. 10. Current loop frequency response.

TABLE III
PROTOTYPE SPECIFICATIONS

| | |
|---|---|
| $Q_1$, $Q_2$, $Q_a$ | Switches: APT5010B2VR |
| $D_1$, $D_2$, $D_a$ | Switches Intrinsic Diodes |
| $C_1$, $C_2$, $C_a$ | Switches Intrinsic Capacitances (≅1.4nF) |
| $L_{in}$ | Ferrite Inductor: IP6-EE65/26, 23turns |
| $L_s$ | Ferrite Inductor: IP6-EE42/20, 17 turns |
| $C_s$ | Electrolytic Capacitor 2 x 470uF/400V |
| $C_{out}$ | Electrolytic Capacitor 2 x 470uF/400V |

## VII. EXPERIMENTAL RESULT

Aiming to prove the theoretical studies, a prototype of 1 kVA was designed. The main specifications are shown in Table III.

Fig. 11 presents the command signals applied to switches $Q_1$, $Q_2$, and $Q_a$. It is important to observe that the $Q_1$ and $Q_2$ command signals are complementary and $Q_a$ is synchronized

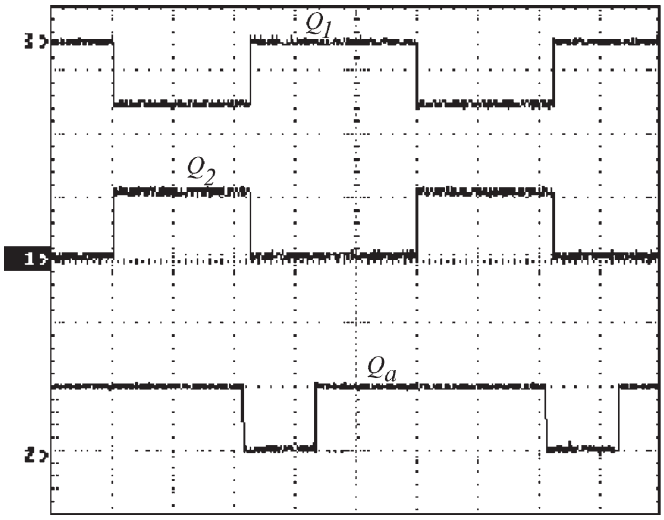


Fig. 11. $Q_1$, $Q_2$, and $Q_a$ signals (−5 V/div, 5 $\mu$s/div).

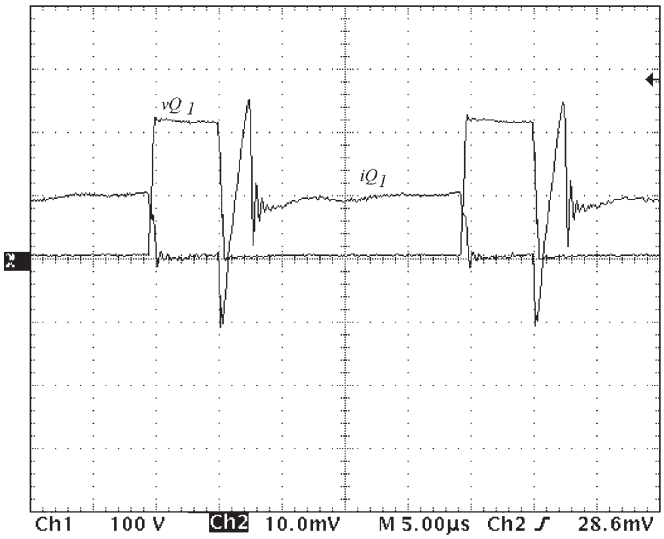


Fig. 12. Voltage (100 V/div) and current (5 A/div) on $Q_1$.

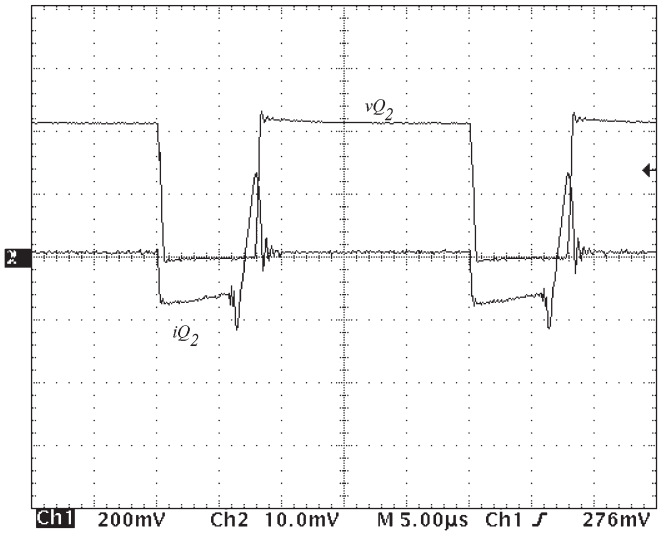


Fig. 13. Voltage (100 V/div) and current (5 A/div) on $Q_2$.

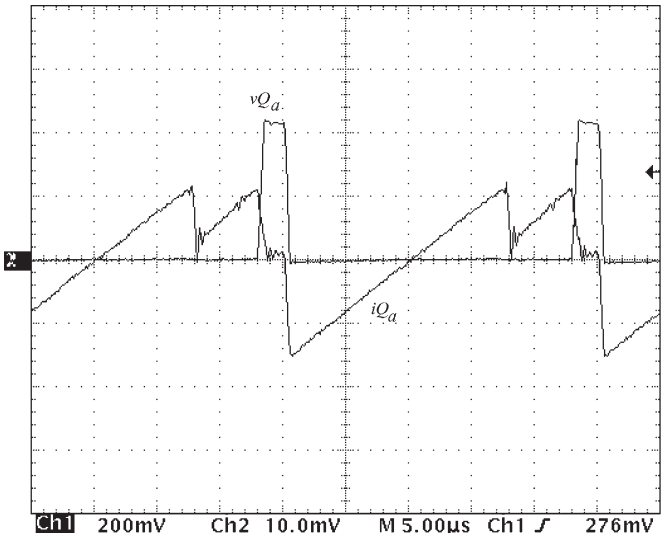


Fig. 14. Voltage (100 V/div) and current (5 A/div) on $Q_a$.

with $Q_1$, meaning that the converter is operating in step-up mode. Another detail in Fig. 11 is that the nominal power of the converter was not acquired; thus, the duty cycle is almost the same for $Q_1$ and $Q_2$. In Figs. 12–14, the voltage and current in $Q_1$, $Q_2$, and $Q_a$ are shown, respectively. It can easily be observed that the voltage on the switches is zero during the commutation. The current in inductor $L_s$ is shown in Fig. 15. The converter transient response to load steps demonstrates the stability of the control. The output voltage and input current during a full-to-half-load step is shown in Fig. 16. On the other hand, Fig. 17 shows the converter during a half-to-full-load step.

Results were also obtained during the current reversion. An isolated dc power supply was used to provide the necessary current to the load and extra energy to be sent back to the batteries.

Figs. 18 and 19 show the output voltage and input current during the current reversion. Fig. 20 shows the efficiency as a function of the load range.

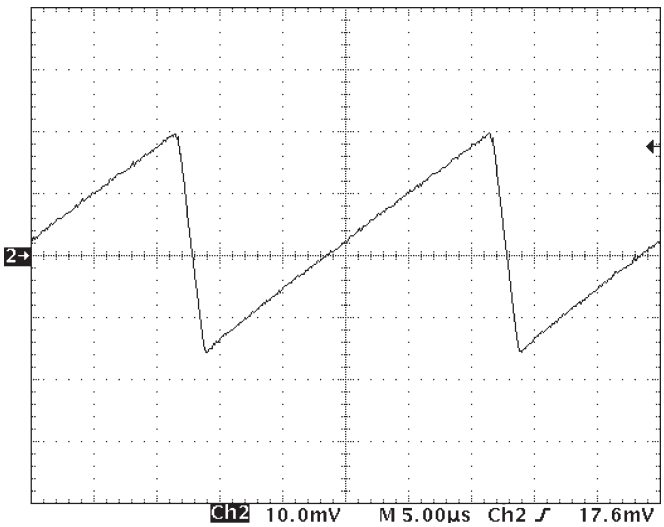


Fig. 15. Current in $L_s$ (5 A/div, step-up mode).

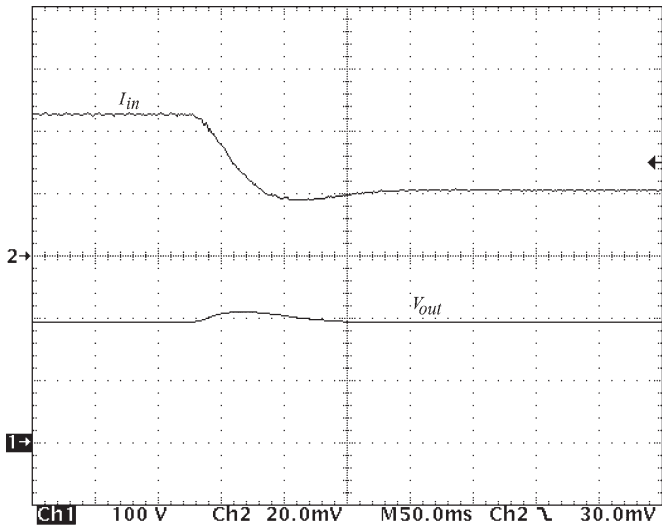


Fig. 16. Output voltage (100 V/div) and input current (4 A/div).

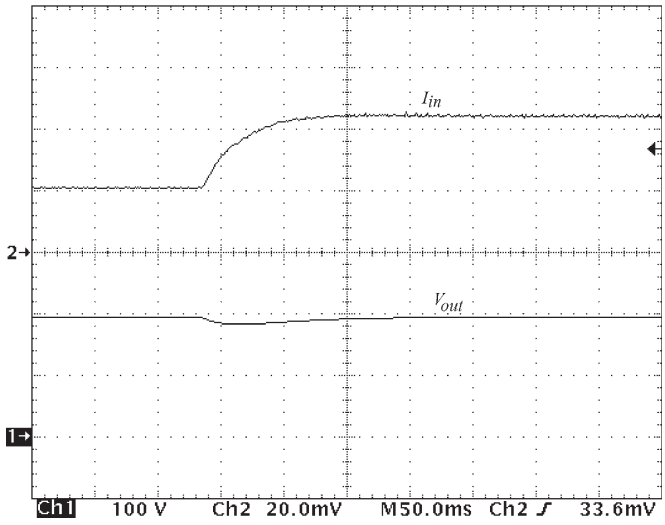


Fig. 17. Output voltage (100 V/div) and input current (4 A/div).

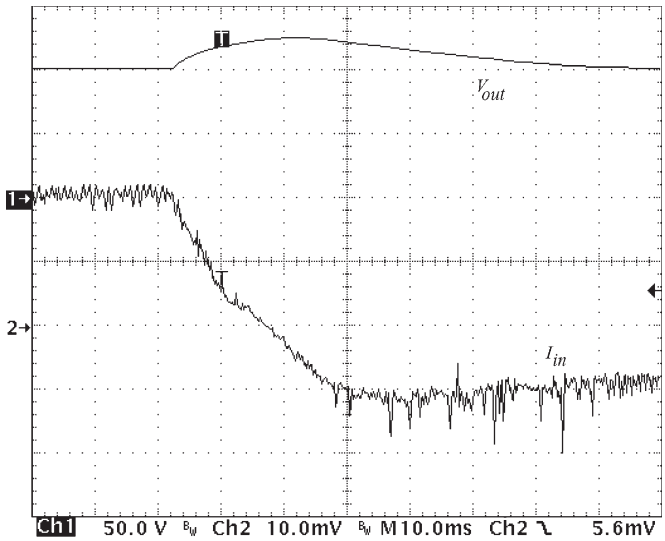


Fig. 18. Output voltage (50 V/div) and input current (2 A/div).

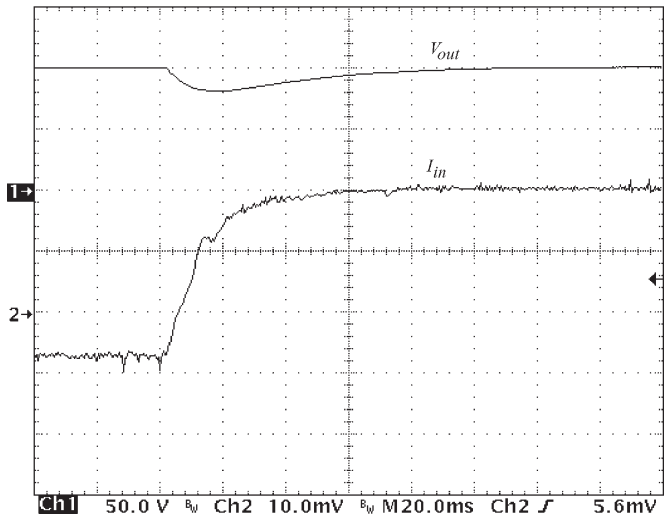


Fig. 19. Output voltage (50 V/div) and input current (2 A/div).

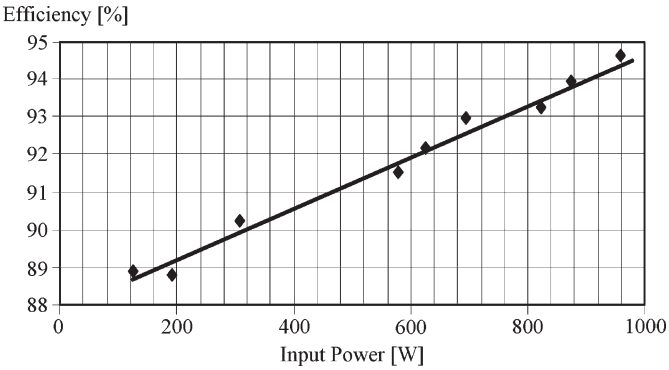


Fig. 20. Efficiency over the output range.

## VIII. Conclusion

In this paper, a step-up/step-down dc–dc ZVS PWM converter with active clamping technique, its qualitative analysis containing operational stage explanation and main theoretical waveforms, and an appropriate quantitative analysis have been presented.

Experimental results confirmed the operation under low loss conditions due to the soft commutation obtained for all the switches. As a consequence, a small heatsink, which reduced the weight, volume, and final costs, had been used.

Equally important, the proposed controller attended all the project goals and provided stable operation during all the practical tests, including load steps and regeneration current test.

Finally, the main advantages associated were the use of a small number of components, simple command strategy, robustness, reduced size and weight, and high efficiency.

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