ANALYSIS OF A MULTI-PHASE INTERLEAVED BIDIRECTIONAL DC/DC POWER CONVERTER WITH COUPLED INDUCTOR

Robson Mayer [1], Menaouar Berrehil El Kattel [1], Maicon Douglas Possamai [1],
Claudio Bruning [3], Sérgio Vidal Garcia Oliveira [1,2]

[1] Santa Catarina State University UDESC, Joinville, Santa Catarina, Brazil

[2] Blumenau Regional University FURB, Blumenau, Santa Catarina, Brazil

[3] Whirlpool Corporation, Benton Harbor, Michigan, USA

e-mail: mayerrobson@gmail.com, sergio_vidal@ieee.org

***Abstract* - This paper proposes a novel multi phase interleaved bi-directional dc/dc power converter to interface two dc sources of different voltage levels which applied for energy storage systems in high power level. The converter is proposed to reduce the input and output ripples, as well as, the size of passive components once the voltage and current ripple in the filters are four times higher than the switching frequency. A coupled inductor is employed to equal current splitting between the switch branch of the converter and obtain higher power density, and to reduce conduction loss, applying a multi phase interleaving technique. The operation and theoretical analysis of the converter are presented with different modes of power transfer. Furthermore, the key operational principle and simulation results are presented showing the converter operation in both directions of the power flow.**

***Keywords* – Bi-directional dc/dc converter, High-power dc/dc converter, Multi phase dc/dc converter, Interleaved operation, Coupled inductors.**

I. INTRODUCTION

There are many applications using or requiring energy storage in the industry, military, agriculture or aerospace such as hybrid/electric vehicle and in uninterrupted power supplies. Additionally, because of the limited space, almost all of these systems use accumulators or different energy buffers for safe, stable and flawless operation [1–4]. Power density is an important factor for these applications, as well as, high efficiency for system integration, so as not to reduce the effective power transfer capacity of the accumulators to the external system. Therefore the bi-directional dc/dc converters, are the key components for interfacing energy storage devices, such as batteries and ultracapacitors or supercapacitors, with various power systems, contributing to the stability of the bus voltage by controlling energy flows [5].

Figure 1 shows an energy storage system (ESS) consisting of batteries or ultracapacitors with a bi-directional dc/dc converter, and a dc/ac inverter. The dc/dc converter is indispensable for the applications that require voltage matching and power flow control between the two systems. Nevertheless, various bi-directional dc/dc converters have been proposed and studied as the interface to energy storage devices with focus on different applications [5–10]. Also, these buck-and-boost type converters are categorized as non-isolated and widely used at vast varying power and voltage levels in industry [11]. A number of non-isolated topologies are proposed in the literature [12], [13] to transfer the power from one source to another. Therefore the proposed circuit is based on the topologies presented in [9, 14, 15] and [16].

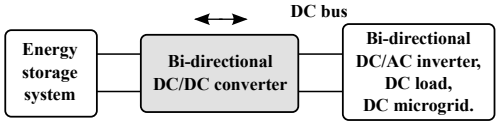


Fig. 1. Basic block diagram configuration for the ESS.

In this paper, a multi phase interleaved bi-directional dc/dc converter with coupled inductor (MIBIC) is proposed for the ESSs to interface the batteries/ultracapacitor and bi-directional dc/ac inverter, dc microgrid or other system that require energy storage. Figure 2 depicts the proposed circuit which is based on the converter presented in [15]. The proposed converter has in certain aspects some advantages over the others [9, 13–15] such as current splitting and rms current stress minimization in the semiconductors, increasing converter's efficiency, current ripple cancelation for $D = 1/4$ and $1/2$, reducing input current ripple, and minimum size of passive component make system more reliable in high power applications. This circuit provides a topology with high power density, improved efficiency to the family of non-isolated bi-directional dc/dc converters and high reliability for the system [10]. The interleaved operation with multiple phases allows the cancellation of the high-frequency switching current ripple in the input inductor obtaining as main advantages the filter's reduction, dynamic response and higher efficiency [15], [17], [18]. Therefore, the converter can become a promising candidate as a power electronic interface for an ESS.

The proposed converter, operating in continuous conduction mode (CCM), is studied and an idealized theoretical analysis is presented.

II. PROPOSED BIDIRECTIONAL DC/DC CONVERTER

The proposed topology is shown in Figure 2, it has three inductances where two of them are coupled (resulting a negative-coupled inductor), consists of a four-leg interleaved with eight switches, eight diodes, and two capacitors. During boost operation, $Q_{1b\ldots4b}$ are for pulse width modulation

(PWM) switching, and during buck operation, $Q_{1a...4a}$ are switching. When power flows from the low-voltage (LV) side or E_1 to the high-voltage (HV) side or E_2, the circuit works in boost mode to discharge the battery/ultracapacitors from the LV side, keeping the HV side at a desired level. In the other power flow direction, the circuit works in buck mode to recharge the battery/ultracapacitors.

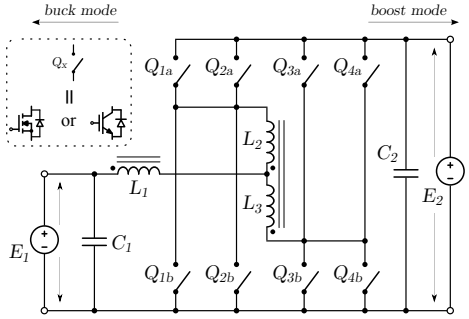
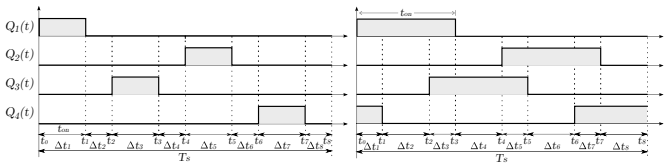


Fig. 2. Circuit schematic of proposed bi-directional dc/dc converter with coupled inductor (MIBIC).

The circuit has two operating regions, differentiated according to the Figure 3. Each one differs from the other by the number of overlapped switches. For each region, the duty cycle can assume different values, varies from 0 to $1/2$.

The driving signals sequence is important to providing a doubled ripple frequency on the coupled inductor and quadrupled ripple frequency in the input inductor current at the same switching frequency.



(a) (b)

Fig. 3. Power switch driving signals: (a) modulation scheme for $0 \leq D \leq 1/4$ region, (b) modulation for $1/4 \leq D < 1/2$ region.

The following sections will describe the operating principles and steady-state analysis for the both power flows direction.

III. ANALYSIS AND BASIC OPERATING PRINCIPLE

To explain the principle of the topology, the following assumptions are made: 1) the converter is operating in steady-state; 2) all the components have ideal characteristics without losses; 3) under steady-state operation the switches have an on time ($t_{on} = D\,T_s$) and the switching period is $T_s = 1/f_s$; 4) all switches have identical duty cycles, $\Delta t_1 = \Delta t_3 = \Delta t_5 = \Delta t_7$ and $\Delta t_2 = \Delta t_4 = \Delta t_6 = \Delta t_8$; 5) the coupled inductor has an infinite magnetizing inductance and unitary coupling factor; 6) the turn ratio of the coupled inductor is unitary ($n_L = 1{:}1$) ; 7) the capacitances are large enough to consider a constant output voltage; 8) the magnetic flux in the inductors is continuous, this means that the converter is operating in CCM; 9) the switching pattern is shifted by $\pi/2$.

A. Operational principle in boost mode

In the boost operation mode, power flows from the dc source E_1 to the load represented by it resistance R_1.

1) Operation in $D < 1/4$ region, with driving gate signals depicted in Figure 3(a):

First Stage [(t_0, t_1); see Fig. 4(a)]: Q_{1b} is ON, while Q_{2b}, Q_{3b} and Q_{4b} are turned OFF. The diodes D_{3a} and D_{4a} are forward biased. Meanwhile, the source provides energy to the circuit, the input inductor current increases linearly, and the energy stored in magnetizing inductance of the coupled inductor is transfers to the load. The inductor's voltage equations can be obtained from Kirchhoff's voltage law and are described by

$$v_{L1}(t) = E_1 - \frac{E_2}{2}\,; \qquad \Delta t_1 = t_1 - t_0 = D\,T_s \tag{1}$$

$$v_{L2}(t) = \frac{E_2}{2}\,; \qquad v_{L3}(t) = -\frac{E_2}{2} \tag{2}$$

Second Stage (t_1, t_2), Fourth Stage (t_3, t_4), Sixth Stage (t_5, t_6), and *Eighth Stage (t_7, t_8); [see Fig. 4(b)]:* During this intervals, all the switchs is turned OFF at t_2, t_4, t_6 and t_8, respectively. All diodes D_{1a}, D_{2a}, D_{3a} and D_{4a} are forward biased. Meanwhile, the source provides energy to the whole circuit, the input inductor current decreases linearly, and the energy stored in magnetizing inductances still transfers to the load and output capacitor C_2 .

$$v_{L1}(t) = E_1 - E_2\,; \qquad \Delta t_2 = t_2 - t_1 = \frac{1 - 4\,D}{4}\,T_s \tag{3}$$

$$v_{L2}(t) = 0\,; \qquad v_{L3}(t) = 0 \tag{4}$$

Third Stage [(t_2, t_3); see Fig. 4(c)]: At t_2, the Q_{3b} is turned ON, D_{1a} and D_{2a} begin conducting. Some of the energy from dc source is transferred to the coupled inductor and the other to the load. The inductor's voltage equations of the coupled inductor can be presented as follows:

$$v_{L2}(t) = -\frac{E_2}{2}\,; \qquad v_{L3}(t) = \frac{E_2}{2} \tag{5}$$

Fifth Stage [(t_4, t_5); see Fig. 4(d)]: This is the same as first stage. At t_4, the Q_{2b} is turned ON, and D_{3a} and D_{4a} begin conducting.

Seventh Stage [(t_6, t_7); see Fig. 4(e)]: This is the same as third stage. At t_6, the Q_{4b} is turned ON, and D_{1a} and D_{2a} begin conducting. The diodes D_{3a} and D_{4a} are reverse biased.

2) Operation in $1/4 \leq D < 1/2$ region, with driving gate signals depicted in Figure 3(b):

First Stage [(t_0, t_1); see Fig. 5(a)]: Q_{1b} and Q_{4b} are ON, and all of diodes $D_{1a...4a}$ are reverse biased. The inductors store energy from power dc source, the current increases linearly, the output capacitor C_2 discharge and feeds the load. The voltage equations across the coupled inductor is given by (4), and the input inductor can be presented as follows:

$$v_{L1}(t) = E_1\,; \qquad \Delta t_1 = \frac{4\,D - 1}{4}\,T_s \tag{6}$$

Second Stage [(t_1, t_2); see Fig. 4(a)]: This is the same as first stage for $D < 1/4$ region. At t_1, the Q_{4b} is turned OFF but Q_{1b} is still in the turn-on state, and D_{3a} and D_{4a} begin

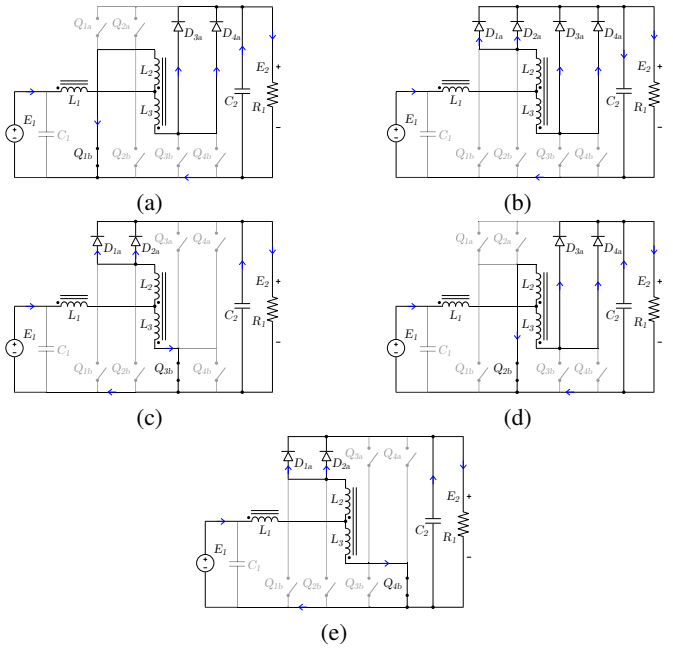


Fig. 4. Topological stages of the proposed converter for boost mode ($D \leq 1/4$): (a) state $[t_0, t_1]$, (b) states $[t_1, t_2]$, $[t_3, t_4]$, $[t_5, t_6]$ and $[t_7, t_8]$, (c) state $[t_2, t_3]$, (d) state $[t_4, t_5]$, (e) state $[t_6, t_7]$.

conducting. The voltage equations across the inductor's are given by (1), (2) and by

$$\Delta t_2 = \frac{1-2\,D}{2}\,T_s \tag{7}$$

Third Stage [(t_2, t_3); see Fig. 5(b)]: Q_{1b} is still in the turn-on state and at t_2 the Q_{3b} is turned ON. This interval is similar to the first stage.

Fourth Stage [(t_3, t_4); see Fig. 4(c)]: This interval is similar to the third stage for $D < 1/4$ region. At t_3, the Q_{1b} is turned OFF but Q_{3b} is still in the turn-on state, and D_{1a} and D_{2a} begin conducting. The voltage equations of the coupled inductor can is given by (5).

Fifth Stage [(t_4, t_5); see Fig. 5(c)]: In this interval, Q_{3b} is still in the turn-on state and at t_4 the Q_{2b} is turned ON. This interval is similar to the first and third stages.

Sixth Stage [(t_5, t_6); see Fig. 4(d)]: This is similar to the fifth stage for $D < 1/4$ region. At t_5, the Q_{3b} is turned OFF but Q_{2b} is still in the turn-on state, D_{3a} and D_{4a} begin conducting. The voltage across the inductors is the same as second stage.

Seventh Stage [(t_6, t_7); see Fig. 5(d)]: Q_{2b} is still in the turn-on state and at t_6 the Q_{4b} is turned ON. This interval is similar to the first, third and fifth stages.

Eighth Stage [(t_7, t_8); see Fig. 4(e)]: This is similar to the seventh stage for $D < 1/4$ region. At t_7, the Q_{2b} is turned OFF but Q_{4b} is still in the turn-on state, D_{1a} and D_{2a} begin conducting. The voltage across the inductors is the same as fourth stage.

The expression of voltage gain, for a CCM of the proposed converter, can be obtained from the analysis of the average voltage across the inductor L_1 as:

$$\overline{V_L}(t) = \frac{4}{T_s}\left[\int_0^{\Delta t_1} v_{L1}(t)\,dt + \int_0^{\Delta t_2} v_{L1}(t)\,dt\right] = 0 \tag{8}$$

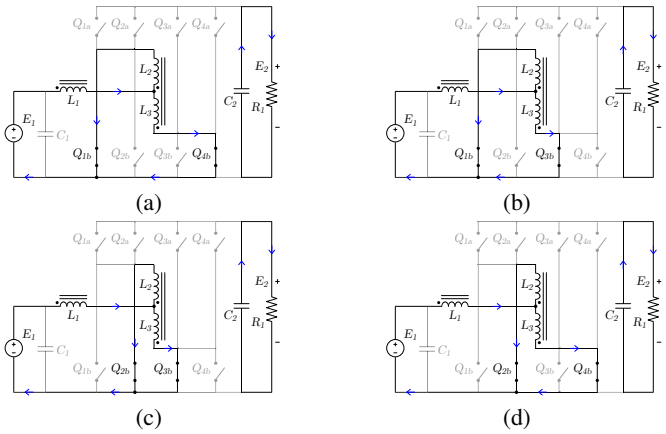


Fig. 5. Topological stages of the proposed converter for boost mode ($1/4 \leq D < 1/2$): (a) state $[t_0, t_1]$, (b) state $[t_2, t_3]$, (c) state $[t_4, t_5]$, (d) state $[t_6, t_7]$.

By substituting the inductor's voltage (1) and (3), or (6) and (1) into (8), the voltage gain in boost operation mode of the converter is given by

$$M_1 = \frac{E_2}{E_1} = \frac{1}{1-2\,D} \tag{9}$$

The DC voltage gain of the proposed converter in boost operating are represented graphically in Figure 8(a), and compared to the classic Boost converter which is the same as [9].

The average value of the inductors current can be obtained as:

$$E_1 \cdot I_{L1} = E_2 \cdot I_{R1}\,; \qquad I_{L1} = \frac{E_2}{(1-2\,D)\,R_1} \tag{10}$$

$$I_{L2} = I_{L3} = \frac{E_2}{2\,(1-2\,D)\,R_1} \tag{11}$$

B. Operational principle in buck mode

In the buck operation mode, power flows from the dc source E_2 to the load represented by it resistance R_2 .

1) Operation in $D < 1/4$ region:

First Stage [(t_0, t_1); see Fig. 6(a)]: At t_0, Q_{1a} is ON, while $Q_{2a\ldots4a}$ are turned OFF. The diodes D_{3b} and D_{4b} are forward biased. Meanwhile, the source provides energy to the circuit, the output inductor current increases linearly, and the energy stored in magnetizing inductance of the coupled inductor is transfers to the load and output capacitor C_1 . The voltage equations across the coupled inductor is given by (2), and the output inductor can be presented as follows:

$$v_{L1}(t) = \frac{E_2}{2} - E_1 \tag{12}$$

Second Stage (t_1, t_2), Fourth Stage (t_3, t_4), Sixth Stage (t_5, t_6), and *Eighth Stage (t_7, t_8); [see Fig. 6(b)]:* During this intervals, all the switchs is turned OFF at t_2, t_4, t_6 and t_8, respectively. All diodes $D_{1b\ldots4b}$ are forward biased. The voltage across the coupled inductor is given by (4).

$$v_{L1}(t) = -E_1 \tag{13}$$

Third Stage [(t_2, t_3); see Fig. 6(c)]: At t_2, the Q_{3a} is turned ON, D_{1b} and D_{2b} begin conducting. The voltage equations of

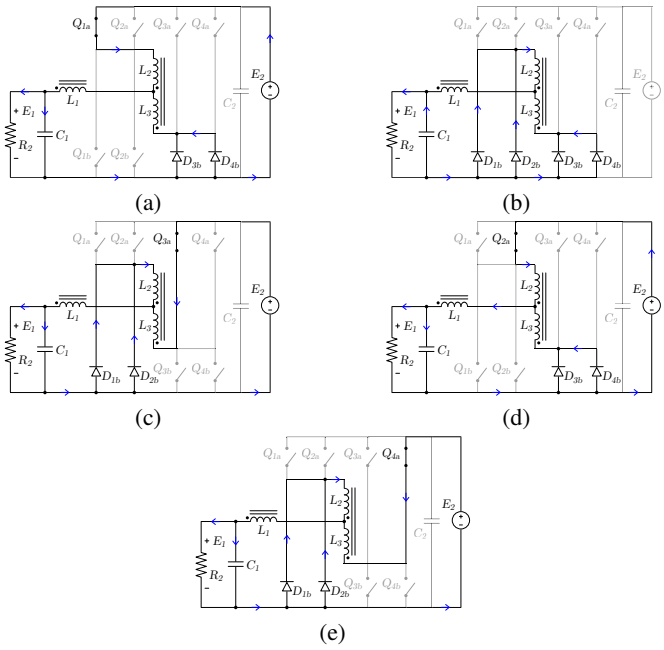


Fig. 6. Topological stages of the proposed converter for buck mode ($D \leq 1/4$): (a) state $[t_0, t_1]$, (b) states $[t_1, t_2]$, $[t_3, t_4]$, $[t_5, t_6]$ and $[t_7, t_8]$, (c) state $[t_2, t_3]$, (d) state $[t_4, t_5]$, (e) state $[t_6, t_7]$.

the coupled inductor is given by (5), and the output inductor is given by (12).

Fifth Stage [(t_4, t_5); see Fig. 6(d)]: This is the same as first stage. At t_4, the Q_{2a} is turned ON, and D_{3b} and D_{4b} begin conducting.

Seventh Stage [(t_6, t_7); see Fig. 6(e)]: This is the same as third stage. At t_6, the Q_{4a} is turned ON, and D_{1b} and D_{2b} begin conducting. The diodes D_{3b} and D_{4b} are reverse biased.

2) Operation in $1/4 \leq D < 1/2$ region:

First Stage [(t_0, t_1); see Fig. 7(a)]: Q_{1a} and Q_{4a} are ON, and all of diodes $D_{1b...4b}$ are reverse biased. The inductors store energy from power dc source, the current increases linearly, the output capacitor C_1 charge. The voltage equations across the coupled inductor is given by (4), and the output inductor can be presented as follows:

$$v_{L1}(t) = E_2 - E_1 \tag{14}$$

Second Stage [(t_1, t_2); see Fig. 6(a)]: This is the same as first stage for $D < 1/4$ region. At t_1, the Q_{4a} is turned OFF but Q_{1a} is still in the turn-on state. The voltage equations across the inductors are given by (12) and (2).

Third Stage [(t_2, t_3); see Fig. 7(b)]: Q_{1a} is still in the turn-on state and at t_2 the Q_{3a} is turned ON. This interval is similar to the first stage.

Fourth Stage [(t_3, t_4); see Fig. 6(c)]: This interval is similar to the third stage for $D < 1/4$ region. At t_3, the Q_{1a} is turned OFF but Q_{3a} is still in the turn-on state. The voltage equations of the coupled inductor is given by (5).

Fifth Stage [(t_4, t_5); see Fig. 7(c)]: In this interval, Q_{3a} is still in the turn-on state and at t_4 the Q_{2a} is turned ON. This interval is similar to the first and third stages.

Sixth Stage [(t_5, t_6); see Fig. 6(d)]: This is similar to the fifth stage for $D < 1/4$ region. At t_5, the Q_{3a} is turned OFF

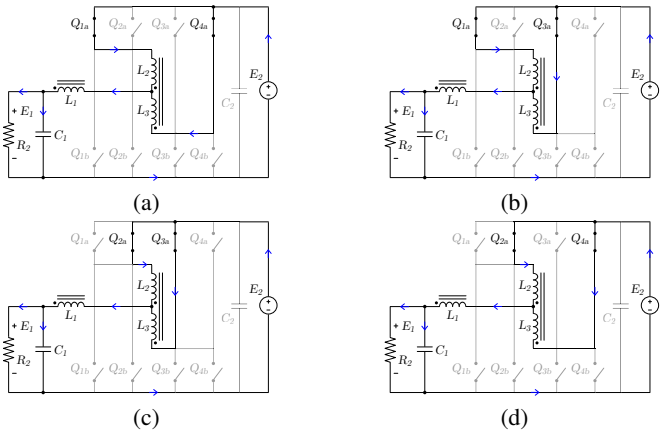


Fig. 7. Topological stages of the proposed converter for buck mode ($1/4 \leq D < 1/2$): (a) state $[t_0, t_1]$, (b) state $[t_2, t_3]$, (c) state $[t_4, t_5]$, (d) state $[t_6, t_7]$.

but Q_{2a} is still in the turn-on state, and D_{3b} and D_{4b} begin conducting. The voltage across the inductors is the same as second stage.

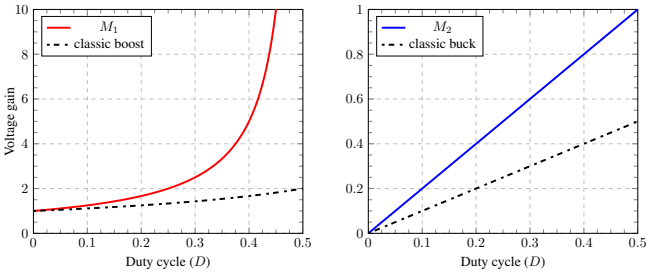
Seventh Stage [(t_6, t_7); see Fig. 7(d)]: Q_{2a} is still in the turn-on state and at t_6 the Q_{4a} is turned ON. This interval is similar to the first stage. This interval is similar to the first, third and fifth stages.

Eighth Stage [(t_7, t_8); see Fig. 6(e)]: This is similar to the seventh stage for $D < 1/4$ region. At t_7, the Q_{2a} is turned OFF but Q_{4a} is still in the turn-on state, D_{1b} and D_{2b} begin conducting. The voltage across the inductors is the same as fourth stage.

Applying a volt-second balance on the magnetizing inductor (8), we get the voltage gain with (12) and (13), or (14) and (12). Then, the voltage gain in buck operation of the converter is given by

$$M_2 = \frac{E_1}{E_2} = 2\,D \tag{15}$$

The DC voltage gain of the proposed converter in buck operating are represented graphically in Figure 8(b), and compared to the classic Buck converter which is the same as [14].



(a) (b)

Fig. 8. DC voltage gain characteristic of the converter in: (a) boost mode, and (b) buck mode.

Expression (16) can be used to determine the current ripple (ΔI_{L1}) or to calculate the input inductance (L_1) in boost mode for CCM, which is valid within the range of variation of the

duty cycle $1/4 \leq D < 1/2$.

$$L_1 = \frac{E_1\,(4\,D-1)}{4\,\Delta I_{L1}\,f_s} \tag{16}$$

IV. SIMULATION RESULTS

To verify the operational principles and the steady-state analysis, OrCAD simulation is conducted. The simulation parameters for operating in both directions are presented in Table I. The simulation waveforms are presented below.

TABLE I
Simulation parameters

$P = 50\,\text{kW}$	Nominal Power
$E_1 = 200\,V$; $E_2 = 600\,V$	Nominal Input / Output Voltage
$f_s = 20\,\text{kHz}$	Switching Frequency
$D = 0.333$; $D = 0.167$	Duty Cycle = boost mode ; buck mode
$\Delta E_1 = 10\,V$; $\Delta E_2 = 30\,V$	Output Voltage Ripple
$\Delta I_{L1} = 30\,A$	Current Ripple
$L_1 = 28\,\mu\text{H}$; $L_2 = L_3 = 26.5\,\mu\text{H}$; $C_1 = 5\,\mu\text{F}$; $C_2 = 12\,\mu\text{F}$	

The current waveforms across the inductors are illustrated in Figure 9, for boost mode operation. Figure 10, shows the load current and output voltage.

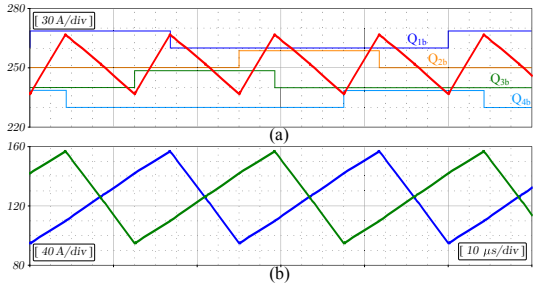


Fig. 9. Boost mode operations: (a) inductor current I_{L1} and switch driving signals, (b) coupled inductor current I_{L2} and I_{L3}.

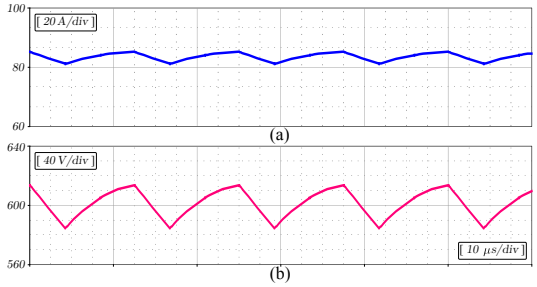


Fig. 10. Boost mode operations: (a) output current I_{R1}, and (b) output voltage E_2.

Figure 11, shows the current waveforms across the inductors when the duty cycle is $1/4$, for buck mode operation.

The current of the source E_2 and the ripple output voltage for duty cycle 0.167 in buck mode, are illustrated in Figure 12.

Table II shows the comparison of the proposed topology with others circuits [9, 15] in the boost operation mode with the specifications shown in Table I. We can notice that the proposed has the smallest inductance, low rms current

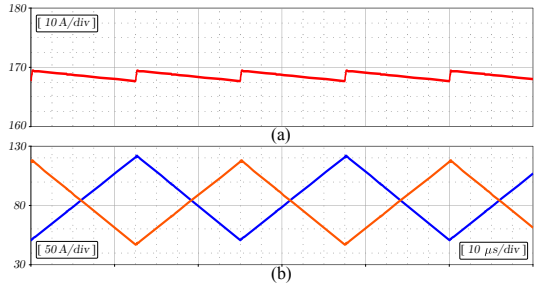


Fig. 11. Buck mode operations for $D = 0.25$: (a) output inductor current I_{L1}, and (b) coupled inductor current I_{L2} and I_{L3}.

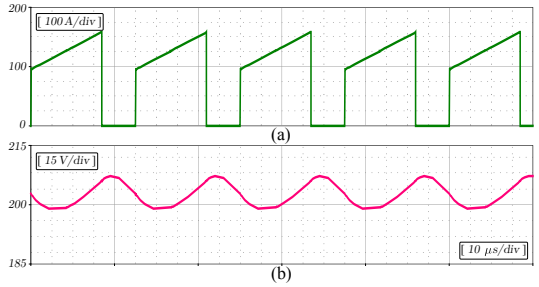


Fig. 12. Buck mode operations: (a) input current I_{E2}, and (b) output voltage E_1.

on the devices, and reduced dc-link capacitance. The main drawbacks of the interleaved converters is the high number of semiconductor devices and gate driver circuits.

TABLE II
Comparison of the dc/dc converter topologies

	f_s	Inductor L_1	Current ripple freq.	Capacitor C_2	Duty cycle	RMS current; Switch / Diode
Classic Boost	80 kHz	55.5 µH	f_s	23 µF	0.665	206 A / 145 A
Boost NCI [9]	40 kHz	28 µH	$2 \cdot f_s$	12 µF	0.664	104 A / 73 A
MDIBC [15]	20 kHz	56 µH	$2 \cdot f_s$	12 µF	0.332	73.4 A / 36.7 A
Proposed	20 kHz	28 µH	$4 \cdot f_s$	12 µF	0.333	73.5 A / 36.7 A

V. CONCLUSION

The paper presented a multi phase interleaved bi-directional dc/dc converter for energy storage systems applications and describes the principle of operation of the converter for bi-directional power flow. The converter provides a bi-directional power transfer between the external electrical system and the energy storage elements, and the interleaving technique decreases the conduction losses and capacitor/inductor size through ripple cancellation. Simulation results showed that the proposed topology is able to manage bi-directional power flow between the batteries / supercapacitors and the dc bus. The newly converter circuit offers the following improvements over existing circuits [9, 10, 14, 15]. (i) This topology uses only eight switches with antiparallel diodes and two magnetic elements to achieve bi-directional power flow. (ii) Reduced

current and voltage ripples by four times. (iii) Decreasing current ratings of power electronic devices. (iv) Improves the efficiency under light loads, and a phase shedding technique can be applied [19]. Thereby, the authors believe that the converter is competitive and qualified for special applications such as high-power (used above kW level) in electric, hybrid or fuel cell vehicles and uninterrupted power supplies that require a reduced input ripple current to extend its lifetime, lower weight and volume.

ACKNOWLEDGEMENT

The authors would like to thank to CAPES and PROMOP/UDESC for scholarship support, the FITEJ and FAPESC for financial support.

REFERENCES

[1] E. Chemali, M. Preindl, P. Malysz, and A. Emadi, "Electrochemical and electrostatic energy storage and management systems for electric drive vehicles: State-of-the-art review and future trends," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 1117–1134, September 2016.

[2] Y.-S. Lin, K.-W. Hu, T.-H. Yeh, and C.-M. Liaw, "An electric-vehicle ipmsm drive with interleaved front-end dc/dc converter," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 6, pp. 4493–4504, June 2016.

[3] A. Ostadi, M. Kazerani, and S.-K. Chen, "Hybrid energy storage system (hess) in vehicular applications: A review on interfacing battery and ultra-capacitor units," in *Transportation Electrification Conference and Expo (ITEC), 2013 IEEE*. IEEE, June 2013, pp. 1–7.

[4] D. M. Sable, F. C. Lee, and B. H. Cho, "A zero-voltage-switching bidirectional battery charger/discharger for the nasa eos satellite," in *Applied Power Electronics Conference and Exposition, 1992. APEC'92. Conference Proceedings 1992., Seventh Annual*. IEEE, February 1992, pp. 614–621.

[5] G. Wang, G. Konstantinou, C. D. Townsend, J. Pou, S. Vazquez, G. D. Demetriades, and V. G. Agelidis, "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Transactions on Sustainable Energy*, vol. 7, no. 4, pp. 1778–1790, October 2016.

[6] M. B. El Kattel, R. Mayer, and S. V. G. Oliveira, "Analysis and simulation of a three-phase push-pull/flyback interleaved bidirectional dc-dc converter," in *Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE*. IEEE, October 2016, pp. 1274–1279.

[7] K. Tytelmaier, O. Husev, O. Veligorskyi, and R. Yershov, "A review of non-isolated bidirectional dc-dc converters for energy storage systems," in *Applied Physics and Engineering (YSF), 2016 II International Young Scientists Forum on*. IEEE, October 2016, pp. 22–28.

[8] M. B. El Kattel, R. Mayer, and S. V. G. Oliveira, "A three-phase flyback current-fed push-pull bidirectional dc-dc converter for dc microgrid application," in *Industry Applications (INDUSCON), 2016 12th IEEE International Conference on*. IEEE, November 2016, pp. 1–6.

[9] H. Wu, J. Lu, W. Shi, and Y. Xing, "Nonisolated bidirectional dc–dc converters with negative-coupled inductor," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2231–2235, May 2012.

[10] F. J. de Brito, R. P. Torrico-Bascopé, S. Daher, and G. V. Torrico-Bascopé, "Comparative analysis of three dc-dc non-isolated buck converters," in *Industry Applications (INDUSCON), 2012 10th IEEE/IAS International Conference on*. IEEE, November 2012, pp. 1–8.

[11] R. Mayer, A. Péres, and S. V. G. Oliveira, "Conversor cc-cc multifásico bidirecional em corrente não isolado aplicado a sistemas elétricos de tração de veículos elétricos e híbridos," *Revista de Eletrônica Sobraep, Brazil*, vol. 20, no. 3, pp. 311–321, August 2015.

[12] Y.-F. Wang, L.-K. Xue, C.-S. Wang, P. Wang, and W. Li, "Interleaved high-conversion-ratio bidirectional dc–dc converter for distributed energy-storage systemscircuit generation, analysis, and design," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5547–5561, August 2016.

[13] A. K. Rathore, D. R. Patil, and D. Srinivasan, "Non-isolated bidirectional soft-switching current-fed lcl resonant dc/dc converter to interface energy storage in dc microgrid," *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1711–1722, March/April 2016.

[14] J. P. R. Balestero, F. L. Tofoli, G. V. Torrico-Bascopé, and F. J. M. de Seixas, "A dc–dc converter based on the three-state switching cell for high current and voltage step-down applications," *IEEE transactions on power electronics*, vol. 28, no. 1, pp. 398–407, January 2013.

[15] O. Hegazy, J. Van Mierlo, and P. Lataire, "Analysis, modeling, and implementation of a multidevice interleaved dc/dc converter for fuel cell hybrid electric vehicles," *IEEE transactions on power electronics*, vol. 27, no. 11, pp. 4445–4458, November 2012.

[16] O. Hegazy, M. El Baghdadi, J. Van Mierlo, P. Lataire, and T. Coosemans, "Analysis and modeling of a bidirectional multiport dc/dc power converter for battery electric vehicle applications," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*. IEEE, August 2014, pp. 1–12.

[17] J. Zhang, J.-S. Lai, R.-Y. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc–dc converter," *IEEE Transactions on power electronics*, vol. 22, no. 4, pp. 1145–1153, July 2007.

[18] O. Garcia, P. Zumel, A. De Castro, and A. Cobos, "Automotive dc-dc bidirectional converter made with many interleaved buck stages," *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 578–586, May 2006.

[19] J.-B. Baek, W.-I. Choi, and B.-H. Cho, "Digital adaptive frequency modulation for bidirectional dc–dc converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 5167–5176, November 2013.