

A ZVS PWM Three-Phase Inverter with Active Clamping Technique Using the Reverse Recovery Energy of the Diodes

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Abstract - This paper presents the analysis of a ZVS PWM Three-Phase Inverter with active voltage clamping technique using the reverse recovery energy of the diodes to improve the converter efficiency. The structure is particularly simple and robust. It is very attractive for Three Phase high power applications. Conduction and commutation losses are reduced due to implementation of a simple active snubber circuit that provides ZVS conditions for all switches, including the auxiliary one. Its main features are: Simple control strategy, robustness, lower weight and volume, lower harmonic distortion of the output current, and high efficiency. The operation principle for steady-state conditions, mathematical analysis and experimental results from a laboratory prototype are presented.

I. INTRODUCTION

With the appearance of the Bipolar Transistors in the 50s and posteriori the Mosfets in the 80s, PWM modulation techniques could be used together with the increase of the commutation frequency, with the aim to reduce the harmonic distortion in the output of the inverters. These measures give some benefits like the reduction of the volume and weight of the filters and magnetic elements; nevertheless they cause some difficulties due to the high commutation losses in the switches, which reduce the converter efficiency, and the electromagnetic interference appearing. This event occurs mainly in inverter topologies that use the bridge configuration; where the main switch conduction provoke the reverse recovery phenomenon of the anti-parallel diode of the complementary switch. A great number of works have been developed by power electronics scientific community, with the aim to diminish these problems. They can be divided in two groups: passive techniques [6, 7, 8, 9] and active techniques [1, 2, 3, 10, 11].

In the active techniques area, some researches were made recently using the reverse-recovery energy from the diodes to obtain soft commutation in the switches of the pre-regulated rectifiers with high power factor [4, 5].

In this paper a ZVS PWM Three-Phase Inverter with voltage clamping across the switches, using only a single auxiliary switch, is presented. The proposed structure uses the diode reverse recovery energy technique to obtain soft commutation in all switches.

This topology presents some advantages in comparison with

the conventional soft commutation inverters studied in the literature, which we can print out:

- Soft commutation in all load range;
- Simple topology with a low number of components;
- Use a classical PWM modulation;
- Auxiliary switch works with constant duty cycle in all operation stages;
- Use of slow and low cost rectifiers diodes;
- Low clamping voltage across the capacitor;
- Low current stress through the main switches;
- Simple design procedure with low restrictions;
- High efficiency.

II. PROPOSED CIRCUIT

The proposed circuit is shown in Fig. 1. It presents a Three-Phase inverter configuration, where **Q1, Q2, Q3, Q4, Q5** and **Q6** are the main switches, and **Qa** is the auxiliary switch. **C1, C2, C3, C4, C5** and **C6** are the commutation capacitors.

One controlled switch **Qa**, with anti-parallel diode **Da**, one small inductor **Ls** and one clamping capacitor **Cs** form the snubber circuit. The capacitor **Cs** is responsible by the storage of the diode reverse recovery energy and by the clamping of switches voltage. The inductor **Ls** is responsible by the control of the di/dt during the diode reverse recovery time. The auxiliary switch works with constant duty cycle in all operation stage. One of the most advantages of this converter consists in the use of only one auxiliary switch, which provides the clamping of the voltage and the ZVS conditions for all switches, including the auxiliary switch in the snubber circuit.

III. OPERATION STAGES

The inverter has symmetrical operation stages, so, will be presented the analysis to only one combination of the load currents. To simplify the studies, the following assumptions are made: the operation of the circuit is steady state; the semiconductors are considered ideal (excluding the reverse recovery of the diodes); the voltage across the capacitor **Cs**, and the current in the output inductors are considered constant during the switching period. The main waveforms are shown in Fig. 2 and Fig. 3 shows the main operation stages.

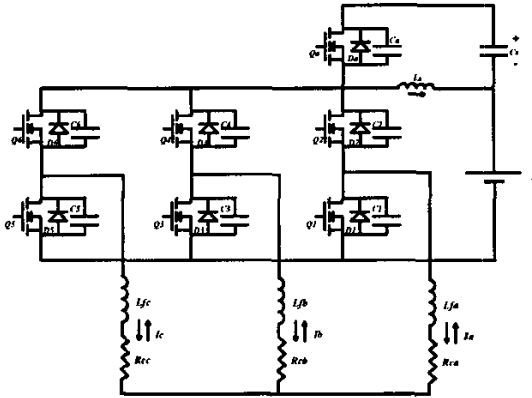


Fig. 1. Proposed Circuit.

First stage (t0-t1): At this stage, the current I_a flows through the circuit formed by inductor L_s , source V_l and diode D_5 . The current I_b flows through the diode D_4 and current I_c flows through the diode D_2 . At same time, the additional current iL_s flows through Q_a , L_s e C_s .

Second stage (t1-t2): This stage starts when the auxiliary switch Q_a is blocked. The current iL_s begins the charge of the capacitor C_a from zero to $E+V_{cs}$, and discharges C_1 , C_3 and C_6 from $E+V_{cs}$ to zero.

Third stage (t2-t3): At this stage the voltage across C_1 , C_3 and C_6 reaches zero, and are clamping by the anti-parallel diodes D_1 , D_3 and D_6 . So, the switches Q_1 , Q_3 and Q_6 conduct with ZVS condition. At this moment, the bus voltage E is applied across the inductor L_s and the current iL_s decrease linearly.

Fourth stage (t3-t4): It begins when the current iL_s inverts its direction and flows through the switches Q_1 , Q_3 and Q_6 . The current iL_s continues to decrease until inverting its direction of current of the diodes D_2 , D_4 and D_5 , starting its reverse recovery phase. The inductor L_s limits the diL_s/dt .

Fifth stage (t4-t5): This stage starts when the diodes D_2 , D_4 and D_5 finish its reverse recovery phase. The current iL_s begins the charge of the capacitors C_2 , C_4 and C_5 from zero to $E + V_{cs}$ and the discharge of C_a from $E + V_{cs}$ to zero.

Sixth stage (t5-t6): At this stage the voltage across the capacitor C_a reaches zero, and it is clamped by the diode D_a . Thus, the auxiliary switch Q_a conducts with zero-voltage switching. The current iL_s increases, due the application of the voltage V_{cs} across the inductor L_s .

Seventh stage (t6-t7): This stage begins when the current iC_s changes its direction and flows through the switch Q_a . The current iL_s continues to increase linearly.

Eighth stage (t7-t8): At this stage the switch Q_1 is blocked. The capacitor C_1 charges itself from zero to $E + V_{cs}$ and the capacitor C_2 discharges itself from $E + V_{cs}$ to zero.

Ninth stage (t8-t9): It begins when the voltage across the capacitor C_2 reaches zero, and it is clamped by the diode D_2 . The current iL_s continues increasing.

Tenth stage (t9-t10): At this stage the switch Q_3 is blocked. The capacitor C_3 charges itself from zero to $E + V_{cs}$ and the capacitor C_4 discharges itself from $E + V_{cs}$ to zero.

Eleventh stage (t11-t12): It begins when the voltage across the capacitor C_4 reaches zero, and it is clamped by the diode D_4 . The current iL_s continues increasing.

Twelfth stage (t12-t0): At this stage the switch Q_6 is blocked. The capacitor C_6 charges itself from zero to $E + V_{cs}$ and the capacitor C_5 discharges itself from $E + V_{cs}$ to zero. This stage finishes when the voltage across the capacitor C_5 reaches zero, and it is clamped by the diode D_5 , restarting the first operation stage.

IV. MATHEMATICAL ANALYSIS OF THE SOFT-SWITCHING CIRCUIT

To guarantee ZVS conditions, it is necessary, in the second stage, that the stored energy in the inductor L_s be sufficient to discharge the capacitor C_1 , C_3 and C_6 and to charge C_a . Thus, by inspection of Fig. 3 (Interval t1-t2) the following condition can be formulated:

$$L_s I_f^2 \geq (C_a + C_1 + C_3 + C_6)(V + V_g)^2 \quad (1)$$

Where I_f is the maximum current in C_s , and V_{cs} is maintained constant during a switching period. Assuming $V_{cs} \ll E$ we have:

$$I_f \min \geq E \sqrt{\frac{C_a + C_1 + C_3 + C_6}{L_s}} \quad (2)$$

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor C_s .

In the steady state conditions the clamping capacitor average current must be zero. Thus:

$$iC_{s_{av}} = \frac{1}{T_s} \left[\int_0^{t_7} \left(\frac{V_{cs}}{L_s} \cdot t - 3I_r \right) dt + \int_{t_7}^{t_9} \left(\frac{V_{cs}}{L_s} \cdot t - 3I_r - I_c \right) dt + \int_{t_9}^{t_{11}} \left(\frac{V_{cs}}{L_s} \cdot t - 3I_r - I_c - I_b \right) dt + \int_{t_{11}}^{t_{12}} \left(\frac{V_{cs}}{L_s} \cdot t - 3I_r - I_c - I_b - I_a \right) dt \right] \quad (3)$$

Where T_s is the switching period.

Solving the integral equation, and considering:

$$D_1 = \frac{t_7}{T_s}; \quad D_3 = \frac{t_9}{T_s}; \quad D_6 = \frac{t_{11}}{T_s}; \quad t_1 \approx T_s; \quad iC_{s_{av}} = 0 \quad (4)$$

We have:

$$V_{cs} = \frac{2L_s}{T_s} [3 \cdot I_r + I_a(2 - D_1 - D_6) + I_b(D_1 - D_3)] \quad (5)$$

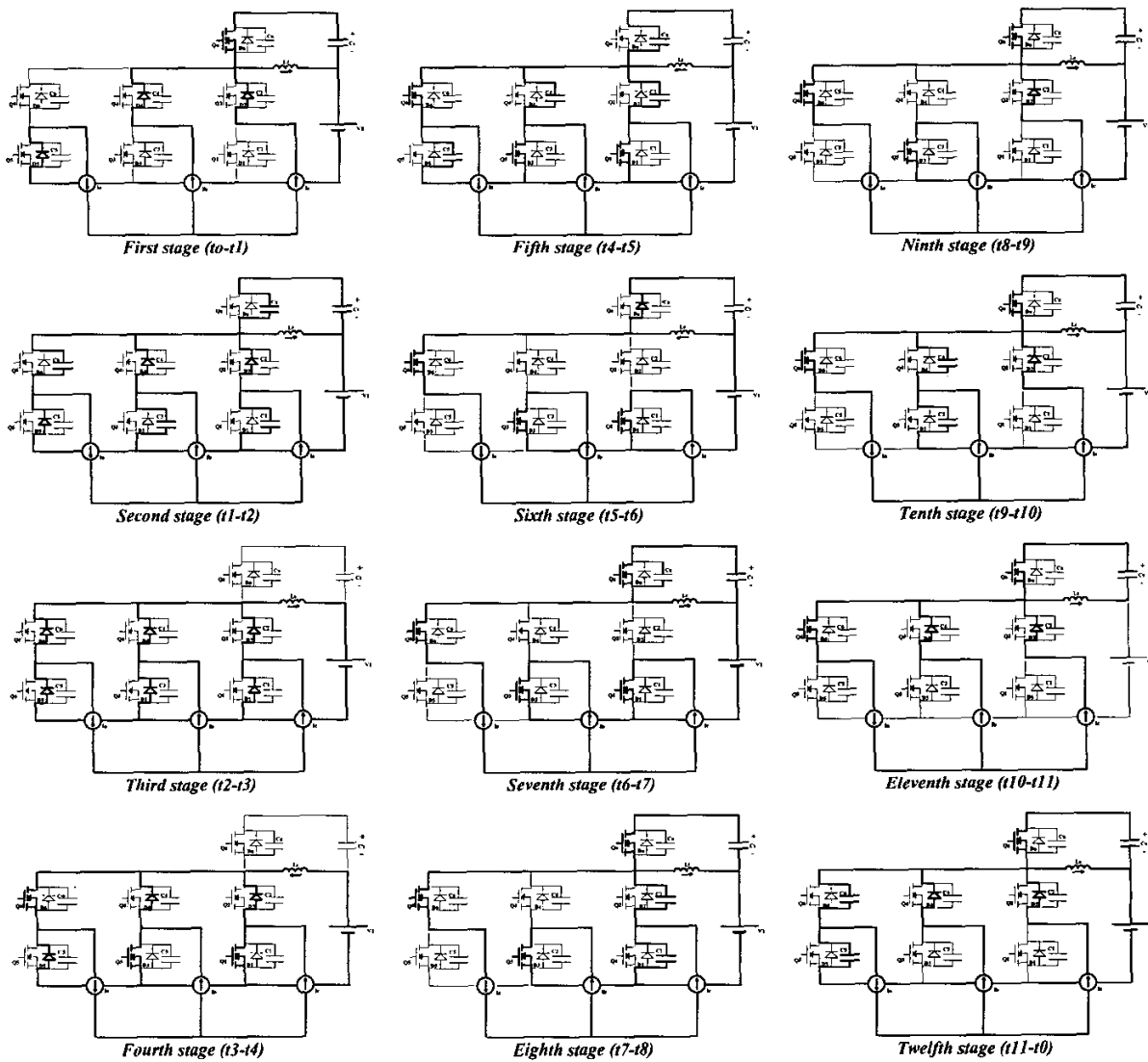


Fig. 2. Operation Stage

The output currents are given by:

$$I_a = \frac{E \cdot ma}{2 \cdot Z_{ca}} \cdot \text{sen } \omega t \tag{6}$$

$$I_b = \frac{E \cdot ma}{2 \cdot Z_{cb}} \cdot \text{sen} \left(\omega t - \frac{2 \cdot \pi}{3} \right) \tag{7}$$

$$I_c = \frac{E \cdot ma}{2 \cdot Z_{cc}} \cdot \text{sen} \left(\omega t - \frac{4 \cdot \pi}{3} \right) \tag{8}$$

$$Z_{ca} = \sqrt{R_{ca}^2 + (\omega \cdot L_{ca})^2} \tag{9}$$

$$Z_{cb} = \sqrt{R_{cb}^2 + (\omega \cdot L_{cb})^2} \tag{10}$$

$$Z_{cc} = \sqrt{R_{cc}^2 + (\omega \cdot L_{cc})^2} \tag{11}$$

R_{ca} , R_{cb} e R_{cc} – Load resistances;

L_{ca} , L_{cb} e L_{cc} – Load inductances

The load impedance are given by:

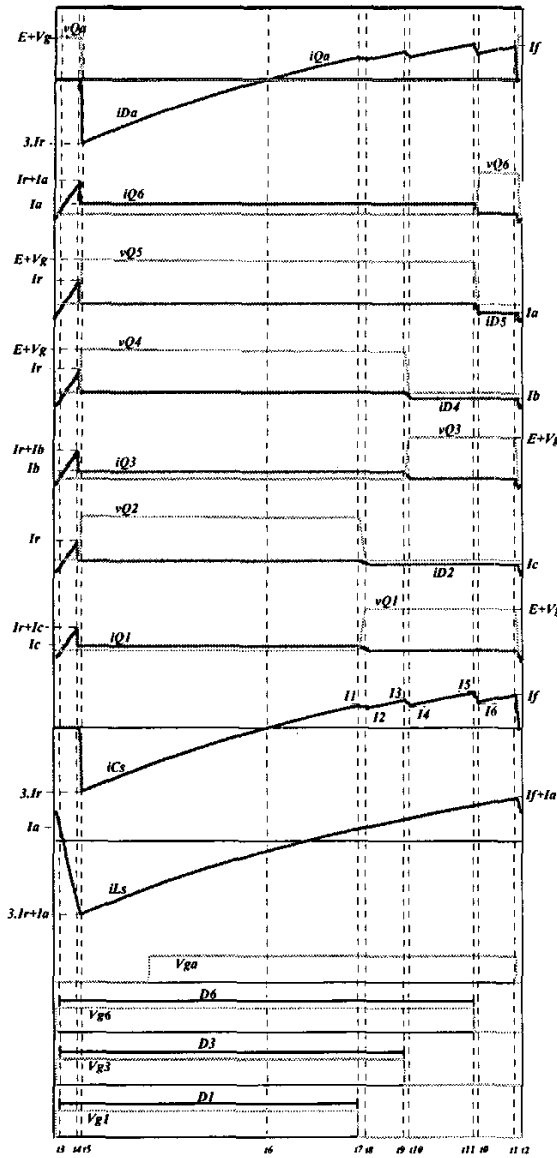


Fig. 3. Main waveforms

The duty cycle D can also be defined as:

$$D = ma \cdot \text{sen} \alpha \tag{12}$$

Where ma represents the modulation factor of amplitude.

From Eqs. 5 and 12 we obtain the expression of the V_{cs} voltage.

$$V_{cs}(t) = \frac{2 \cdot L_s}{T_s} \left[3 \cdot I_r + \frac{E \cdot ma}{Z_{ca}} \cdot \text{sen} \alpha - \frac{E \cdot ma^2}{2 \cdot Z_{ca}} \cdot \text{sen}^2 \alpha - \frac{E \cdot ma^2}{2 \cdot Z_{ca}} \cdot \text{sen} \alpha \cdot \text{sen} \left(\alpha - \frac{4 \cdot \pi}{3} \right) + \frac{E \cdot ma^2}{2 \cdot Z_{cb}} \cdot \text{sen} \alpha \cdot \text{sen} \left(\alpha - \frac{2 \cdot \pi}{3} \right) - \frac{E \cdot ma^2}{2 \cdot Z_{cb}} \cdot \text{sen}^2 \left(\alpha - \frac{2 \cdot \pi}{3} \right) \right] \tag{13}$$

Where I_r is the peak reverse recovery current of the anti-parallel diode, which can be given by:

$$I_r = \sqrt{\frac{4}{3} \cdot Q_{rr} \cdot \frac{E}{L_s}} \tag{14}$$

Q_{rr} – Reverse Recovery Charge

From the analysis of the current behavior in the capacitor C_s , the expression of the current I_f can be obtained:

$$I_f(t) = \frac{V_{cs}}{L_s} \cdot T_s - 2 \cdot I_a - 3 \cdot I_r \tag{15}$$

Combining Eq. 13 with Eq. 15 and making some simplifications we obtain the expression that represents the evolution of the current I_f .

$$I_f(t) = 2 \cdot I_r + \frac{E \cdot ma}{Z_{ca}} \cdot \text{sen} \alpha - \frac{E \cdot ma^2}{Z_{ca}} \cdot \text{sen}^2 \alpha - \frac{E \cdot ma^2}{Z_{ca}} \cdot \text{sen} \alpha \cdot \text{sen} \left(\alpha - \frac{4 \cdot \pi}{3} \right) + \frac{E \cdot ma^2}{Z_{cb}} \cdot \text{sen} \alpha \cdot \text{sen} \left(\alpha - \frac{2 \cdot \pi}{3} \right) - \frac{E \cdot ma^2}{Z_{cb}} \cdot \text{sen}^2 \left(\alpha - \frac{2 \cdot \pi}{3} \right) \tag{16}$$

To guarantee ZVS condition in all load range the minimum value of the current I_f obtained from Eq. 16 must be bigger than the value obtained from Eq. 2.

V. DESIGN EXAMPLE

A. INPUT DATA

- | | |
|---------------------------------------|---------------------|
| $E = 400V$ | Bus Voltage |
| $V_{out} = 127 V$ | RMS Output Voltage |
| $P_{out_{3\phi}} = 12 \text{ kVA}$ | Output Power |
| $f_s = 20KHz$ | Switching Frequency |
| $f = 60Hz$ | Output Frequency |
| $L_{ca} = L_{cb} = L_{cc} = 575\mu H$ | Load Inductance |
| $R_{ca} = R_{cb} = R_{cc} = 4\Omega$ | Load Resistance |
| $ma = 0,9$ | Modulation Factor |

B. CALCULATION OF THE AUXILIARY INDUCTOR.

The auxiliary inductor is responsible for the di/dt limit during the turn off of the main diodes. The di/dt is directly related

with the peak reverse recovery current I_r of the antiparallel diodes. A “snappy” di/dt produces a large amplitude voltage transient and contributes significantly to Electro-magnetic interference.

In the design procedure it is chosen a di/dt that is usually find in the diode data book. This is a simple way to obtain the diodes fundamental parameter for the design of the inverter. In such case the di/dt chosen for this example was 40A/us. Knowing that the current ramp rate is determined by the external circuit, thus:

$$L_s = \frac{E}{\frac{di}{dt}} = \frac{400V}{40 \frac{A}{\mu s}} = 10\mu H \tag{17}$$

C. LOAD IMPEDANCE.

The load impedance is obtained from Eq. 18

$$Z_{out} = \sqrt{4\Omega^2 + (2 \cdot \pi \cdot 60\text{Hz} \cdot 575\text{mH})^2} \cong 4\Omega \quad (18)$$

D. DIODE CHOOSE.

For the performance of the inverter it is important to choose a slow diode. So, we opt to use the diode SEMIKRON SKKD 81/12, which has the following characteristics:

- V_{rrm} = 1.200V Maximum Reverse Voltage
- I_{fav} = 80A Diode Average Current
- Q_{rr} = 120μC Reverse Recovery Charge

E. SWITCHING PERIOD

$$T_s = \frac{1}{f_s} = \frac{1}{20\text{KHz}} = 50\mu\text{s} \quad (19)$$

F. REVERSE RECOVERY CURRENT.

The reverse recovery current is given by the Eq. 20.

$$I_r = \sqrt{\frac{4}{3} \cdot 120\mu\text{C} \cdot \frac{400\text{V}}{10\mu\text{H}}} = 80\text{A} \quad (20)$$

G. CAPACITOR CLAMPING VOLTAGE BEHAVIOR

Using a Eq. 13 the curves described in Fig. 4 are obtained.

For ma=0,9, the maximum clamping voltage is 108V.

We can observe that the voltage increment across the switches is too low.

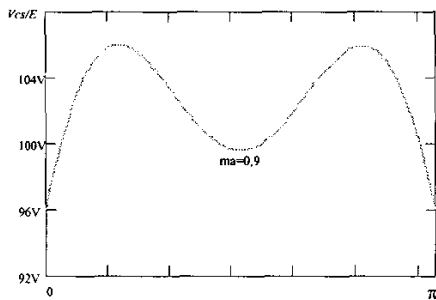


Fig 4. Capacitor Clamping Voltage Behavior

H. CURRENT If BEHAVIOR.

The current If behavior, obtained from Eq. 2 and Eq.16, can be seen in Fig. 5.

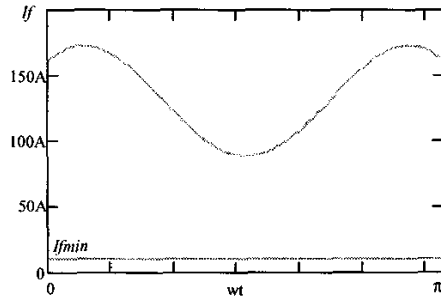


Fig. 5. Current If Behavior

It is observed that the current If has a minimum point that is located in π/2, and the intensity of the current diminishes with the increase of the load. To guarantee ZVS condition in all range load, the minimum value of the current If, obtained from Eq. 16, must be bigger than the value of the traced straight line from Eq. 2.

VI. EXPERIMENTAL RESULTS

An inverter prototype rated 12kVA operating with PWM commutation was built to evaluate the proposed circuit. The main specifications and components are given below:

A. PROTOTYPE SPECIFICATIONS

- P_{outφ} = 12 kVA (Output Power)
- E = 400V (Input Voltage)
- V_{out} = 127V (Rms Output Voltage)
- f = 60Hz (Output Frequency)
- f_s = 20 kHz (Switching Frequency)
- Switches (IGBT GA250TS60U)
- Diodes (SKKD81/12)
- Intrinsic Capacitance 1.5nF
- L_s (10uH each; Ferrite Core EE55/39; N=20 turns, 57 wires #22AWG)
- C_s (4 x 1000uF/350V; Electrolytic Capacitor)

B. EXPERIMENTAL WAVEFORMS

In the figures presented below we can observe the experimental waveforms obtained from the laboratory prototype. Figs. 6, 7 and 8 show the voltage and current in the switches. In Fig. 9 it can be observed the current in the commutation auxiliary inductor for a switching period. The voltage across the clamping capacitor Cs is shown in Fig. 10. We can note a very low voltage across Cs. The output voltage and current are presented in Fig. 11. The efficiency of the converter at full load was about 96.5%.

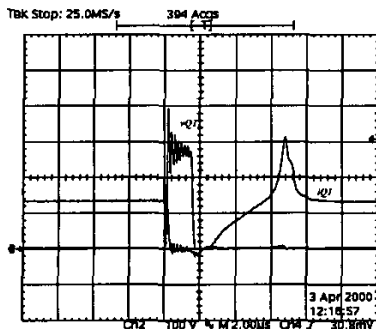


Fig 6. Voltage and current in Q1, D1 e C1
100V/div, 20A/div, 2us/div

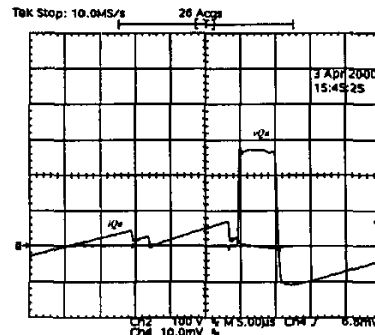


Fig 8. Voltage and current in Qa, Da e Ca
100V/div, 50A/div, 10us/div

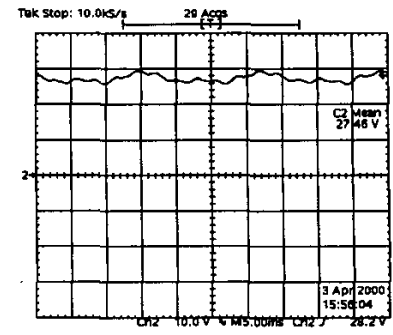


Fig 10. Voltage in Cs
10V/div, 5ms/div

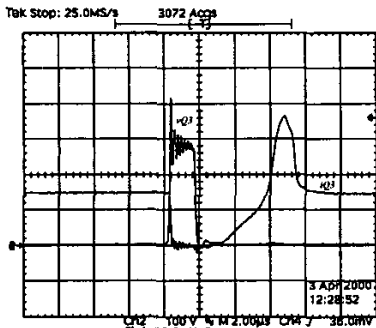


Fig 7. Voltage and current in Q3, D3 e C3
100V/div, 20A/div, 2us/div

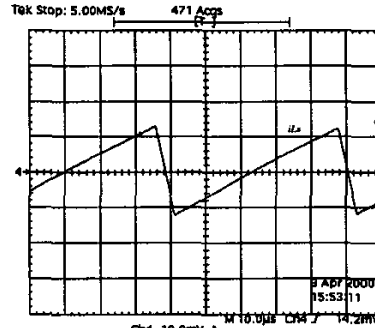


Fig 9. Current in Ls
50A/div, 10us/div

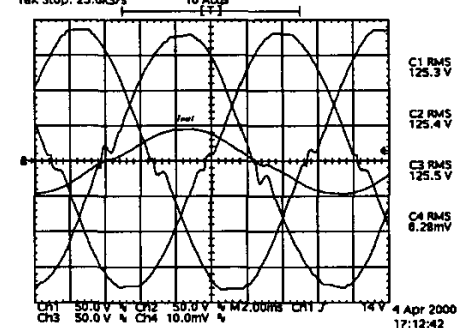


Fig 11. Output voltage and current
50V/div, 50A/div, 5ms/div

VII. CONCLUSIONS

A ZVS PWM Three-Phase Inverter with voltage clamping using a single auxiliary switch has been developed. The operation stages for steady-state condition, mathematical analysis, main waveforms and experimental results were presented. The experimental results show a low voltage in the clamping capacitor. Conduction and switching losses are reduced due to the implementation of the simple active snubber circuit, which provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability, and make it suitable for practical applications. The proposed circuit presents soft commutation for all load range, confirming the theoretical studies.

VIII. REFERENCES

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