

TRANSFORMERLESS DOUBLE-CONVERSION UPS USING A REGENERATIVE SNUBBER CIRCUIT

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Abstract – This paper proposes a transformerless double-conversion UPS, which uses a regenerative Undeland snubber to regenerate the energy from switching losses to the dc bus. The regenerative circuit uses a simple buck-boost QSC (Quasi-Square-Wave) ZVS (Zero Voltage Switching) converter. This auxiliary commutation circuit includes only one active switch and its operation is independent of the UPS operation mode. A detailed methodology is included to design the main components of the auxiliary commutation circuit. Experimental results based on a 1.3 kVA prototype are presented for distinct operation modes to verify the feasibility of the proposed UPS.

Keywords – Double-conversion UPS, soft-commutation, transformerless.

I. INTRODUCTION

Double-conversion UPSs (Uninterruptible Power Systems) are largely used to protect critical loads, because they present several advantages: (i) low-THD (Total Harmonic Distortion) output voltages can be synthesized with amplitude and frequency independent of the respective values of the input voltages, (ii) zero transfer time can be accomplished when utility grid fails, and (iii) it is possible to obtain a high input power factor [1], [2]. Among several configurations of double-conversion UPSs, transformerless UPSs have been widely employed at power ratings below 40 kVA [3]. As these UPSs do not use conventional bulky and heavy transformers, they are a compact and cost-effective solution for several environments, such as office rooms [3]–[7].

Although double-conversion UPSs present several advantages, they usually have a smaller efficiency by comparing them with passive-standby UPSs, because there are two power conversion stages. Therefore, it is necessary to analyze alternatives to reduce conduction and switching losses of these UPSs. An option is to use auxiliary commutation circuits, such as passive snubbers [8]–[13] and soft-commutation cells [14]–[22], which have been employed in several converters to reduce the switching losses and the electromagnetic interference (EMI). However, these auxiliary circuits increase the number of components, and therefore the cost and the complexity of the overall system. This complexity is enlarged for multi-stage power conversion system, such as double-conversion UPSs, so that it is imperious to introduce techniques to reduce the number of additional components and, mainly, active switches [23], [24].

A well-known passive snubber was proposed by Undeland [8]. It transfers the energy from switching losses to a

clamping capacitor, but it is not capable to regenerate this energy that should be dissipated on a resistor. As an attempt to minimize the switching losses, some works introduced some modifications in the Undeland snubber to regenerate the switching losses [9]–[13].

Aiming to improve the efficiency, a buck-boost QSC (Quasi-Square-Wave) ZVS (Zero Voltage Switching) converter was added to a three-phase PWM inverter with a modified Undeland snubber to transfer the energy stored in the clamping capacitor to the dc bus [25], [26]. This auxiliary commutation circuit can regenerate the energy from n -leg converters with only one inductor and one active switch, which operates under ZVS, and it operates independently of main switches.

Therefore, this paper proposes a transformerless double-conversion UPS, which uses a modified Undeland snubber and a simple buck-boost converter to regenerate the energy from switching losses to the dc bus. A detailed methodology is included to design the main components of the auxiliary commutation circuit. Experimental results based on a 1.3 kVA prototype are presented for distinct operation modes to verify the feasibility of the proposed UPS.

II. UPS DESCRIPTION

Figure 1 shows a simplified diagram of the transformerless double-conversion UPS under study, which is composed of a half-bridge rectifier, a step-down/step-up bidirectional converter for battery bank charge/discharge and a half-bridge inverter [4]. The rectifier has a filter inductor (L_i), two switches (S_1 and S_2) and two diodes (D_1 and D_2). The bidirectional converter is composed of two switches (S_3 and S_4), two diodes (D_3 and D_4) and one inductor (L_b) connected to the battery bank. The inverter has two switches (S_5 and S_6), two diodes (D_5 and D_6) and an output LC filter (L_o and C_o) to minimize the high-frequency harmonics of the ac output voltage waveform.

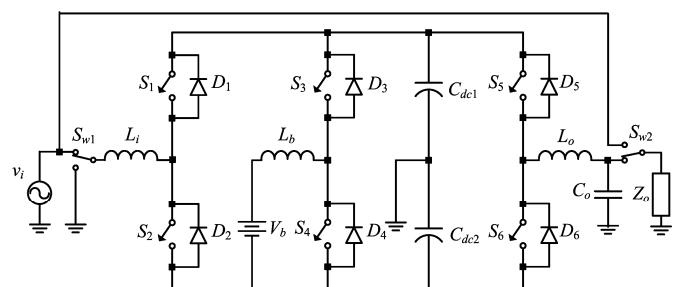


Fig. 1. Transformerless double-conversion UPS under study.

This UPS presents some advantages, such as:

- reduced number of components;
- reduced battery bank voltage;
- semiconductors can be implemented in a single power module;
- common neutral connection between input and output. Thus, it is not necessary to use an isolation transformer to implement the bypass switch.

On the other hand, for the same ac output voltage level, the voltage across the semiconductors is twice that of the full-bridge-based topologies.

This UPS has two operation modes, according to the utility grid state:

- **Normal mode:** it occurs when the utility voltage is within adequate limits. The half-bridge rectifier operates as a PFC (Power Factor Correction) converter and it regulates the voltages across the dc-bus capacitors. The bidirectional converter operates as a buck converter to charge the battery bank. The inverter synthesizes a sinusoidal voltage with reduced harmonic content to the ac loads.
- **Backup mode:** it occurs when the ac input supply is out of UPS preset tolerances. At this mode, the bidirectional converter acts as a dc-dc boost converter to maintain the total dc-bus voltage v_{dc} regulated. The inductor L_i is connected to the ground by the switch S_{w1} and the half-bridge rectifier maintains the voltages across the dc-bus capacitors balanced and equal to $v_{dc}/2$ [27]. The half-bridge inverter maintains the ac output voltage during a specified battery discharge time.

By occurring an UPS fault, the states of S_{w1} and S_{w2} are modified so that the utility voltage source is connected directly to the load.

III. UPS WITH AUXILIARY COMMUTATION CIRCUITS

Figure 2 presents an alternative to reduce the electromagnetic interference and the switching losses of the double-conversion UPS shown in Figure 1. Passive snubbers

are used to transfer the energy from switching losses to a clamping capacitor. This energy could be dissipated on a resistor, but the efficiency of the overall system would be penalized. On the other hand, an interesting option to increase the efficiency is to include a single regenerative circuit to transfer the energy stored in the clamping capacitor, for instance, to the dc bus.

Based on this concept, a modified Undeland snubber was included in the UPS presented in Figure 1 to transfer the switching losses and, therefore, to alleviate the main switches. This snubber has some important advantages, such as the utilization of only one inductor, which is common to all UPS legs, and the clamping capacitor is connected above the dc bus. By comparing it with the original Undeland snubber [8], the number of magnetic elements is reduced as well as the voltage across the clamping capacitor.

The transformerless double-conversion UPS with the modified Undeland snubber can be seen in Figure 3. As mentioned before, this snubber transfers the energy from switching losses to a clamping capacitor C_s and dissipates it on a resistor R_d .

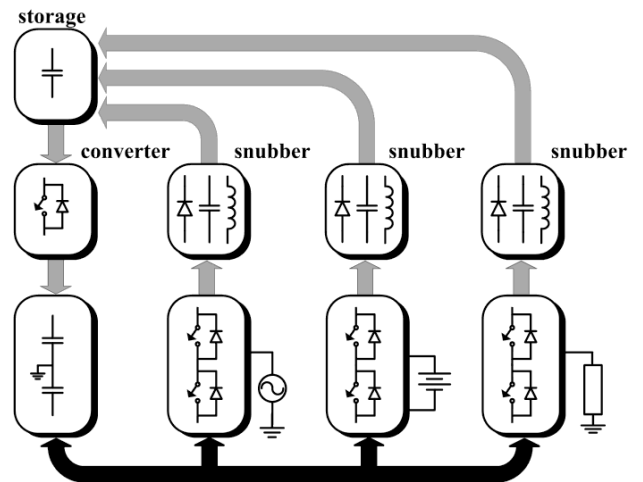


Fig. 2. Simplified block diagram of the proposed UPS.

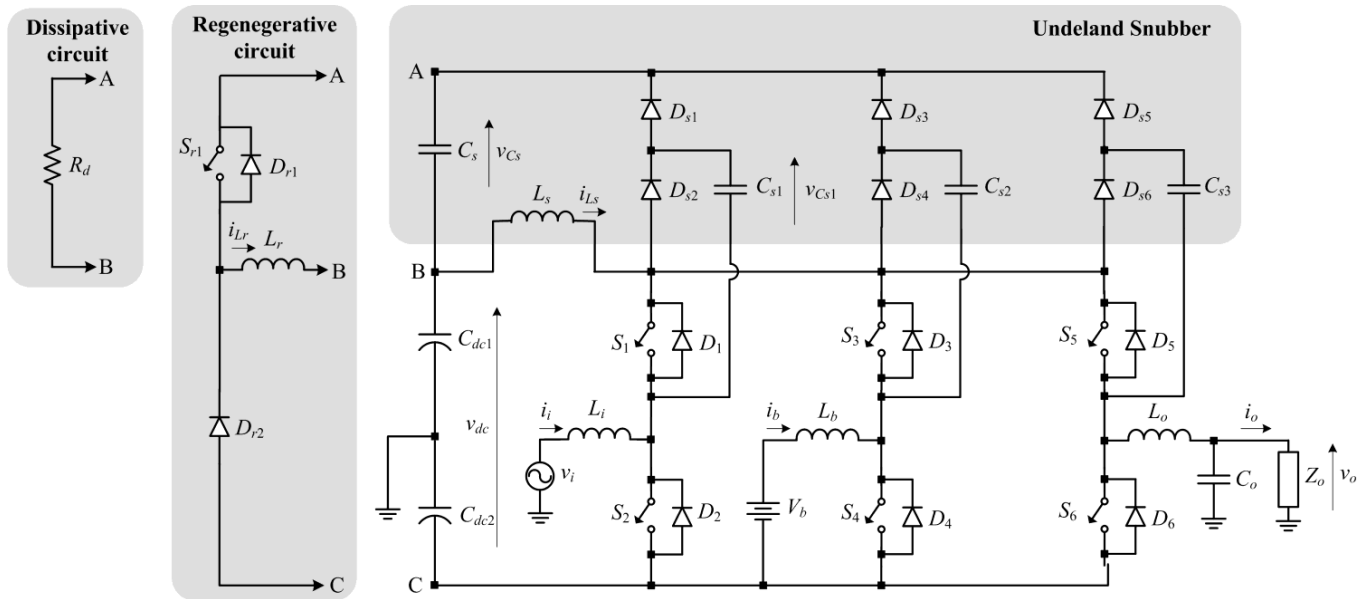


Fig. 3. Proposed UPS circuit.

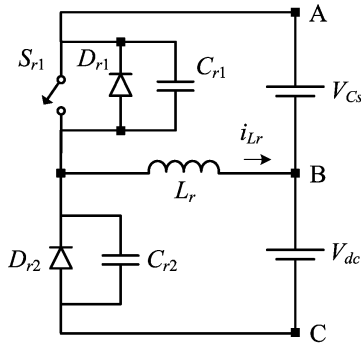


Fig. 4. Equivalent circuit of the buck-boost QSC-ZVS converter.

Alternatively, it is possible to include a converter to regenerate the energy stored in C_s . Therefore, a buck-boost QSC-ZVS converter [26] is included in the UPS to regenerate this energy, removing the resistor R_d . The connection of this regenerative circuit to the double-conversion UPS is shown in Figure 3. It is important to highlight again that the resistor R_d is not necessary if the regenerative buck-boost converter is included.

The buck-boost converter can be designed to operate under soft-commutation, increasing the efficiency, reducing the electromagnetic interference and, therefore, improving the overall performance of the double-conversion UPS. An equivalent circuit to analyze the operation of the regenerative buck-boost converter is presented in Figure 4. At this circuit, the voltage across the capacitor C_s is considered a dc voltage source and the voltages across the dc bus capacitors are replaced by a single dc voltage source. The intrinsic capacitances of the semiconductors were also considered.

Based on this equivalent circuit, the operation of the regenerative circuit can be concisely described as follows [25]: initially, the switch S_{r1} is turned on and the energy is transferred from dc source V_{Cs} to inductor L_r . After, the switch S_{r1} is turned off and the current circulates through C_{r1} and C_{r2} , charging C_{r1} and discharging C_{r2} . Then, the voltage across C_{r2} reaches zero, the diode D_{r2} conducts and the energy stored in the inductor L_r is transferred to dc bus. The inductor current (i_{Lr}) reaches zero and becomes negative, due to the reverse recovery energy from diode D_{r2} . At the instant that the reverse recovery energy is fully transferred to the inductor L_r , the diode D_{r2} turns off and the inductor current circulates again through the capacitors C_{r1} and C_{r2} , but now discharging C_{r1} and charging C_{r2} . The voltage across C_{r1} reaches zero, the diode D_{r1} conducts and there is power transfer to the dc source V_{Cs} . During this time interval, the switch S_{r1} may be turned on to guarantee ZVS.

IV. DESIGN CONSIDERATIONS

This section presents some guidelines to design the auxiliary commutation circuits that compose the proposed UPS.

A. Design of the Modified Undeland Snubber

The design methodology for the modified Undeland snubber uses the following specifications:

- V_{dc} – nominal dc bus voltage;
- $di_s/dt|_{\max}$ – maximum rate of current change of the main switches;

$dv_s/dt|_{\max}$ – maximum rate of voltage change across the main switches;

I_p – maximum peak current of the converter legs;

ΔV_{Cs} – clamping capacitor voltage ripple;

f_s – switching commutation of the main switches.

It is possible to design the main components of the modified Undeland snubber by using these specifications, as follows:

Step 1 – Choose the clamping voltage of the modified Undeland snubber in the nominal operating point. The following range can be considered to avoid a significant voltage stress across the main switches:

$$0.05V_{dc} \leq V_{Cs} \leq 0.1V_{dc} \quad (1)$$

Step 2 – Determine the inductance L_s that limits the rate of current change of the main switches:

$$L_s = \frac{V_{dc}}{\left. \frac{di_s}{dt} \right|_{\max}} \quad (2)$$

Step 3 – Compute the capacitances C_{s1} , C_{s2} and C_{s3} , which limit the rate of voltage change across the main switches:

$$C_{s1} = C_{s2} = C_{s3} = \max(f_1, f_2) \quad (3)$$

where:

$$f_1 = \frac{1}{2 \left(\left. \frac{dv_s}{dt} \right|_{\max} \right)^2} \left[\frac{V_{dc}^2}{L_s} + \sqrt{\frac{V_{dc}^4}{L_s^2} + \left(\left. \frac{dv_s}{dt} \right|_{\max} \right)^2 I_p^2} \right] \quad (4)$$

$$f_2 = \frac{V_{dc}}{\sqrt{L_s} \left. \frac{dv_s}{dt} \right|_{\max}} \quad (5)$$

Step 4 – Determine the maximum power P_{Cs} transferred from the switching losses to the clamping capacitor.

The analytical computation of P_{Cs} is extremely complex due to the large number of variables that affect the power transferred by the snubber. Therefore, the easiest and efficient way to obtain a reliable estimate of this power level is to simulate the overall circuit, considering that:

- UPS processes the maximum power level in normal mode, that is, nominal load is connected to the output, and the bidirectional converter operates as a step-down converter to charge the battery bank;
- capacitor C_s can be replaced by a dc voltage source V_{Cs} ;
- models of the components used in simulation must represent adequately the real behavior of the semiconductors employed in the converter (SPICE model);
- simulation describes at least one operation cycle of the converter.

Step 5 – Determine the minimum value of the clamping capacitor C_s to limit its voltage ripple at the specified value.

The analytical computation of C_s depends on i_{Cs} , which cannot be easily solved analytically. Again, the easiest and efficient way to determine a reliable estimate of this current

is to simulate the overall circuit, considering the same conditions described at step 4 and:

- replace the dc voltage source V_{Cs} by a capacitor C_s , whose capacitance is determined by simulation. An initial estimate for this capacitance to start the iterations can be given by:

$$C_s = \frac{P_{Cs}}{\Delta V_{Cs} f_s V_{Cs}}; \quad (6)$$

- include the equivalent series resistance of the capacitor in the model;
- connect a resistor R_d in parallel to the capacitor C_s to dissipate the energy stored in the capacitor. The resistance can be obtained by:

$$R_d = \frac{V_{Cs}^2}{P_{Cs}}. \quad (7)$$

It is important to highlight that the capacitance to be used in practice can be greater than the value obtained from simulations. A larger capacitance does not affect the snubber performance, because it results in smaller clamping capacitor voltage ripple. In practical applications, the capacitor design is closely related to thermal restrictions so that it can be necessary to connect several capacitors to satisfy this condition.

B. Design of the Buck-Boost QSC-ZVS Regenerative Converter

The design methodology for the buck-boost QSC-ZVS converter, which is utilized to regenerate the energy stored in the clamping capacitor, is based on [25]. In addition to the specifications to design the modified Undeland snubber, the clamping capacitor voltage V_{Cs} and the maximum power P_{Cs} transferred from the switching losses to the clamping capacitor must be specified to design the regenerative circuit. Both variables are obtained from the snubber design.

One can design the main components of the regenerative circuit by using these specifications, as follows:

Step 1 – Choose the diode D_{r2} , whose maximum voltage is $V_{dc} + V_{Cs}$ and the average current is:

$$\overline{I_{Dr2}} = \frac{V_{dc}}{P_{Cs}}. \quad (8)$$

The reverse recovery time (t_{rr}), the rate of current change used in the reverse recovery test (di_d/dt) and the intrinsic junction capacitance (C_{r2}) are obtained from the datasheet of the selected diode. These values are used at the following steps.

Step 2 – Determine the reverse recovery charge (Q_{rr}) of the diode D_{r2} :

$$Q_{rr} = \frac{t_{rr}^2}{3} \left(\frac{di_d}{dt} \right). \quad (9)$$

Step 3 – Determine the nominal duty ratio of the buck-boost converter from the following expression:

$$D_{nom} = \frac{V_{dc}}{V_{dc} + V_{Cs}}. \quad (10)$$

Step 4 – Compute the inductance L_r .

$$L_r = \left(a - \sqrt{a^2 - b} \right) V_{dc} (1 - D_{nom})^2 \quad (11)$$

where:

$$a = \frac{1}{2f_s I_{Dr2}} + \frac{4Q_{rr}}{6I_{Dr2}^2} \quad (12)$$

$$b = \frac{1}{4f_s^2 I_{Dr2}^2}. \quad (13)$$

Step 5 – Choose the switch S_{r1} , whose maximum voltage is $V_{dc} + V_{Cs}$ and the average current is:

$$\overline{I_{Sr1}} = \frac{V_{Cs} f_s t_{sw}^2}{L_r} \quad (14)$$

where:

$$t_{sw} = \frac{D_{nom}}{f_s} - \frac{I_R L_r}{V_{Cs}} \quad (15)$$

$$I_R = \sqrt{\frac{4V_{dc} Q_{rr}}{3L_r}}. \quad (16)$$

The output capacitance of the selected switch (C_{r1}) is obtained from the datasheet. This value is used at the following step.

Step 6 – Verify the soft-commutation condition, which is given by:

$$Q_{rr} > \frac{3(C_{r1} + C_{r2})(V_{dc} + V_{Cs})^2}{4V_{dc}}. \quad (17)$$

If this condition is not satisfied, the regenerative circuit operates in dissipative mode. In this case, to obtain a ZVS converter it is necessary to return to Step 1 and to repeat the design procedure with another diode D_{r2} , which should have a larger reverse recovery time.

Step 7 – Determine the duty ratio of S_{r1} , which should satisfy the following condition:

$$D_{min} < D < D_{nom} \quad (18)$$

where:

$$D_{min} = D_{nom} - \frac{f_s}{V_{Cs}} \sqrt{\frac{4}{3} L_r V_{dc} Q_{rr}}. \quad (19)$$

This duty ratio interval corresponds to the conduction period of D_{r1} , in which the switch S_{r1} must be turned off to guarantee ZVS.

V. EXPERIMENTAL RESULTS

A prototype of the transformerless double-conversion UPS presented in Figure 3 was built in our lab. The UPS specifications are presented in Table I and the main components of this prototype are given in Table II. A closed-

TABLE I
UPS specifications

$v_i = 127 \text{ V}_{\text{rms}}$	Input voltage
$v_o = 127 \text{ V}_{\text{rms}}$	Output voltage
$v_{dc} = 400 \text{ V}$	DC bus voltage
$V_{bat} = 96 \text{ V}$	Battery bank voltage
$P_o = 1.3 \text{ kVA}$	Nominal output power
$f_s = 50 \text{ kHz}$	Switching frequency

TABLE II
Main components

$S_1 - S_6, S_{r1}$	IGBTs IRG4PF50WD
$D_1 - D_6, D_{r1}$	Ultrafast soft recovery diodes of IGBTs IRG4PF50WD
$D_{S1} - D_{S6}, D_{r2}$	Diodes: HFA16TB120
$C_{s1} - C_{s3}$	Polypropylene capacitor: 4.7 nF
C_{dc1}, C_{dc2}	Electrolytic capacitor: 680 μF
C_s	Electrolytic capacitor: 2 x 470 μF
C_o	Polypropylene capacitor: 5 x 1 μF
L_i, L_b, L_o	Toroidal iron powder inductor: 560 μH
L_r	Ferrite inductor: 40 μH
L_s	Ferrite inductor: 0.5 μH

loop UPS was implemented to obtain a high input power factor at the normal operation mode and to synthesize an output voltage with reduced THD.

Figure 5 shows the input voltage and current waveforms in the normal operation mode by connecting a 500 W resistive load to the UPS output. The input current THD is 3.4 % and the input power factor is 0.99, illustrating that the auxiliary commutation circuits do not affect the performance of the half-bridge rectifier. There is a small phase displacement between the input voltage and current waveforms because an LC filter was included at the UPS input to reduce high-frequency harmonics. Figure 6 presents the output voltage and current waveforms in the normal operation mode with the same resistive load. The output voltage THD is 3.2 %, demonstrating that the performance of the output inverter is independent from the auxiliary commutation circuits.

On the other hand, when the ac input supply is out of UPS preset tolerances, the step-down/step-up bidirectional converter operates as a boost converter to maintain the voltages across the dc bus capacitors regulated. Figure 7 shows the voltage and current waveforms at the battery bank.

The performance of the double-conversion UPS with the regenerative Undeland snubber circuit was analyzed in this paper. The efficiency of the proposed UPS was compared to the efficiency of a similar UPS with dissipative Undeland snubber. Figures 8 and 9 present the efficiency curves of both UPSs in normal mode and in backup mode, respectively. As can be seen in both figures, the results show that the regenerative snubber improves the efficiency around 6% over a wide output power range. Moreover, the efficiency in backup mode is lower than the efficiency obtained in normal mode. This occurs because the battery bank current is higher than the input rms current for the same output power.

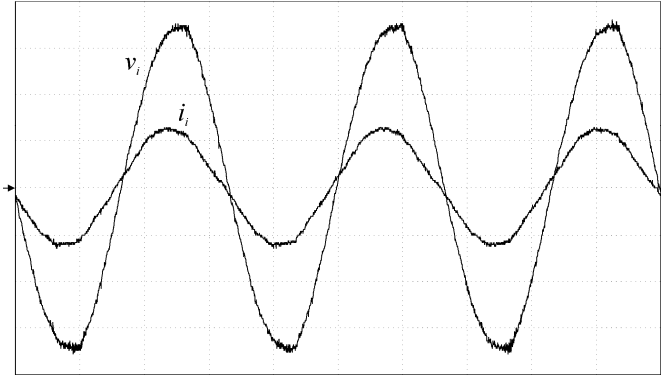


Fig. 5. UPS in normal mode: input voltage and current waveforms (50 V/div, 5 A/div, 5 ms/div).

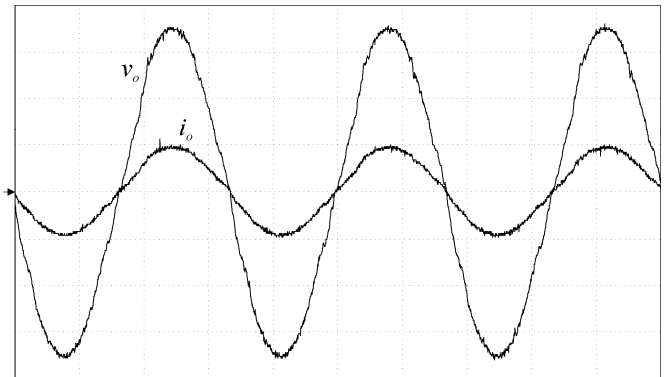


Fig. 6. UPS in normal mode: output voltage and current waveforms (50 V/div, 5 A/div, 5 ms/div).

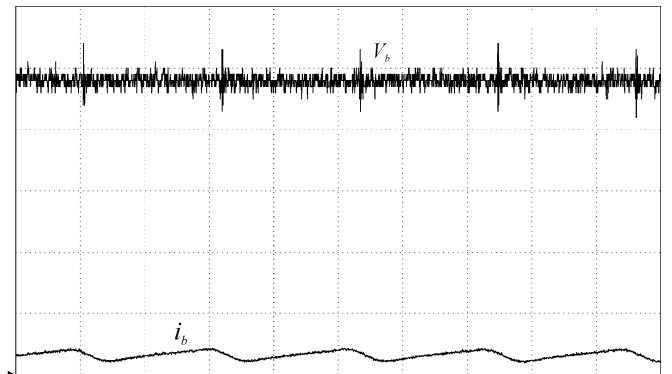


Fig. 7. UPS in backup mode: voltage and current in the battery bank (20 V/div, 10 A/div, 10 μs /div).

One can also observe that it was not possible to obtain the nominal output power in backup mode. This occurs because the output power is derated in backup mode to comply with ratings of the semiconductors. However, it is worth mentioning that the regenerative Undeland snubber could operate with distinct semiconductors.

VI. CONCLUSIONS

This paper presented a new transformerless double-conversion UPS, which uses a modified Undeland snubber to transfer the switching losses energy to a clamping capacitor and a simple buck-boost converter regenerates this energy to the dc bus. This topology has a higher efficiency by comparing it with dissipative snubbers. Moreover, the proposed topology also has some advantages by comparing it

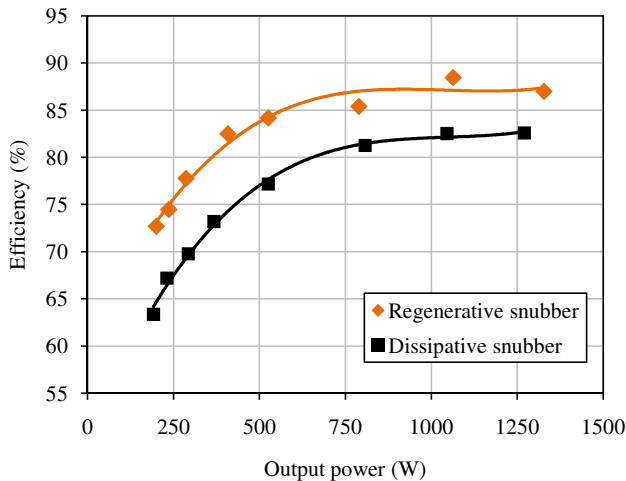


Fig. 8. Efficiency curve of the UPS in normal mode.

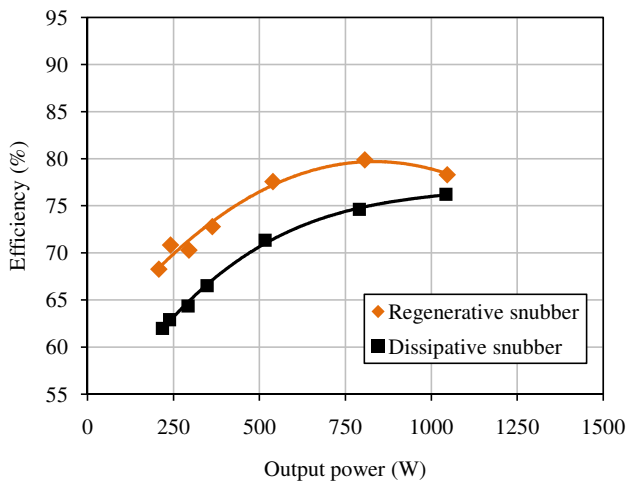


Fig. 9. Efficiency curve of the UPS in backup mode.

with soft-commutation cells presented in the literature, which are:

- robust structure with only one controlled switch;
- auxiliary switch operates with independent pulse-width modulation and constant duty cycle;
- low clamping voltage across the capacitor;
- simple design procedure with few restrictions.

The experimental results included in the paper show that the regenerative snubber improves the efficiency around 6% over a wide output power range. With these features, the authors believe that the proposed regenerative snubber circuit can be very useful for several UPS applications.

REFERENCES

[1] *IEEE Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications*, IEEE Standard 446-1995 (Orange Book), 1995.

[2] *Uninterruptible Power Systems (UPS) – Part 3: Method of Specifying the Performance and Test Requirements*, IEC 62040-3, 1999.

[3] R. Koffler, “Transformer or Transformerless UPS?”, *IEE*

Power Engineer, v. 17, n. 3, pp. 34-36, June/July 2003.

[4] K. Hirachi, A. Kajiyama, T. Mii, M. Nakaoka, “Cost-Effective Bidirectional Chopper-Based Battery Link UPS with Common Input-Output Bus Line and Its Control Scheme”, in *Proc. 22nd IECON*, pp. 1681-1686, 1996.

[5] R. C. Fuentes, H. Pinheiro, “Non-Isolated Single Phase UPS Based on Step-Up Converters”, in *Proc. CIEP’2000*, pp. 353-358, 2000.

[6] S. B. Bekiarov, A. Nasiri, A. Emadi, “A New Reduced Parts On-Line Single-Phase UPS System”, in *Proc. 29th IECON*, pp. 688-693, 2003.

[7] J.-K. Park, J.-M. Kwon, E.-H. Kim, B.-H. Kwon, “High-Performance Transformerless Online UPS”, *IEEE Trans. Ind. Electr.*, vol. 55, n. 8, pp. 2943-2953, Aug. 2008.

[8] T. M. Undeland, “Switching Stress Reduction in Power Transistor Converters”, in *Proc. IEEE IAS Annual Meeting*, pp. 383-391, 1976.

[9] J. Holtz, S. F. Salama, K. Werner, “A Nondissipative Snubber Circuit for High-Power GTO-Inverters”, in *Proc. IEEE IAS Annual Meeting*, pp. 613-618, 1987.

[10] D. Tardiff, T. H. Barton, “A Summary of Resonant Snubber Circuits for Transistors and GTOs”, in *Proc. IEEE IAS Annual Meeting*, pp. 1176-1180, 1989.

[11] J. A. Taufiq, “Advanced Inverter Drivers For Traction”, in *5th European Conf. on Power Electr. and Applicat.*, v. 5, pp. 224-228, 1993.

[12] X. He, Y. Deng, B. W. Williams, S. J. Finney, Z. Qian, “A Simple Energy Recovery Circuit for High-Power Inverters With Complete Turn-On and Turn-Off Snubbers”, *IEEE Trans. Ind. Electr.*, v. 51, n. 1, pp. 81-88, Feb. 2004.

[13] X. He, A. Chen, H. Wu, Y. Deng, R. Zhao, “Simple Passive Lossless Snubber for High-Power Multilevel Inverters”, *IEEE Trans. Ind. Electr.*, v. 53, n. 3, pp. 727-735, June 2006.

[14] A. Cheriti, “A Rugged Soft Commutated PWM Inverter for AC Drivers”, in *Proc. IEEE PESC*, pp. 656-662, 1990.

[15] H. Foch, M. Cheron, M. Metz, T. Meynard, “Commutation Mechanisms and Soft Commutation in Static Converters”, in *Proc. COBEP’91*, pp. 338-346, 1991.

[16] W. McMurray, “Resonant Snubbers with Auxiliary Switches”, in *Proc. IEEE IAS Annual Meeting*, pp. 829-834, 1990.

[17] J. A. Bassett, “New Zero Voltage Switching, High Frequency Boost Converter Topology for Power Factor Correction”, in *Proc. INTELEC’95*, pp. 813-820, 1995.

[18] A. Pietkiewicz, D. Tollik, “New High Power Single-Phase Power Factor Corrector with Soft-Switching”, in *Proc. INTELEC’96*, pp. 114-119, 1996.

[19] C. M. O. Stein, H. A. Gründling, H. Pinheiro, J. R. Pinheiro, H. L. Hey, “Zero-Current and Zero-Voltage Soft-Transition Commutation Cell for PWM Inverters”, *IEEE Trans. Power Electr.*, v. 19, n. 2, pp. 396-403, March 2004.

- [20] Y. Li, F. C. Lee, "Design methodologies for high-power three-phase zero-current-transition inverters", in *Proc. IEEE-PESC*, pp.1217–1223, 2001.
- [21] Y. P. Li, F. C. Lee, D. Boroyevich, "A Simplified Three-Phase Zero-Current-Transition Inverter With Three Auxiliary Switches", *IEEE Trans. Power Electr.*, v. 18, n. 3, pp. 802-813, May 2003.
- [22] M. Mezaroba, D. C. Martins, I. Barbi, "A ZVS PWM Inverter With Active Voltage Clamping Using the Reverse Recovery Energy of the Diodes", *IEEE Trans. Circuits and Systems I: Regular Papers*, v. 52, n. 10, pp. 2219 – 2226, Oct. 2005.
- [23] J. L. Russi, M. L. S. Martins, L. Schuch, J. R. Pinheiro, H. L. Hey, "Synthesis methodology for multipole ZVT converters", *IEEE Trans. Ind. Electr.*, vol. 54, n. 3, pp. 1783-1795, June 2007.
- [24] L. Schuch, C. Rech, J. R. Pinheiro, "Integrated auxiliary commutation circuits: a generalised approach", *IET Power Electr.*, v. 2, n. 1, pp. 42-51, Jan. 2009.
- [25] M. Mezaroba, J. D. Sperb, "Conversor Auxiliar com Comutação ZVS Aplicado ao Snubber de Undeland Regenerativo", *Revista Eletrônica de Potência*, v. 13, n. 2, pp. 61-68, May 2008.
- [26] V. Vorperian, "Quasi-Square-Wave Converters: Topologies and Analysis", *IEEE Trans. Power Electr.*, v. 3, n. 2, pp 183-191, April 1988.
- [27] R. W. Johnson Jr., "Power Conversion Apparatus and Methods Using Balancer Circuits," U.S. Patent 6 819 576 B2, Nov. 16, 2004.