FULL BRIDGE – FLYBACK ISOLATED CURRENT RECTIFIER WITH POWER FACTOR CORRECTION

Janderson Duarte, Marcello Mezaroba, Leandro Michels, Cassiano Rech
Electrical Power Processing Research Group - nPEE – Electrical Engneering Department
Santa Catarina State University UDESC - CCT
Campus Universitário Prof. Avelino Marcante s/n – Joinville/SC - Brazil
PO-BOX 89223-100 – Phone (47) 4009-7200
E-mails: janderson_duarte@yahoo.com.br, mezaroba@joinville.udesc.br, michels@ieee.org, cassiano@ieee.org

***Abstract* – This paper presents a single-stage isolated current rectifier with power factor correction, based on full bridge and flyback topologies. The proposed converter can operate as a step-down or a step-up converter, according to the input and output voltage levels. This paper presents the theoretical analysis of the converter as well as experimental results based on a 3.5 kW prototype.**

***Keywords* – Current fed rectifier, full bridge – flyback, power factor correction.**

I. INTRODUCTION

Nonlinear loads introduce current harmonics in the utility grid. These current harmonics are not desirable, because they distort the utility voltage, increase the reactive energy and, consequently, the current levels in the utility grid. Therefore, there is an increasing demand for electric equipments with power factor correction.

On the other hand, electric isolation also is an important concern for power sources applications. It is common to use galvanic isolation between the utility grid and the converter outputs to protect the users.

The usual solution to achieve high power factor and galvanic isolation is to use a two-stage converter composed of a boost PFC pre-regulator converter and another dc-dc isolated converter. This configuration is well known and there are several topologies based on this solution proposed in the literature [1]-[5].

However, it is possible to reduce size and cost by using single-stage power sources with power factor correction and galvanic isolation. As an example, an isolated Flyback current fed Push-Pull converter was proposed for power factor correction [6], [7]. This isolated converter has high power factor and it can operate as a step-up or step-down converter. However, due to the Push-Pull features, this converter has some disadvantages that limit its application only for low and medium power levels: transformer saturation and voltage stress across the switches. Another single-stage configuration is the Full-Bridge Boost converter [4], [8], [9]. This converter has high-frequency galvanic isolation and it also presents high power factor. Nevertheless, the switches are submitted to high voltage levels when they are turned off by protection circuits. In addition, this topology only operates as a step-up converter.

Therefore, as an attempt to overcome these disadvantages, this paper proposes a Full-Bridge Flyback isolated current rectifier with power factor correction. This converter has high power factor, high-frequency galvanic isolation and it can operate as a step-up or step-down converter.

The main differences between the proposed topology and the Flyback Push-Pull converter are:

- It can operate with high power levels;
- The transformer does not saturate;
- Low voltage stress in the witches.

The differences between the proposed converter and Full-Bridge Boost topology are:

- The switches are not submitted to high voltage levels when all the switches are turned off;
- It can also operate as a step-down converter.

II. PROPOSED TOPOLOGY AND OPERATION PRINCIPLES

Fig. 1 shows a simplified circuit of the proposed converter. The circuit is composed of a full-bridge diode rectifier (D_7, D_8, D_9 and D_{10}), a flyback coupled inductor (L_C), four main switches (S_1, S_2, S_3, and S_4), a full-bridge transformer (T_1), two flyback diodes (D_5 and D_6), four full-bridge diodes (D_1, D_2, D_3 and D_4) and an output filter capacitor (C_o).

The main features of the proposed converter are:

- single-stage converter;
- high power factor;
- galvanic isolation;
- constant switching frequency.
- step-down or step-up operation;
- it can operate with high power levels;
- it does not need an auxiliary pre-loading circuit to reduce the startup current (Inrush).

This converter can operate in two different modes, according to the input and output voltage levels, as it can be observed in Fig. 2. When the rectified input voltage is less than the output voltage referred to the transformer primary (V_o') the converter operates in Boost mode. On the other hand, the converter operates in Buck mode when the input voltage becomes higher than V_o'.

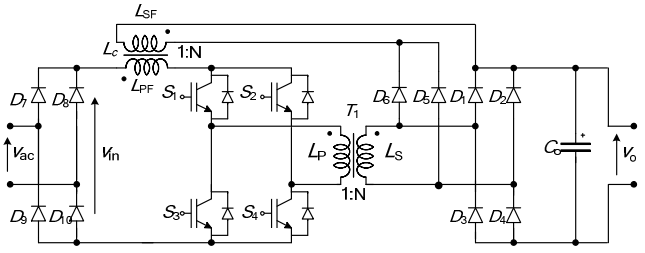

Fig. 1 Proposed converter.

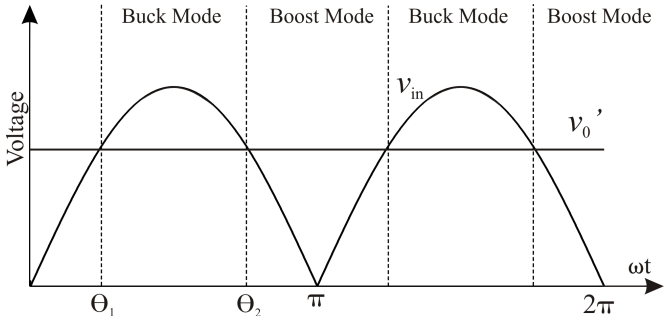

Fig. 2 Operation modes of the proposed converter.

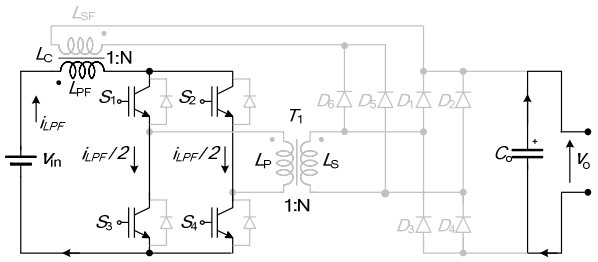

Fig. 3 First and third stages in Boost mode.

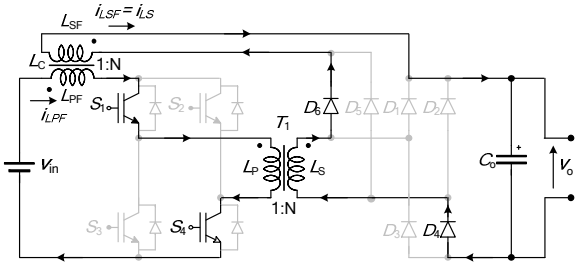

Fig. 4 Second stage in Boost mode.

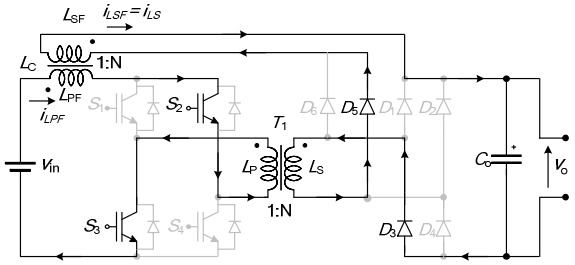

Fig. 5 Fourth stage in Boost mode.

Considering that the switching frequency is much higher than the fundamental frequency, the input voltage is assumed to be constant and the proposed converter can be analyzed as a DC-DC converter. Moreover, it is considered that the converter operates in continuous conduction mode (CCM). Thus, for each operation mode, the converter has four stages in a switching period. The transformer and coupled inductor turns ratios are considered unitary.

A. Boost mode

In this mode, the main switches operate with duty cycle between 0.5 and 1.0. The operation stages are presented as follows.

First Stage ($0 \le t \le t_c$-$T_S/2$): During this stage all switches are on and the input voltage is applied to the primary inductor. The current iL_{PF} increases linearly and L_C stores energy. There is no energy transfer from input source to the load, and only the output capacitor supplies energy to the load. The first operation stage is presented in Fig. 3.

Second Stage (t_c-$T_S/2 \le t \le T_S/2$): In this stage the switches S_2 and S_3 are turned off and the switches S_1 and S_4 are still on. The voltage across the primary inductor is $(V_{in} - NV_o)/2$ and the primary inductor current decreases linearly. As the transformer and coupled inductor turns ratios are unitary, the currents flowing through the primary and the secondary of the coupled inductor are equal, that is, $iL_{PF} = iL_{SF}$. During this stage there is energy transfer from input source to the output through D_4 and D_6. The second stage is shown in Fig. 4.

Third Stage ($T_S/2 \le t \le t_c$): During this stage all switches are on again and, therefore, this stage is identical to the first stage. Then, the third stage can be illustrated by Fig. 3.

Fourth Stage ($t_c \le t \le T_S$): In this stage the switches S_1 and S_4 are turned off and the switches S_2 and S_3 are still on. The voltage across the primary inductor is $(V_{in} - NV_o)/2$ and the primary inductor current decreases linearly.

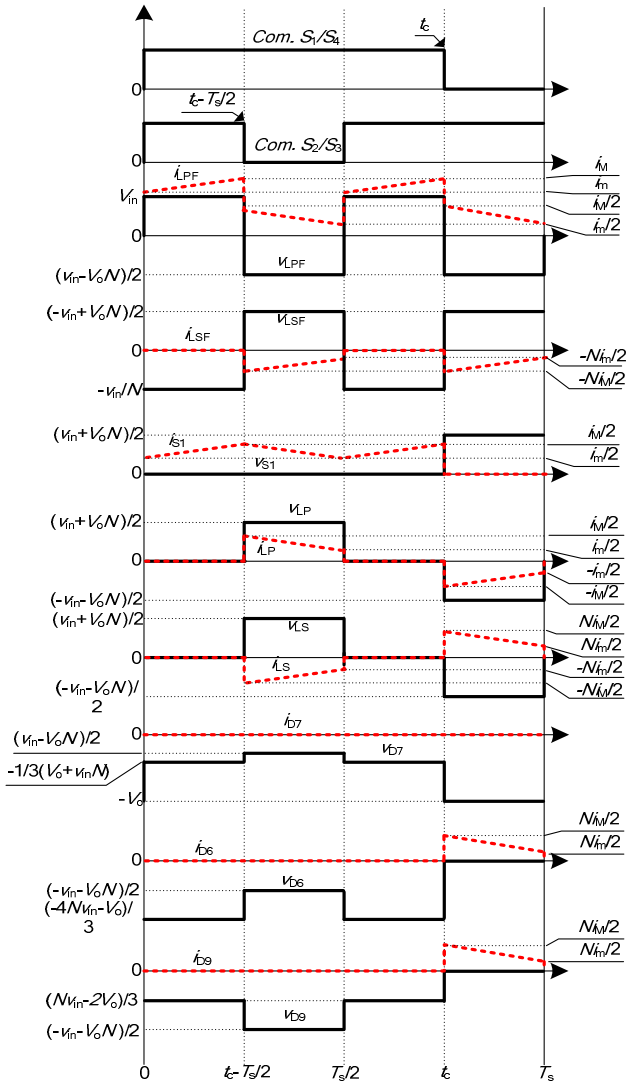

Fig. 6 Theoretical waveforms for the Boost mode

Again, the currents flowing through the primary and the secondary of the coupled inductor are equal, that is, $iL_{PF} = iL_{SF}$.During this stage there is energy transfer from input source to the output through D_3 and D_5. The fourth stage is presented in.Fig. 5.

The main waveforms for the Boost mode are shown in Fig. 6.

The static gain in this operation mode is:

$$G_{Boost} = \frac{V_o'}{V_{in}} = \frac{D}{1-D} \quad (1)$$

where:

$$V_o' = V_o N \quad (2)$$

and D is the duty cycle.

B. Buck mode

In this mode, the main switches operate with duty cycle between 0 and 0.5. The operation stages for this mode are presented as follows.

First Stage ($0 \le t \le t_c$): During this stage the switches S_1 and S_4 are on and S_2 and S_3 are off. The voltage across the primary inductor is $(V_{in} - NV_o)$ and the current iL$_{PF}$ increases linearly. There is energy transfer from input source to the output through the transformer, D_1 and D_4. The first stage of buck mode is presented in Fig. 7.

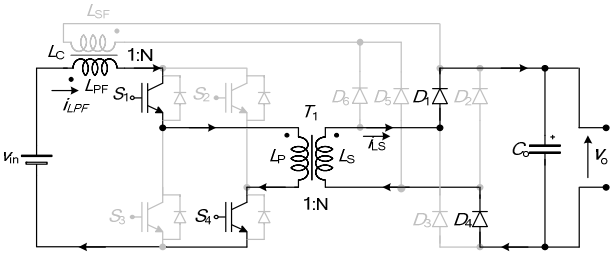

Fig. 7 First stage in Buck mode.

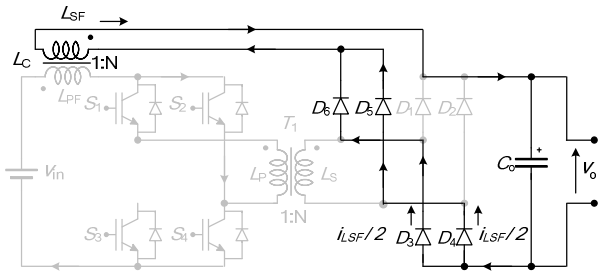

Fig. 8 Second and fourth stages in Buck mode.

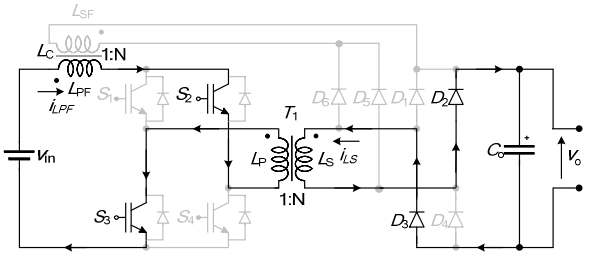

Fig. 9 Third stage in Buck mode.

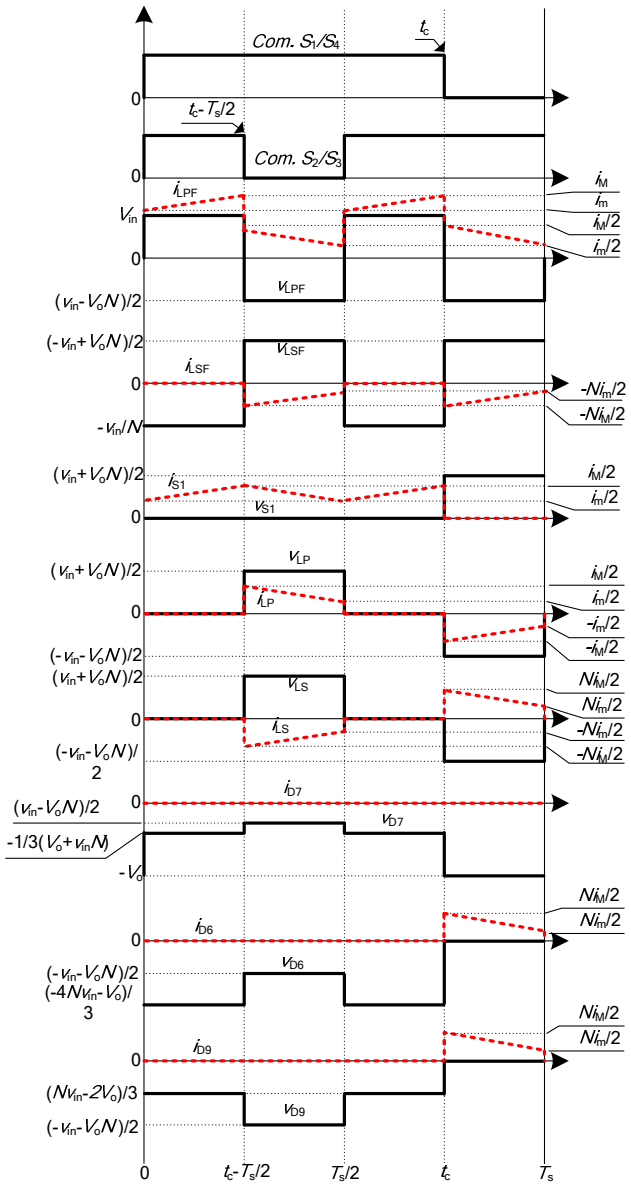

Fig. 10 Theoretical waveforms for the Buck mode.

Second Stage ($t_c \le t \le T_S/2$): In this stage all switches are turned off. The secondary inductor assumes the current, and it supplies energy to the output through D_3, D_4, D_5, and D_6. The voltage applied to the secondary inductor is $-V_o$ and the current decreases linearly. The second stage is presented in shown in Fig. 8.

Third Stage ($T_S/2 \le t \le t_c + T_S/2$): During this stage the switches S_2 and S_3 are turned on and S_1 and S_4 are still off. Again, the voltage across the primary inductor is $(V_{in} - NV_o)$ and the current iL$_{PF}$ increases linearly. There is energy transfer from input source to the output through the transformer, D_2 and D_3. The third stage is shown in Fig. 9.

Fourth Stage ($t_c + T_S/2 \le t \le T_S$): The fourth stage is identical to the second stage. Thus, the fourth stage operation can be observed in Fig. 8. The main waveforms for the Buck mode can be seen in Fig. 10.

The static gain in this operation mode is:

$$G_{Buck} = \frac{V_o'}{V_{in}} = 2D \quad (3)$$

III. TRANSITION BETWEEN BOOST AND BUCK MODES

The transition between the Boost and Buck modes occurs when the duty cycle reaches 0.5. At this point, both operation modes present the same static gain, as can be observed in Fig. 11. Therefore, the transition between these two modes is smooth for the proposed converter.

For Boost mode, the duty cycle can be estimated from the following expression:

$$D(\omega t) = \frac{V_o'}{V_o' + V_P \sin(\omega t)} \quad (4)$$

On the other hand, for Buck mode, the duty cycle behavior can be computed by:

$$D(\omega t) = \frac{V_o'}{2 \cdot V_P sen(\omega t)} \quad (5)$$

Fig. 12 shows the amplitude of the duty cycle for a half-period of the utility grid, considering $V_o = 200$ V and $V_P = 311$ V.

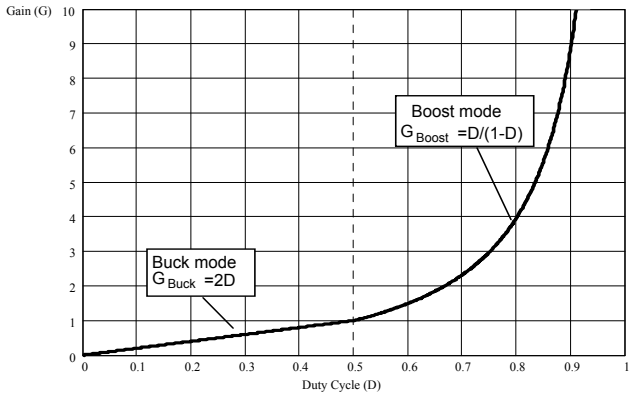

Fig. 11 Static gain *versus* duty cycle.

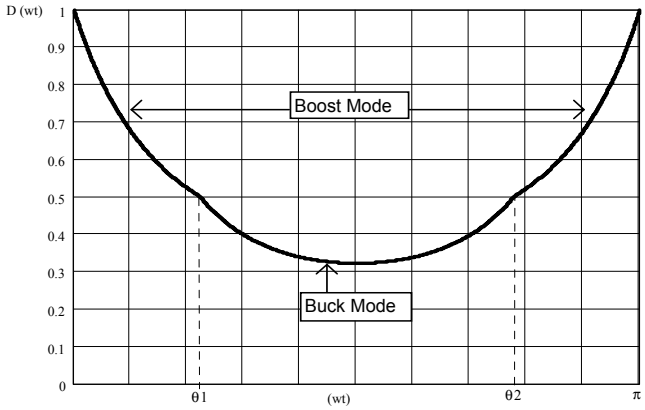

Fig. 12 Duty cycle for a half-cycle of the utility grid.

IV. DESIGN CONSIDERATIONS

The main parameters to be designed for the proposed converter are transformer and coupled inductor turns ratios, the inductance of the coupled inductor and the output capacitance.

Due to the dc voltage gain of this converter, the turns ratio can vary within a wide range and it can be computed from distinct specifications. An optimum turns ratio can be obtained to minimize the losses at the main switches or to limit the maximum voltage across the main switches. As optimization is not the main objective of this paper, an unitary turns ratio (N=1) was adopted for the transformer and for the coupled inductor.

Furthermore, the inductance L_C must be determined to limit the maximum current ripple in the coupled inductor Δi_{LPF}. The maximum ripple in magnetizing current i_{LPF} occurs at the step down mode, so that the inductance can be computed from (6), using the voltage applied in the primary side of the coupled inductor at this operation mode:

$$L_C = \frac{0,5 V_P T_S}{2 \Delta i_{LPF}} \quad (6)$$

In addition, the output capacitance can be calculated from the following expression:

$$C_o = \frac{P_o}{4\pi f_r V_o \Delta V_o} \quad (7)$$

where P_o is the output power and f_r is the rectified input voltage frequency.

MODULATION AND CONTROL STRATEGY

The command signals of the main switches can be obtained from the comparison of the control signal with two sawtooth signals phase-shifted among them with 180°, as illustrated in Fig. 13. The sawtooth signals are the input of two different comparators. The other inputs of the comparators are connected to the same control signal. The output of one comparator is the command signal of S_1 and S_4, and the output of the other comparator is the command signal of S_2 and S_3.

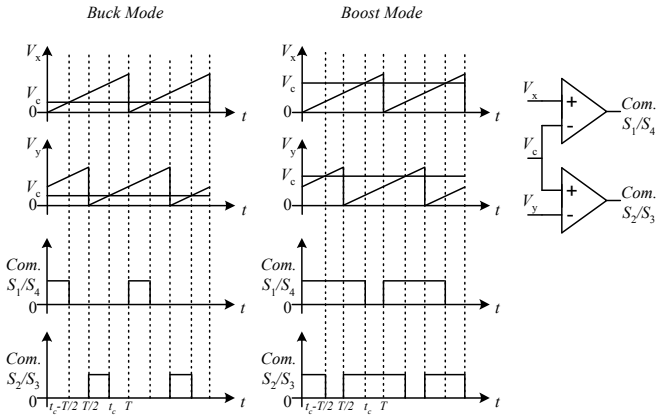

Fig. 13 Proposed PWM modulation technique

The control strategy applied to this converter is the Average Current Mode Control [10]-[12], using the current of the flyback coupled inductor as the control parameter.

The converter has input current control and output voltage control. A simplified block diagram of the control strategy is shown in Fig. 14.

The output of the voltage controller is multiplied by a rectified utility grid voltage and its result is the reference to the current control. The current controller forces the input current to follow the reference current, which is in-phase with the rectified input voltage. The output voltage controller

increases or decreases the amplitude of the reference current according to the error voltage so that the output dc voltage is regulated to the reference voltage.

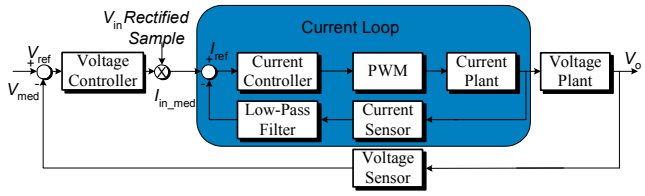

Fig. 14 Simplified block diagram of the control strategy.

V. EXPERIMENTAL RESULTS

A prototype of the full-bridge flyback isolated current rectifier was implemented in our lab to verify the performance of the proposed converter under practical conditions. The design specifications of this prototype are presented in Table 1.

Table 1
Design specifications

$P_o = 3.5$ kW	Output power
$V_o = 400$ V	Output voltage
$V_{in} = 311\sin(\omega t)$ V	Input voltage
$\Delta V_o = 1$ %	Maximum output voltage ripple
$f_r = 60$ Hz	Input frequency
Fs = 75 kHz	Switching frequency
$\Delta i_{LPF} = 10\ \% \cdot i_{LPFpk}$	Maximum input current ripple
$\eta = 90$ %	Efficiency
$N = a = 1$	Turns ratio

A schematic diagram of the prototype is shown in Fig. 15.

The implemented prototype is presented in Fig. 16.

It was necessary to include RCD clamp circuits and a snubber circuit to limit the voltage in all semiconductors, because the energy stored in the transformer and coupled inductor leakage inductances cause high transient voltages in the semiconductors.

Once this converter operates with high power levels, the energy stored in leakage inductance is high. However, this energy has not a natural path to discharge itself, so it is necessary to use voltage clamp circuits.

An Undeland snubber [13] was chosen to limit the voltage in the switches, and individual RCD clamp circuits to protect the diodes. These circuits can be observed in Fig. 15.

The main components used in prototype are specified in Table 2. The control system was implemented in a DSP TMS320F2812 of Texas Instruments® [15]-[17]. Drivers circuits SKHIOPA from Semikron® were used and an interface board was included to adapt the signals from DSP to the power circuit.

The experimental results were obtained using a digital oscilloscope TPS2024 model of Tektronix®. The waveforms were obtained through files that contain the points relative to the measured waveforms. The points were exported to MatLab® software and then plotted the figures.

Fig. 17 shows the input voltage and input current waveforms with a load equal to 58.6 Ω, an output voltage equal to 400.0 V and nominal input voltage.

The harmonic spectrum of the input current waveform is shown in Fig. 18 and it is compared with the limits imposed by IEC61000-3-2 standard class A [14].

At this operating point, the converter operates only in Boost mode and all the current harmonics are lower than the standard, as can be seen in Fig. 18. The total harmonic distortion (THD) of the input current waveform is 3.65% and the input power factor is 0.99.

Fig. 19 shows the voltage in switch S_1 and the primary inductor current.

In addition, the performance of the proposed converter was investigated for a smaller output voltage. By using an output voltage equal to 200 V the proposed converter operates in both modes (Boost and Buck modes). The load resistance was set to 30.5 Ω.

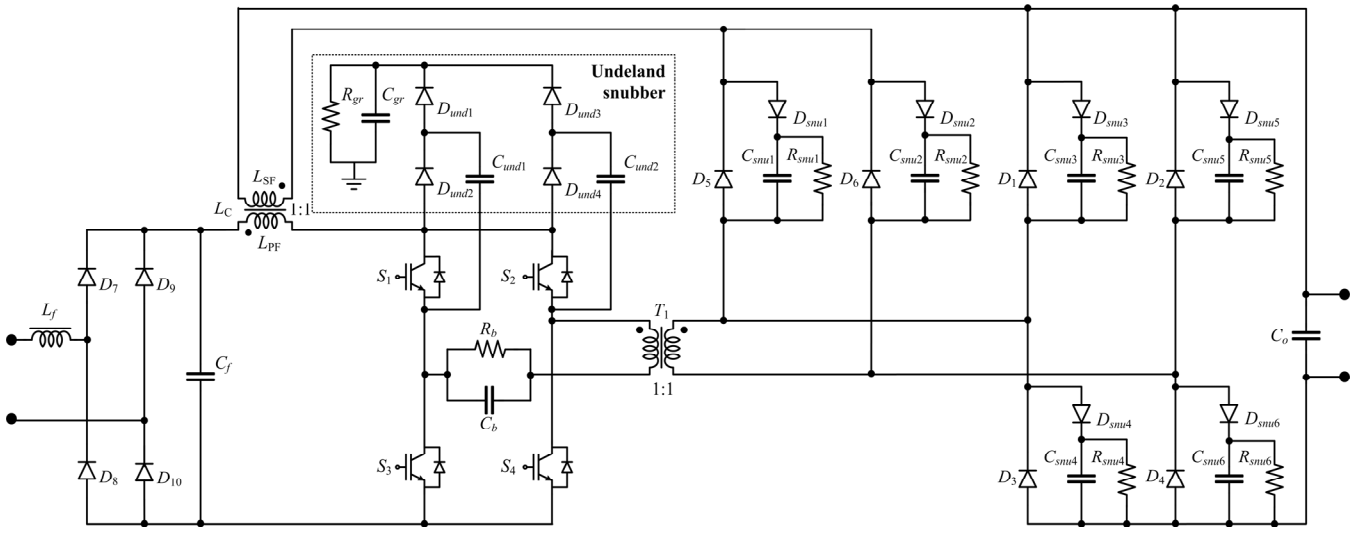

Fig. 15 Schematic diagram of the prototype.

Table 2
Main components

S_1, S_2, S_3, S_4	Switches: IRGP50B60PD
D_1, D_2, D_3, D_4, D_5, D_6	Diodes: HFA16TB120
D_7, D_8, D_9, D_{10}	Bridge rectifier: SK50B08
C_o	Electrolytic capacitor: 6 x 470µF/400V
L_F	Toroidal inductor: Iron powder, L=100µH, 32 turns
C_f	Polypropylene capacitor: 5µF
Coupled inductor	Ferrite inductor: IP6-EE65/91, L=200µH, 16 turns, total leakage inductance = 12µH
Transformer	Ferrite transformer: IP6-EE65/91, 10 turns, total leakage inductance = 4µH
R_b	Resistor: 3 x 47Ω/3W
C_b	Polypropylene capacitor: 2.2µF/400V
D_{snu1}-D_{snu6} and D_{und1}-D_{und4}	Diodes: MUR4100
C_{und1},C_{und2}	Polypropylene capacitor: 4.7nF
R_{snu3}-R_{snu6}	Resistor: 90kΩ/3W
R_{snu1}, R_{snu2}	Resistor: 156kΩ/3W
C_{gr}	Electrolytic capacitor: 73 µF/750V
R_{gr}	Resistor: 3.3kΩ/600W

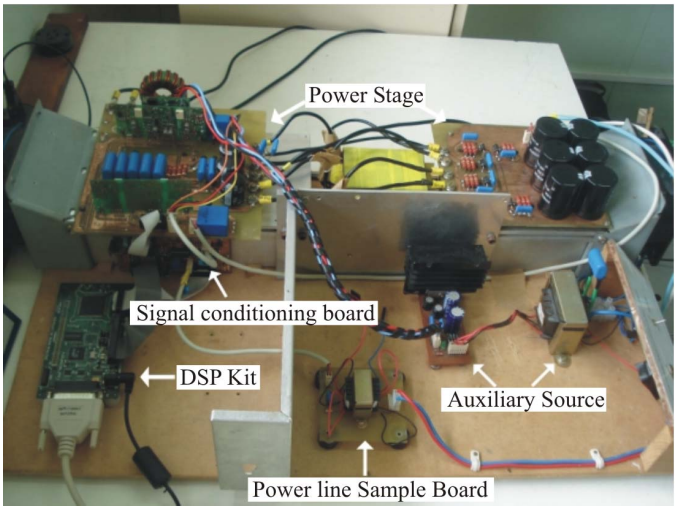

Fig. 16 Developed System.

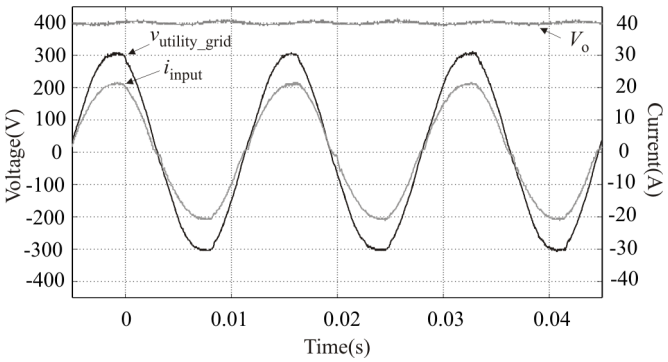

Fig. 17 Input/output voltage and input current.

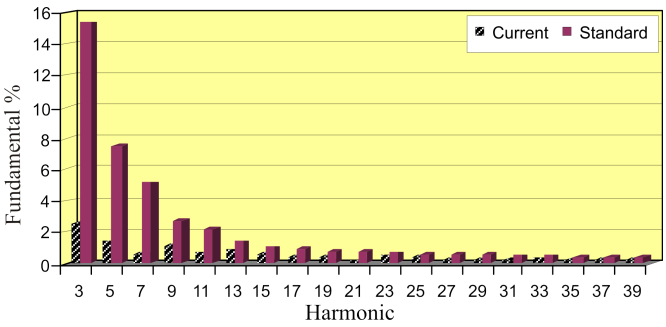

Fig. 18 Harmonic spectrum of the input current waveform for Boost mode and the IEC61000-3-2 Class A limits.

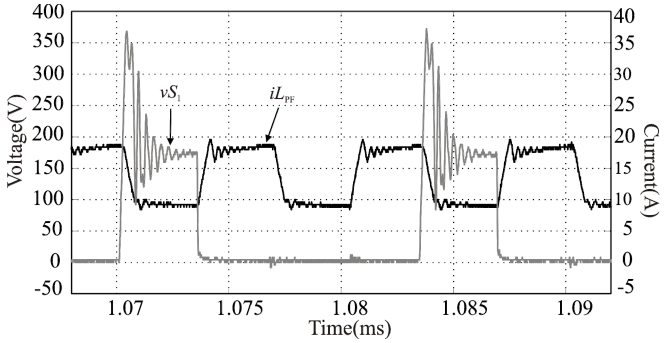

Fig. 19 Primary inductor current and S_1 voltage.

Fig. 20 shows the output and input voltages and the input current for this operating point.

Fig. 21 shows the harmonic spectrum of the input current waveform presented in Fig. 20 and it is compared with the limits specified by IEC61000-3-2 standard.

In this case, the THD of the input current waveform is 7.72 % and the input power factor is 0.98. The harmonics 13, 15 and 19 don't satisfy the IEC61000-3-2 Class A limits.

As can be observed in Fig. 20 and Fig. 21, the input current THD increases when the converter operates in Buck mode. The input current waveform is distorted because a fraction of the energy stored in the primary coupled inductor, in the first and third stages, is not transferred to the secondary coupled inductor in other stages. This occurs because there is a smaller impedance path through the Undeland snubber. Consequently, the Undeland snubber chosen to this converter is not efficient for the Buck mode.

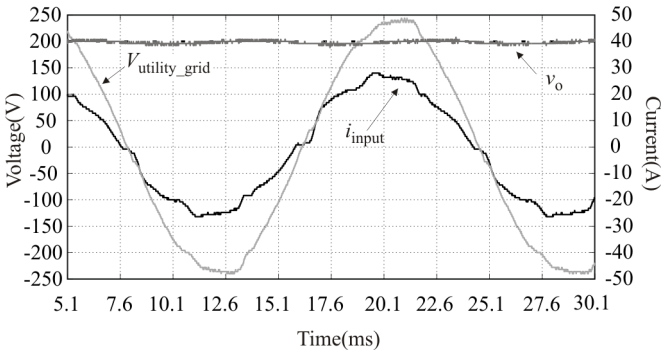

Fig. 20 Input and output voltages and input current.

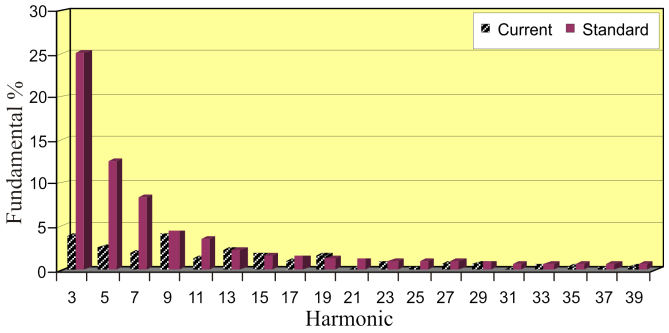

Fig. 21 Harmonic spectrum of the input current waveform for Boost/Buck modes and the IEC61000-3-2 Class A limits.

VI. CONCLUSIONS

It is possible to conclude from analysis and results presented in this paper that the full-bridge flyback isolated current rectifier satisfies the proposed specifications, which are: single-stage converter, high power factor, galvanic isolation, magnetic components operating at high frequency, output voltage control, low startup input current, step-up or step-down operation and reduced number of switches (41% less than the Push-Pull topology). The control system is very simple and the well-known Average Current Mode Control was used for power factor correction.

The leakage inductances in this converter have a great influence in the converter efficiency. The efficiency obtained in this prototype is 75%. Due to the cores employed to build the coupled inductor and the transformer the leakage inductances are high. A suggestion for future works is to use a planar transformer and coupled inductor which have a very low leakage inductance [18].

Another suggestion is to use RCD clamp circuits in each switch, so that the input current is not distorted in Buck mode. Moreover, it is possible to implement an isolated converter to regenerate the energy stored in leakage inductances, transferring this energy to the output. However, it is not necessary to transfer this energy from inductances by using planar magnetics, because the energy loss would be too low.

REFERENCES

[1] G. Chu, Tan Siew-Chong, C. K. Tse, Siu Chung Wong ”General control for Boost PFC converter from a sliding mode viewpoint” PESC 2008 IEEE, pp. 4452-4456, June 2008.

[2] L. Ping, M. Yu, K. Yong, Z. Hui, C. Jian, “Analysis of single-phase boost power factor correction (PFC) converter”, PEDS ‘99 *IEEE,* vol. 2, pg. 933-937, July 1999.

[3] J. W. Kim, S. M. Choi, K. T. Kim, “Variable on-time control of critical conduction mode boost power factor correction converter to improve zero-crossing distortion” PEDS ‘2005 *IEEE,* vol. 2, pg. 1542-1546, Nov. 2005.

[4] Lizhi Zhu “A noval soft-commutating Isolated Boost Full-Bridge ZVS-PWM DC-DC converter for bidirectional high power applications” IEEE transactions on power eletronics, vol. 21, no. 2, pg. 422-429, March 2006.

[5] A. Ahmed, E. V. Mack, “Power Eletronic” Book, Ed. Prentice Hall, São Paulo 2000.

[6] G. V. T. Bascopé, “Conversor Flyback-Push-Pull alimentado em corrente com correção de fator de potência” Master dissertation, Pg. 140, Universidade Federal de Santa Catarina, June-1996.

[7] I. Barbi, D. Ruiz-Caballero, “A new ZVS-PWM clamping mode isolated non pulsating input and output current DC-to-DC power converter” *IEEE INTELEC’99*, 20-1, Copenhagen-Denmark June 5-10, 1999.

[8] P. Em-Sung, J. C. Sung, J. M. Lee, B. H Cho, “A soft-switching active clamp scheme for isolated full-bridge boost converter”, APEC’04 IEEE, vol. 2, pg. 1067-1070, 2004.

[9] R. Watson, F. C. Lee, “A soft-switched, full-bridge boost converter employing an active-clamp circuit”, PESC’96 Record IEEE, vol. 2, pp. 1948-1954, 1996.

[10] P. Chrin, C. Bunlaksananusorn, “Novel Current Feedforward Average Current Mode Control Technique to Improve Output Dynamic Performance of DC-DC Converters” PEDS 2007, pg. 1416-1421, Nov. 2007.

[11] W. R. Erickson, D. Maksimovic, “Fundamentals of power eletronics” Book, Second Edition, University of Colorado, 2001.

[12] W. Tang, F. C. Lee, R. B. Ridley, “Small-signal modeling of average current-mode control”; IEEE APC’92 Conference Proceedings, 1992. pg. 747-755.

[13] T. M. Undeland, “Switching stress reduction in power transistor converters”; IEEE Industry Applications Society, p. 383-391, 1976.

[14] Internacional Standard “Limits for harmonic current emissions” 2005.

[15] P. Kornetzky, Z. Moussaqui, I. Batarseh, S. Hawasly, C. Kennedy, “Modeling Technique for DC to DC Converters Using Weinberg Topology”; IEEE SoutheastCon’96, Tampa, FlL. pp. 551-556, April 1996.

[16] TMS320F2812 Data manual, Literature Number SPRS174L, Dec/2004.

[17] DSP (digital signal processing) development tools, Code Composer Studio, applications software, C6000, C5000, C2000.

[18] E. Maset, A. Ferreres, J. B. Ejea, E. Sanches-Kilders, J. Jordan, V. Esteve “5kW Weinberg converter for battery discharging in high-power communications satellites”; PESC’2005 Record, 36th Annual IEEE, 2005 pg. 69-75.