Bidirectional Rectifier – Comparison between Average Current and "dq0" Coordinates Control Techniques Implemented on DSP

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***Abstract* – This paper shows a comparison between two different control strategies to the bidirectional rectifier with high power factor. The same hardware was applied during the tests for both control techniques and with the controllers implemented on Texas TMS320F2812 DSP. Besides the techniques, this paper will focus on the differences to carry out the controllers and in the results for each applied methodology.**

***Keywords* – Digital control, bidirectional rectifier, rectifier with high power factor and PFC.**

I. INTRODUCTION

The digital control application over analogical processes was intended a long time before the technological development to make able its use. Otherwise, nowadays, the digital control, since correctly structured, could be applied in the most processes due to the development of the digital processors.

Bidirectional three-phase rectifiers with high power factor were widely used so much in the academic research as in industrial applications, and can be found in the literature in many references, with a large base of knowledge. Some of these studies use classical control and its requirements as a starting point to the project of the controllers.

By following the natural evolution of Power Electronics and Digital Control, some different models to the rectifier circuit were developed. In this paper will be illustrated two different techniques used to control this rectifier and the results obtained from these techniques carried out using the same hardware. This methodology creates conditions to compare the final results of the techniques in order to prove or dismythfy some points relative the efficiency of each one of them.

II. TOPOLOGY

The power circuit of the proposed rectifier can be seen in the Fig. 1, where a two level conventional configuration was used. The chosen topology is well known on the literature because it's widely used as a three-phase inverter or a PFC. It has positive characteristics as to make possible bidirectional power flux, low total harmonic distortion and nice output voltage regulation. On the other hand, it's necessary a bigger effort and caution on the conception of the command and control circuits, which should prevent the output short-circuits through the semi-conductors switches. Other important characteristic is that the output voltage must be higher than the pick of the input line voltage ([1] to [5]).

The converter used to realize the tests was developed to operate with the parameters showed on the Table I.

Beyond the power circuit, other items those are included in the hardware, as sensors, signal conditionings, filters, inductors and DSP. On the Fig. 2 a blocks diagram shows the functional parts of the hardware project.

In order to design the control, it's necessary to define some parameters to be used. These parameters are showed on the Table II.

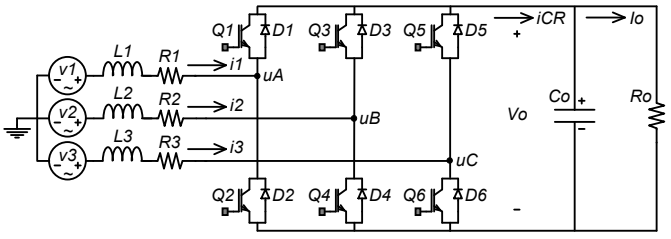

Fig. 1. Classical two level topology for power circuit converter.

TABLE I
PROJECT REQUIREMENTS

Output power	$P_O = 2500W$
Output voltage	$V_O = 400V$
RMS phase voltage (source)	$V_{IN} = 127Vrms$
Ripple current (%maximum)	$\Delta i_L = 0.10$ (10%)
Output ripple voltage (%maximum)	$\Delta V_O = 0.05$ (5%)
Switching frequency	$f_S = 20kHz$
Sampling period	$T_s = 1/20kHz$
Circuit efficiency (estimated)	$\eta = 0.87$

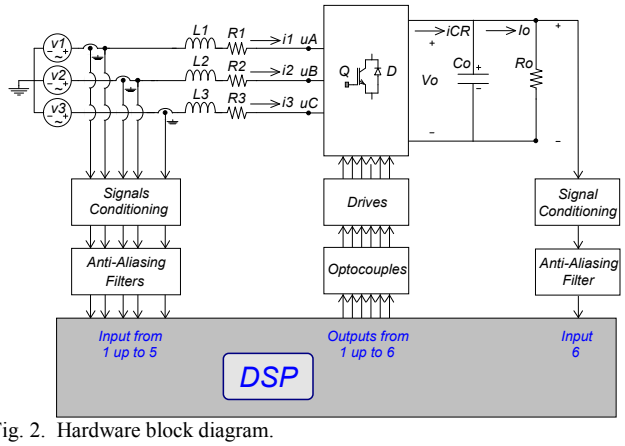

Fig. 2. Hardware block diagram.

TABLE II
PARAMETERS TO THE CONTROLLERS DESIGN

Triangle carrier wave amplitude	$V_T = 3750$
Peak of voltage phase input	$V_P = 180V$
Peak of current phase input	$I_P = 10.67A$
Input inductance (L = L1=L2=L3)	$L = 2.74mH$
Input resistance	$R = 0.1\Omega$
Output capacitance	$C_O = 1500\mu F$
Sampling frequency	$f_s = 20kHz$
Current sensor gain	$K_i = 0.1$
Voltage sensor gain	$K_v = 6.5x10^{-3}$
Multiplication gain	$K_M = 1$
ACD gain to current	$K_{ADc} = 2^{11}/3$
ACD gain to output voltage	$K_{ADv} = 2^{12}/3$
Anti-aliasing gain	$K_{AA} = 1$
Converter gain, $(V_O/2V_T).1.15$	$K_{conv} = 61.3x10^{-3}$
Current loop gain, $K=K_{conv}.K_i.K_{ADc}$	$K = 4.18$
Voltage "d" axis on the operation point	$V_{dP} = 180V$
Output voltage on the operation point	$V_{OP} = 400V$

III. AVERAGE CURRENT CONTROL

The average current control is a technique quite used to control this kind of converter, mainly for analogical controllers. The digital accomplishment for this technique allows reusing all solid knowledge acquired and structured by the classical continuous control theory. However, some considerations and adaptations are necessary during the converter analysis because the digitization process results in changes of the plant.

A. Current loops

In a design methodology to digital controllers is necessary some modifications on the analysis to tune the converter analysis to the digital world ([6] and [7]).

Among the necessary changes, note the reference for the input current wave is generated inside the DSP. Then, the distortion existent on the input voltage signal doesn't disturb the input current wave form. Other particular characteristic for digital systems is the necessity to sample analogical signals from the real plant and carry them on to the discrete universe inside the DSP. Therefore, samplers and holders (zero order holders) appear on the blocks diagram. To complete the control structure transfer from the analogical world to the discrete world, anti-aliasing filters was included on the system to limit the signal frequency spectrum before the sampling process. In order to use the ADC (analog-digital converter) is necessary to consider its gain on the analysis. Fig. 3 shows the current loop diagram transferred to the discrete universe and the Fig. 4 represent the output voltage loop diagram.

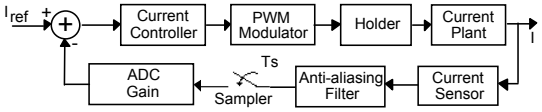

Fig. 3. Digital current loop blocks diagram.

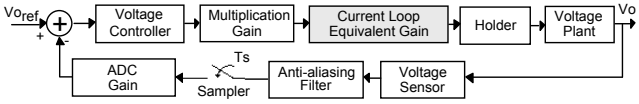

Fig. 4. Digital voltage loop blocks diagram.

B. Modeling

The voltage and current plants are digitized from the continuous model with a sample period T_s. The converter modeling can be found in the literature [2] and [8]. With the digitized transfer functions, Tustin bilinear transformation is used to converter the model from the ***z*** plan to ***w*** plan, where the controller design can be done with the same techniques used on continuous systems. Tustin inverse transform will convert the controllers from the ***w*** plan to ***z*** plan again. The current transfer function is showed in (1), where variables used on it are defined on Tables I and II. The voltage plant transfer function is showed in (2):

$$\frac{i(w)}{d(w)} = \frac{V_o}{\frac{2}{3}L.V_T}.\frac{1-\frac{T_s}{2}w}{w} \quad (1)$$

$$\frac{V_O(w)}{I_P(w)} = A_1.\left(\frac{1-e^{-T_s/A_2}+w.\frac{T_s}{2}\left(e^{-T_s/A_2}-1\right)}{1-e^{-T_s/A_2}+w.\frac{T_s}{2}\left(1+e^{-T_s/A_2}\right)}\right) \quad (2)$$

where

$$A_1 = \frac{3.V_P.V_o}{2.P_o} \quad (3)$$

and

$$A_2 = \frac{C_o.V_o^2}{P_o} \quad (4)$$

C. Design Precedents

The controllers design on the ***w*** continuous plan follow the [9] rules. Based on the blocks diagram showed in Fig. 3, the open-loop transfer function for the current plant is:

$$G(w)_i \times H(w)_i = H_i(w).\frac{V_O.K_i.K_{ADc}}{\frac{2}{3}.L.V_T}.\frac{1-\frac{T_s}{2}.w}{w} \quad (5)$$

From (5), it's possible to note that the system has a pole on the origin and a zero on high frequency. For this plant was choosed a proportional controller (P) as represented in (6).

$$H_i(w) = k_{Hi} \quad (6)$$

The current controllers were designed to obtain a phase margin between 45° and 90°, and a cross frequency by 0 dB in 2 kHz ($f_s/10$), then:

$$H_i(w) = 3.05 \tag{7}$$

Transferring the controller transfer function from ***w*** plan to ***z*** plan, and after that obtain the difference equation, it's possible to find (8):

$$y_i(n) = 3.05 \cdot \left(x_i(n) - x_i(n-1)\right) \tag{8}$$

Where x_i is the controller input and y_i is the controller output.

Using the blocks diagrams in the Fig. 4, it's possible to obtain the open-loop transfer function for the voltage plant:

$$G_v(w) \cdot H_v(w) = H_v(w).K_{ADv}.K_{i\_eq} \cdot \frac{V_O(w)}{I_P(w)} \tag{9}$$

From (9), it's possible to use a PI controller (Proportional-Integral) to close the design requisites. Then, the controller transfer function $H_v(w)$ will be:

$$H_v(w) = \frac{k_{Hv} \cdot (w + \nu_z)}{w} \tag{10}$$

where

- k_{Hv} is the controller gain;
- ν_z is the zero position in ***w*** plan.

The voltage controller parameters were designed to attend the criterion design for the cross frequency by 0dB in 36Hz.

$$H_v(w) = \frac{6.579 \cdot (w + 13.508)}{w} \tag{11}$$

Transferring the controller function from ***w*** plan to ***z*** plan, and after that obtaining the difference equation, it's possible to find (12):

$$y_v(n) = 6.1078 \cdot x_v(n) - 6.1042 \cdot x_v(n-1) + y_v(n-1) \tag{12}$$

D. Software Implementation

For carry out this step, it was used the TMS320F2812 DSP from *Texas Instruments*, more specifically the didactic kit eZdsp from *Spectrum Digital Inc*. The program was fully developed on high-level language (C++) using the *Code Composer* compiler [10].

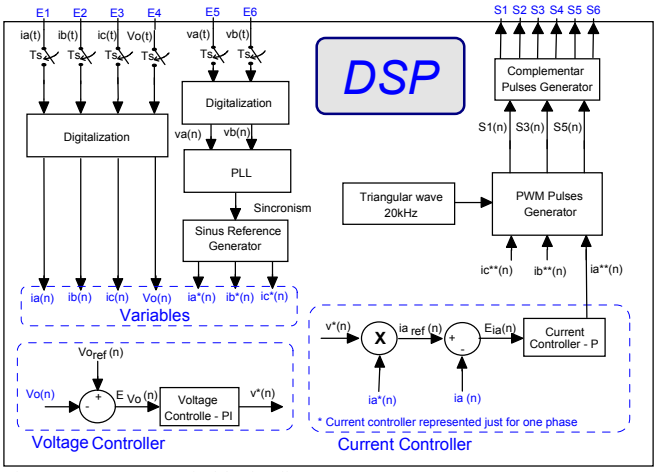

Fig 5 – DSP program in blocks diagram.

An illustrative diagram in the Fig. 5 represents the functional structure for the controllers' software. It shows the main blocks of the program carried out in the DSP.

E. Experimental Analysis

During the converter operation as a rectifier, with energy flux from source to output DC link and with nominal load, the current waveform is almost identical to the voltage waveform. The input voltage and input current waves for this situation are shown in the Fig. 6. Fig. 7 shows the three-phase input current

In the Fig. 8 are showed the output voltage and input current (for one phase) during a load switching. In this case, the system is switched from 100% to 50% of nominal load.

To validate the performance of the designed control relative to the regeneration, a power injection in the DC link is made to induce the system to regenerate the excess of energy. Fig. 9 shows the moment where happened the injection of power in the output and changes of direction on the energy flux in the input sources.

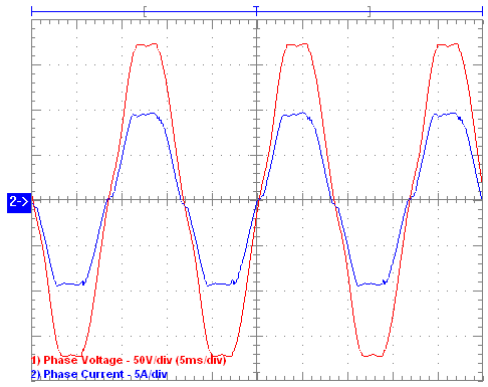

Fig. 6 – Input current and voltage for one phase.

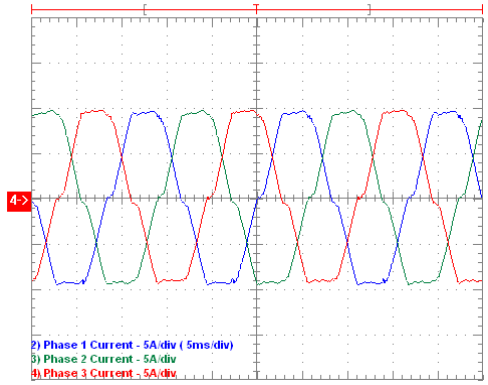

Fig 7 – Three-phase input current.

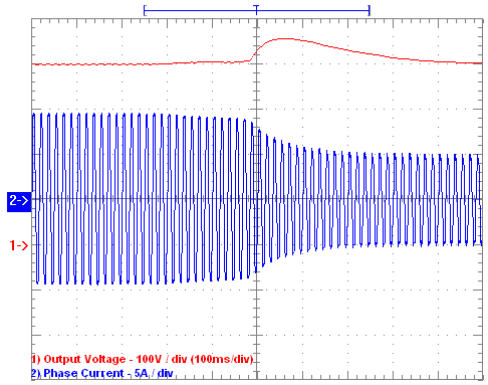

Fig. 8 – Step of load from 100% down to 50%

The output voltage and input current, for one phase, during the start and end of regeneration period are showed in the Figs. 10 and 11.

The saturation found on the output voltage during the end of regeneration is occasioned by the action of the protection on power supply used to inject power in the system.

Considering the converter operation as a rectifier with nominal load, we have the following operational indices:

TABLE III
PERFORMANCE OF AVERAGE CURRENT CONTROL

Power Factor	PF = 0,9984
Voltage Total Harmonic Distortion	THDv = 2.7%
Current Total Harmonic Distortion	THDi = 6.6%
Displacement Power Factor	F_{sh} = 3.2º
Output Voltage Ripple	ΔV=±1V

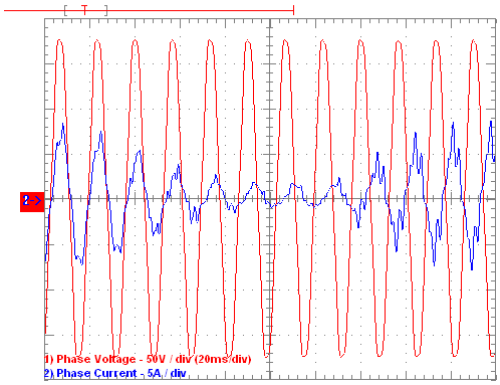

Fig. 9 – Flux power inverting.

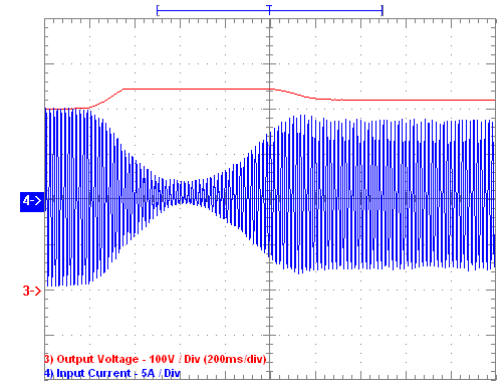

Fig. 10 – Start of recovery energy.

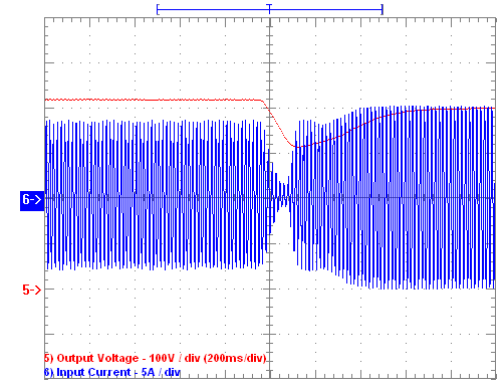

Fig 11 – End of recovery energy.

IV. CONTROL IN DQ0 COORDINATES

The control in *dq0 coordinates* is based on representation of the electric variables, in similar form to the vectors, in a frame of orthogonal components that can be either stationary or rotating [11]. From this representation, it is possible to obtain a control totally or partially decoupled between the variables of direct "d" and quadrature "q" axis, so that it can be possible, for example, to control the amplitude and the phase of any signal in an independent way. The alignment of vectors can also facilitate the control, because it's possible to reduce the amount of variables and the order of the system. In fact, the artifice of decoupling of variables physically linked can also to improve the response of the system for specific prerequisites of control.

A. Control Loops

Fig. 12 presents the current loops of "d" and "q" axis. As the loops are identical, both are represented in the same figure. In this way, the Fig. 13 shows the modeling to the voltage loop of the DC link. The same considerations of the *average current* technique, previously presented, have been kept. From Fig. 12, using the transformations to lead from ***s*** to ***z*** plan, it's possible to arrive at the following transference function to the current loops of "d" and "q" axis in the ***w*** plan:

$$G(w)_{i_{dq}} = \frac{K}{R}\cdot\left(1 - w \Big/ \left(\frac{1-e^{-R/L\,Ts}}{T_s}\right) + \left(\frac{1+e^{-R/L\,Ts}}{2}\right)\right) \qquad (13)$$

Similarly, from the Fig. 13 it's possible to obtain the following transference function to the voltage loop of DC link in the ***w*** plan:

$$G(w)_v = A_3 \cdot \frac{\left(1 - T_s/2 \cdot w\right)}{w} \qquad (14)$$

where

$$A_3 = \frac{V_{dP}}{C_O . V_{OP}} \cdot \frac{K_{ST}}{K_{SC}} \cdot \frac{K_{AD_T}}{K_{AD_C}} \qquad (15)$$

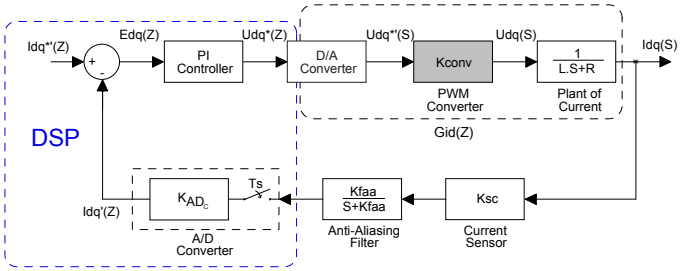

Fig. 12. Current loops with not unit Feedback.

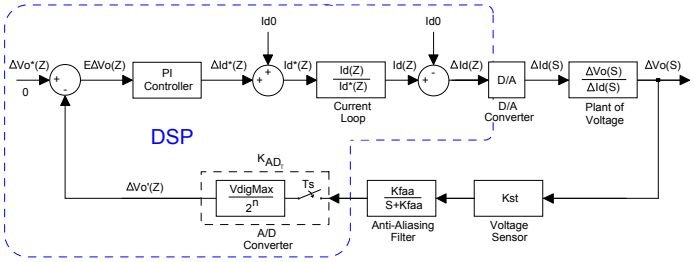

Fig. 13. Voltage loop with not unit feedback.

B. Design Procedures

Looking for that the current loops keeps phase margin between 45º and 90º, and cross over frequency by 0 dB at 2.0 kHz (fs/10), it's found the following values to the PI controllers:

$$\begin{cases} K_P = K_{PI} = 8.94 \\ K_I = K_{PI} \cdot Zw = 8.94 \cdot 100 = 894 \end{cases} \quad (16)$$

where, K_P represents the proportional gain, K_I the integrative gain and Zw represents the zero of the controllers.

In a similar form, looking for that the voltage loop keeps phase margin between 45º and 90º, and cross over frequency by 0 dB at 36 Hz, it's found the following values to the PI controller:

$$\begin{cases} K_P = K_{PI} = 4.72 \\ K_I = K_{PI}.Zw = 4.72 \cdot 50 = 236.13 \end{cases} \quad (17)$$

where, again, K_P represents the proportional gain, K_I the integrative gain and Zw represents the zero of the controller.

In order to implement the controllers on the DSP, they are rearranged in difference equations form. In this way, from (13) to (17), it's not difficult to arrive in the equations (18) and (19), being, respectively, the first to the current controls of "d" and "q" axis, and the second to the voltage control of DC link, as follow:

$$y_{idq}(n) = 8.9619.x_{idq}(n) - 8.9172.x_{idq}(n-1) + y_{idq}(n-1) \quad (18)$$

$$y_v(n) = 4.7286.x_v(n) - 4.7168.x_v(n-1) + y_v(n-1) \quad (19)$$

C. Control Software Implementation

The functional control structure of the converter in *dq0 coordinates* can be observed on the schematic illustrative diagram from Fig. 14, where are represented the software blocks internally implemented on DSP [10]. A symmetric three-phase regular PWM technique was used ([12] and [13]).

D. Experimental Results

Fig. 15 shows the results for one input phase, for the converter operating as a rectifier, with nominal load. Fig. 16 shows all three input currents on same conditions.

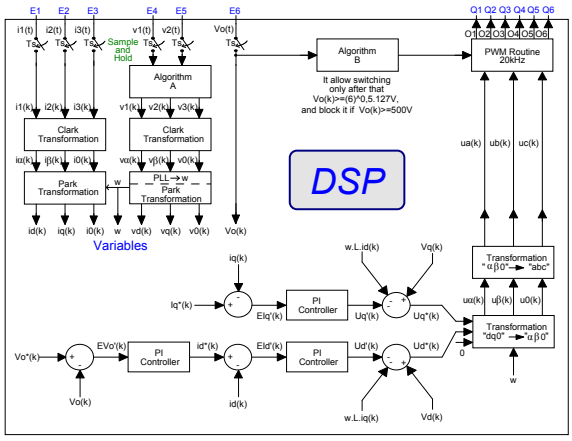

Fig. 14. DSP Program in blocks diagram.

Fig. 17 shows the behavior of voltage in the DC link under a step of load from 100% down to 50%.To validate the performance of the control with relation to reversibility, the same procedures of the previous technique have been used. Thus, the Fig. 18 shows in detail the energy flux reversion, and the Figs. 19 and 20 show the voltage on the DC link and the input current for one phase for the conditions of end and beginning of recovery energy, respectively.

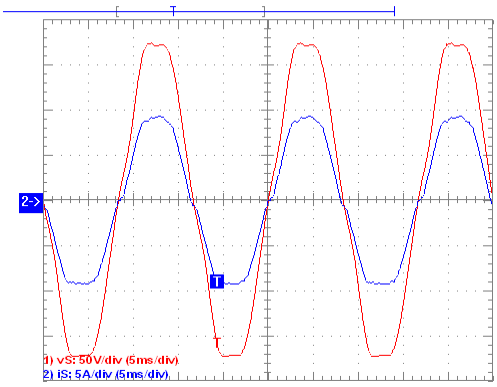

Fig 15 – Input current and voltage for one phase.

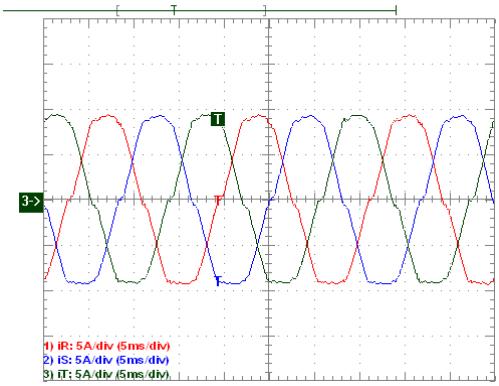

Fig 16 – Three-phase input current.

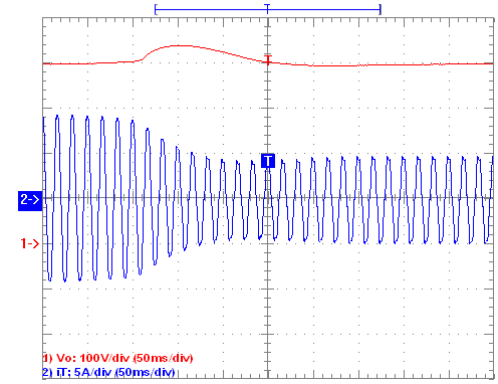

Fig. 17 – Step of load from 100% down to 50%.

Table IV presents the converter performance operating in nominal power as follows:

TABLE IV
PERFORMANCE OF "DQ0" CONTROL STRATEGY

Power Factor	PF = 0.9964
Voltage Total Harmonic Distortion	THDv = 5.2%
Current Total Harmonic Distortion	THDi = 6.7%
Shifting Phase	F_{sh} = 1.86º
Output Voltage Ripple	ΔV=±1V

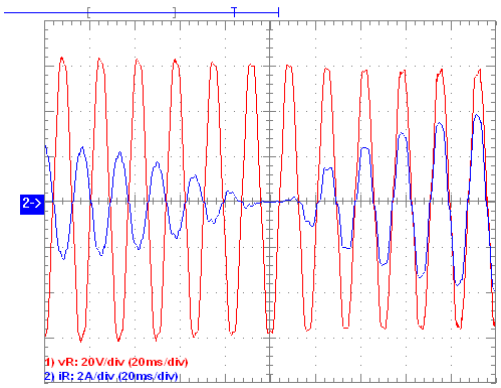

Fig. 18 – Flux power inverting.

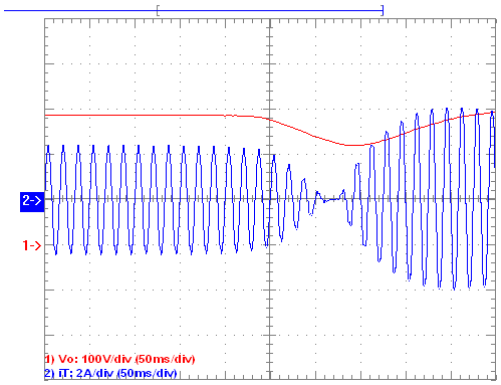

Fig. 19 – End of recovery energy.

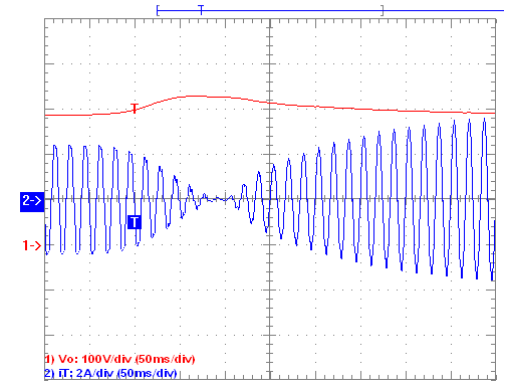

Fig. 20 – Start of recovery energy.

V. CONCLUSIONS

From experimental results in full load condition, it can be affirmed that the converter have presented identical performance for both control techniques. However, evaluating transitory response, the *average current* technique has presented slower results when compared to *dq0* technique. This fact can have been happening because of the characteristics of the software and we believe it could be solved using a float point DSP. Comparing the techniques it's possible to verify that the *average current* has a small difference on the output voltage that depends on the energy flow. It's happen because the model for rectifier mode is different of the model for inverter mode (regeneration stage). On the *dq0 coordinate* control this change doesn't occur. In other hand, comparing both control strategies, the *average current* technique uses less memory (98k bytes) and the algorithm is faster (15µs) than the *dq0 coordinates* technique, who use 103k bytes and whose routine run time is around 39µs. The safe memory is not significance, but the run time processing in *average current* tecnique to make able to include other routines or increase the switching frequency. The delay on the *dq0 coordinates* occur mainly because is necessary to transform the *abc* to *dq0*, and vice-versa.

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