A New Digital Control System for a Single-Phase Half-Bridge Rectifier with Fast Dynamic Response

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***Abstract* – This paper proposes a digital control system for a half-bridge boost rectifier, which composes the input stage of a single-phase transformerless double-conversion UPS. The proposed control system has an inner current loop and two outer voltage loops to maintain near unity input power factor and to regulate the dc bus voltages. The control loops operate with distinct sampling frequencies, so that current loop operates with high sampling frequency, and voltage loops operate with reduced sampling frequency and moving average filters to improve the dynamic response, without affecting the input power factor. Experimental results are included to demonstrate the performance of the closed-loop system.**

***Index Terms* – AC-DC converter, digital control, power factor correction.**

I. INTRODUCTION

Double-conversion UPSs (Uninterruptible Power Systems) have been largely used to protect critical loads, because they present several advantages: (i) low-THD (Total Harmonic Distortion) output voltages can be synthesized with amplitude and frequency independent of the respective values of the input voltages, (ii) zero transfer time can be accomplished when utility grid fails, and (iii) it is possible to obtain a high input power factor [1], [2].

Nowadays, conventional transformer-based double-conversion UPSs are being replaced by transformerless counterparts for some low-power applications [3]. Although transformerless UPSs do not have galvanic isolation between power supply and load, the elimination of the isolation transformer results in a compact, efficient and cost-effective solution for some loads. Among several transformerless topologies, the double-conversion UPS presented in Fig. 1 has attracted attention for low-power levels [4]-[7]. This UPS is composed of a half-bridge rectifier, a step-down/step-up bidirectional converter for battery bank charge/discharge and a half-bridge inverter. This configuration has a common input-output neutral line and a small number of switches, but the semiconductors are submitted to high voltage levels.

In addition to these features, the input half-bridge converter can operate as a preregulator converter. Thus, the rectifier control system must maintain the input current sinusoidal at near unity power factor, to regulate the total dc bus voltage at the desired reference value and to maintain the voltages across the dc bus capacitors balanced. These specifications can be achieved by using a fast inner current loop and slow outer voltage loops [8], [9]. The bandwidth of the voltage loops is limited to frequencies significantly lower than the voltage ripple frequency to synthesize a low-THD input current and, therefore, to maintain near unity input power factor. Nevertheless, this bandwidth limitation affects the output dynamic response.

Several papers have been published in an attempt to improve the output dynamic response of power factor correction rectifiers [10]-[15]. A well-known technique applied to the boost converter is based on sampling the output voltage at twice the line frequency, filtering this

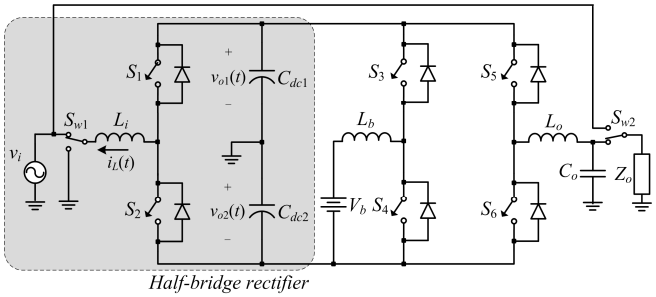

Fig. 1. Single-phase transformerless double-conversion UPS.

harmonic component from the measured output voltage [10]. However, the voltages across the dc bus capacitors of the half-bridge rectifier have voltage ripple at line frequency and its multiples when a single-phase inverter feeding a nonlinear load is connected to the dc bus. Then, it would be necessary to sample the voltages at the line frequency, limiting the bandwidth of the voltage loops. Other alternatives are based on the use of notch filters to minimize the sensed voltage ripple at the desired frequencies and to reduce the distortion in the reference current even with increased voltage-loop bandwidth [11], [12]. However, it would be necessary to include one notch filter for each frequency, increasing significantly the complexity of the voltage control loops.

Therefore, this paper proposes a new digital control system for the single-phase half-bridge rectifier, which results in fast output dynamic response. The current loop operates with high sampling frequency, whereas the voltage loops operate with reduced sampling frequency and moving average filters to eliminate the ripple at the output of the voltage compensators. With this, one can increase the voltage loop bandwidths, without affecting the input power factor.

This paper is organized as follows: Section II describes the proposed digital control system. Section III shows the dynamic models required to design the digital control system and Section IV presents the design methodology of the controllers. Section V shows some simulation results and Section VI includes some experimental results.

II. Proposed Control System of the Half-Bridge Rectifier

Fig. 2 shows a simplified block diagram of the proposed digital control system for the half-bridge rectifier. This system is composed of an inner current loop and two outer voltage loops to achieve a near unity input power factor and to regulate the voltages across the dc bus capacitors.

The inner current loop controls the switches so that the input current waveform is proportional to the line voltage and near unity input power factor is achieved. The input current $i_L(t)$ is sampled once at each switching period $T_{s1} = 1/f_{s1}$ and the current sensor is modeled as a gain h_i. The reference signal of the inner current loop $i_L^*(t)$ is composed of two components, which are produced by the outer voltage loops.

One voltage loop regulates the total dc bus voltage $v_o(t) = v_{o1}(t) + v_{o2}(t)$ to the desired reference voltage $v_o^*(t)$. Usually, the bandwidth of this voltage loop is significantly lower than the line frequency (usually smaller than 10 Hz), due to the voltage ripple in the dc bus capacitors [8], [9]. Therefore, to increase the bandwidth of this voltage loop, this paper proposes the connection of a moving average filter $C_f(z)$ [16] at the output of the total voltage compensator $C_v(z)$ to reject the measured voltage ripple in the dc bus capacitors, which present frequency components that are integer multiples of the fundamental frequency when an output inverter feeding a nonlinear load is connected to the dc bus. Moreover, the total dc bus voltage is sampled at a higher sampling period $T_{s2} = 1/f_{s2}$ to reduce the number of samples required to implement the digital moving average filter. The output of the moving average filter is multiplied by a sample of the input line voltage $v_{in}(t)$ to obtain a sinusoidal reference signal for the inner current loop. The input line voltage $v_{in}(t)$ is sampled at T_{s1} so that the current reference $i_L^*(t)$ is updated once at each switching period.

The other voltage loop must maintain the voltages across the dc bus capacitors balanced, that is, the differential voltage between the dc bus capacitors, defined as $v_d(t) = v_{o2}(t) - v_{o1}(t)$, must be equal to zero. This voltage loop injects a dc level to $i_L^*(t)$ to maintain the dc bus voltages balanced even with unbalanced loads connected to the dc bus capacitors. Similarly to the total dc bus voltage loop, a moving average filter $C_f(z)$ was included to this loop to improve the output dynamic response.

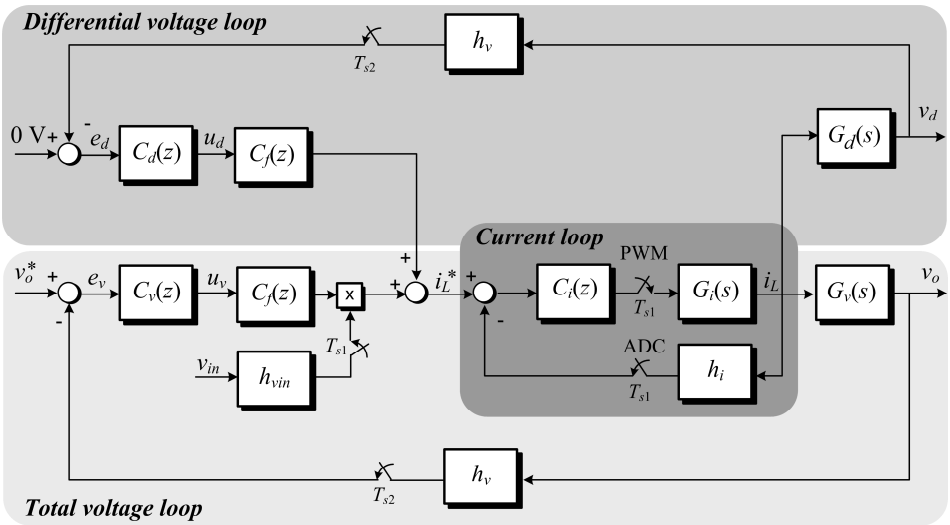

Fig. 2. Simplified block diagram of the proposed digital control system.

III. MODELING

This section presents some ac models of the single-phase half-bridge rectifier, which are required to design the digital control system shown in Fig. 2.

A. Duty-Ratio to Input Current Model

Firstly, it is necessary to obtain the duty-ratio to input current transfer function to design the current compensator.

It is well-known that the voltage loops are significantly slower than the current loop. Consequently, the dc bus capacitors and loads can be replaced by two dc voltage sources with amplitude equal to $V_o/2$, as shown in Fig. 3, to design the inner current loop.

Considering that $d(t)$ is the duty ratio of S_1, and using the small-ripple approximation to replace $i_L(t)$ and $v_i(t)$ with their average values over a switching period T_{s1}, $\langle i_L(t)\rangle$ and $\langle v_i(t)\rangle$ respectively, one can obtain the following averaged equation to describe how input current vary with time [17]:

$$L_i \frac{d\langle i_L(t)\rangle}{dt} = \langle v_i(t)\rangle + \frac{V_o}{2}\left[2d(t)-1\right] \tag{1}$$

To construct a small-signal ac model at a quiescent operating point, it is assumed that the input voltage $v_i(t)$ is constant over a switching period and small ac perturbations are imposed to the duty cycle $d(t)$, then a simplified duty-ratio to input current transfer function can be obtained:

$$G_i(s) = \frac{I_L(s)}{D(s)} = \frac{V_o}{L\,s} \tag{2}$$

B. Input Current to Total Output Voltage Model

Due to the inner current loop, the input voltage source connected in series with the input inductor was replaced by a current source, as illustrated in Fig. 4, to find the ac models required to design the outer voltage loops.

From Fig. 4 and considering that $C_{dc1} = C_{dc2} = C$ and $Z_{o1} = Z_{o2} = R$, one can obtain that the dc side current $i_o(t)$ to total output voltage $v_o(t)$ transfer function is given by:

$$\frac{V_o(s)}{I_o(s)} = \frac{2R}{RCs+1} \tag{3}$$

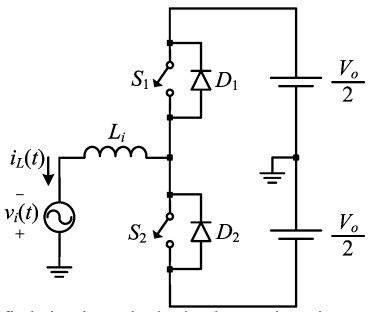

Fig. 3. Simplified circuit to obtain the duty-ratio to input current model.

The relation between $i_o(t)$ and $i_L(t)$ can be found through the power balance of the converter, resulting in a model valid for low frequencies. At the nominal quiescent operating point and considering unity power factor, the average dc side current over an input voltage period is given by:

$$\langle i_o(t)\rangle = \frac{V_i\, i_{L,rms}(t)}{V_o} \tag{4}$$

where V_i is the rms value of the input voltage, which is considered constant, and $i_{L,rms}(t)$ is the rms value of the input current, which is variable according to the load.

In addition, the amplitude modulation depth is defined as:

$$m_a = \frac{\sqrt{2}\,V_i}{V_o} \tag{5}$$

then, it is possible to rewrite (4) as:

$$\langle i_o(t)\rangle = \frac{m_a}{\sqrt{2}} i_{L,rms}(t) \tag{6}$$

Consequently, the rms input current to total output voltage transfer function is:

$$G_v(s) = \frac{V_o(s)}{I_{L,rms}(s)} = \frac{\sqrt{2}m_a R}{RCs+1} \tag{7}$$

Finally, considering that the rms value of the input current was employed as the input variable of the transfer function (7), the multiplier of the control system shown in Fig. 2 can be modeled as a gain K_m, given by the rms value of the sampled input voltage.

C. Input Current to Differential Output Voltage Model

Considering again that $C_{dc1} = C_{dc2} = C$ and $Z_{o1} = Z_{o2} = R$, the average values of the voltages across C_{dc1} and C_{dc2} over a switching period can be computed, respectively, by:

$$\langle v_{o1}(t)\rangle = -d(t)\,Z\langle i_L(t)\rangle \tag{8}$$

$$\langle v_{o2}(t)\rangle = \left(1-d(t)\right)Z\langle i_L(t)\rangle \tag{9}$$

where Z is the impedance of the parallel RC branch.

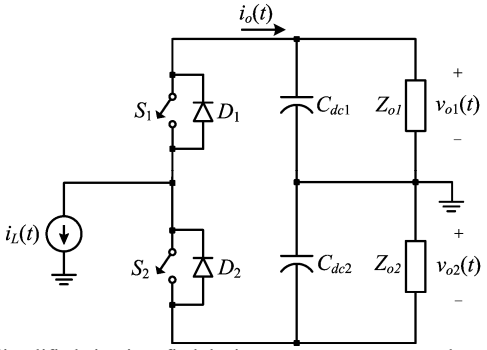

Fig. 4. Simplified circuit to find the input current to output voltage models.

Since $v_d(t) = v_{o2}(t) - v_{o1}(t)$, then:

$$\left\langle v_d\left(t\right)\right\rangle = Z\left\langle i_L\left(t\right)\right\rangle \tag{10}$$

Therefore, the input current to differential output voltage transfer function is given by:

$$G_d\left(s\right) = \frac{V_d\left(s\right)}{I_L\left(s\right)} = \frac{R}{RCs+1} \tag{11}$$

IV. Control System Design

This section presents a design example for the digital control system presented in Fig. 2, using the parameters given in Table I.

TABLE I
PARAMETERS OF THE SINGLE-PHASE HALF-BRIDGE RECTIFIER

P_o = 1 kW	Nominal output power
V_o = 420 V	Nominal dc bus voltage
V_i = 127 V_{rms}	Nominal input voltage
f_l = 60 Hz	Line frequency
f_s = 39.6 kHz	Switching frequency
f_{s1} = 39.6 kHz	Sampling frequency (current loop)
f_{s2} = 1.2 kHz	Sampling frequency (voltage loop)
$C_{dc1} = C_{dc2}$ = 2 mF	DC bus capacitances
L_i = 1 mH	Input converter inductance
h_i = 1/10	Current sensor gain
h_v = 2/165	DC bus voltage sensor gain
h_{vin} = 1/165	AC input voltage sensor gain
h_{AD} = 4096/3	A/D converter gain
K_{PWM} = 1/1894	PWM gain

A. Current Compensator

A block diagram of the digital system used to control the input current can be seen in Fig. 2, where $C_i(z)$ is a digital proportional-integral (PI) compensator with an additional high-frequency pole.

The pulse-width modulator can be approximated by a zero-order hold (ZOH) because the switching frequency is much higher than the reference signal frequency [18]. Therefore, the discrete-time transfer function of $G_i(s)$ is given by:

$$G_i\left(z\right) = Z\left\{\left(\frac{1-e^{-sT_s}}{s}\right)G_i\left(s\right)\right\} \tag{12}$$

The design of the digital PI controller was based on the frequency response method using the w-plane methodology [18]. Consequently, it is necessary to obtain the open-loop transfer function $T_i(w)$ in w-domain. For the system shown in Fig. 2, this transfer function is given by:

$$T_i\left(w\right) = C_i\left(w\right)K_{PWM}\,G_i\left(w\right)h_i\,h_{AD} \tag{13}$$

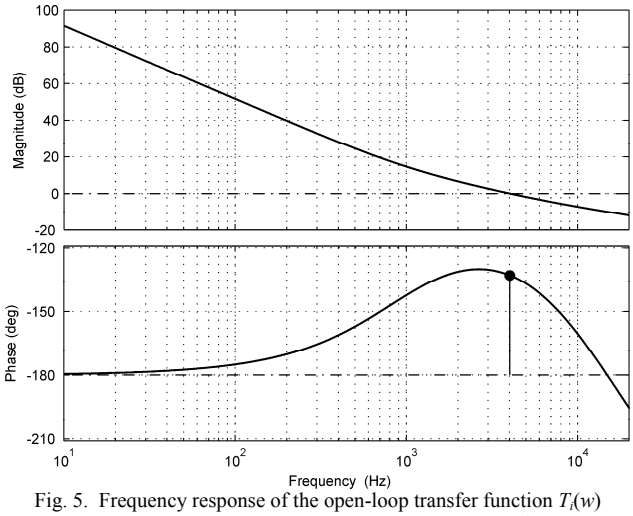

Fig. 5. Frequency response of the open-loop transfer function $T_i(w)$ (gain crossover frequency: 4 kHz; phase margin: 47°).

where:

$$z = \frac{1+\frac{T_s}{2}w}{1-\frac{T_s}{2}w} \tag{14}$$

The w-domain transfer function of the PI controller with an additional high-frequency pole is given by:

$$C_i\left(w\right) = k_i\,\frac{w+\omega_z}{w\left(w+\omega_p\right)} \tag{15}$$

where k_i, ω_z and ω_p are the parameters to be designed.

The specifications imposed to the inner current loop are a minimum phase margin equal to 45° and a minimum gain crossover frequency equal to 4 kHz. As a result, the w-domain transfer function of the current compensator is:

$$C_i\left(w\right) = 9.885\times10^4\,\frac{w+6283}{w\left(w+1.255\times10^5\right)} \tag{16}$$

and the resulting discrete transfer function $C_i(z)$ is derived by using the w-plane to z-plane transform (14):

$$C_i\left(z\right) = \frac{0.5185z^2+0.07538z-0.4431}{z^2-0.7774z-0.2226} \tag{17}$$

Fig. 5 presents the frequency response of the open-loop transfer function $T_i(w)$ with the compensator presented in (16).

B. Moving Average Filter

Depending on the load connected to the half-bridge rectifier, the dc capacitors can present voltage ripple with frequency components that are integer multiples of the fundamental frequency. Thus, as mentioned before, the bandwidth of voltage control loops should be significantly lower than the line frequency to maintain low input current distortion.

An alternative to minimize this effect is to employ one notch filter for each harmonic frequency, increasing considerably the overall control system complexity. Another option is to use a digital moving average filter [15], which provides large attenuation for every harmonic order smaller than or equal to $M/2$, where M is the number of samples in a fundamental period.

The digital moving average filter can be represented by the following recursive equation:

$$y(k) = y(k-1) + \frac{1}{M}\left[x(k) - x(k-M)\right] \tag{18}$$

where $x(k)$ and $y(k)$ are the input and output signals, respectively, of the digital moving average filter.

Thus, the transfer function of the digital moving average filter is given by:

$$C_f(z) = \frac{Y(z)}{X(z)} = \frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}} \tag{19}$$

The design of the digital moving average filter is extremely simple, because it is only necessary to define the number of samples M. The number of filtered harmonics depends directly on the value of M. Nevertheless, one can verify from (18) that the implementation of the moving average filter requires an M-word vector to store the last M samples. Therefore, the voltages across the dc bus capacitors were sampled at 1.2 kHz, so that the harmonic components with order smaller than or equal to 10 were filtered out with only two summations, one multiplication and one 20-word vector. Higher order harmonics could also be filtered out by increasing the number of samples, but the amplitudes of these harmonics on the dc bus voltages are not significant.

C. Total Voltage Compensator

A block diagram of the digital control system used to regulate the output voltage is shown in Fig. 2, where $C_v(z)$ is a digital PID controller to compensate the phase delay introduced by the moving average filter.

It is assumed that the input current is constant over a switching period to derive $G_v(z)$, then:

$$G_v(z) = Z\left\{\left(\frac{1-e^{-sT_s}}{s}\right)G_v(s)\right\} \tag{20}$$

Moreover, the inner current loop was replaced by the gain $1/(h_i h_{AD})$ to design the voltage loops. This simplification is valid, because the voltage loops are significantly slower than the current loop and the open-loop transfer function T_i is large in magnitude for low frequencies [17].

Therefore, the w-domain open-loop transfer function $T_v(w)$, utilized to design the voltage controller, is given by:

$$T_v(w) = C_v(w)C_f(w)K_m\frac{1}{h_i}G_v(w)h_v \tag{21}$$

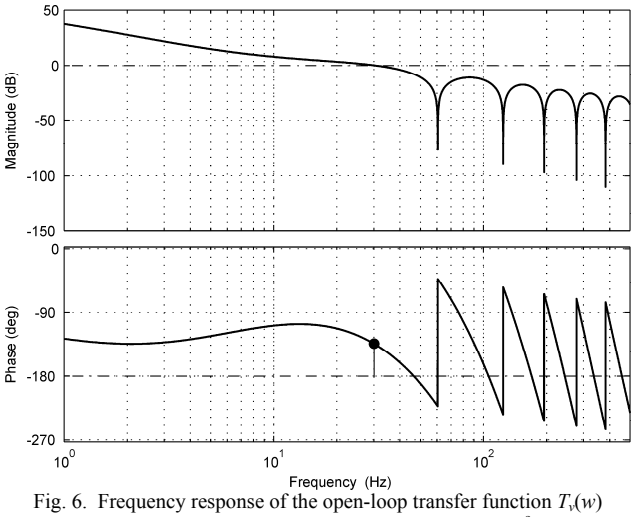

Fig. 6. Frequency response of the open-loop transfer function $T_v(w)$ (gain crossover frequency: 30 Hz; phase margin: 45°).

The specifications imposed to this voltage loop are a phase margin around 45° and a gain crossover frequency equal to 30 Hz. As a result, the w-domain transfer function of the total voltage compensator is:

$$C_v(w) = 0.0287\frac{(w+38.7)(w+67.6)}{w(w+730)} \tag{22}$$

Using (14), one can obtain the discrete transfer function of the total voltage compensator:

$$C_v(z) = \frac{0.023z^2 - 0.044z + 0.02105}{z^2 - 1.5335z + 0.5335} \tag{23}$$

Fig. 6 presents the frequency response of the open-loop transfer function $T_v(w)$ with the compensator presented in (22) and the moving average filter.

D. Differential Voltage Compensator

The differential voltage controller must ensure that the voltages across C_{dc1} and C_{dc2} remain balanced, that is, the differential voltage must be equal to zero even with unbalanced loading from dc bus capacitors.

The design of differential voltage controller is based on the open-loop transfer function $T_d(w)$, given by:

$$T_d(w) = C_d(w)C_f(w)\frac{1}{h_i}G_d(w)h_v \tag{24}$$

The specifications imposed to this voltage loop are a phase margin greater than 60° and a gain crossover frequency equal to 15 Hz. As a result, the transfer function of the differential voltage controller, which also is a PID controller, is:

$$C_d(w) = 5.6\frac{(w+31.4)(w+62.8)}{w(w+377)} \tag{25}$$

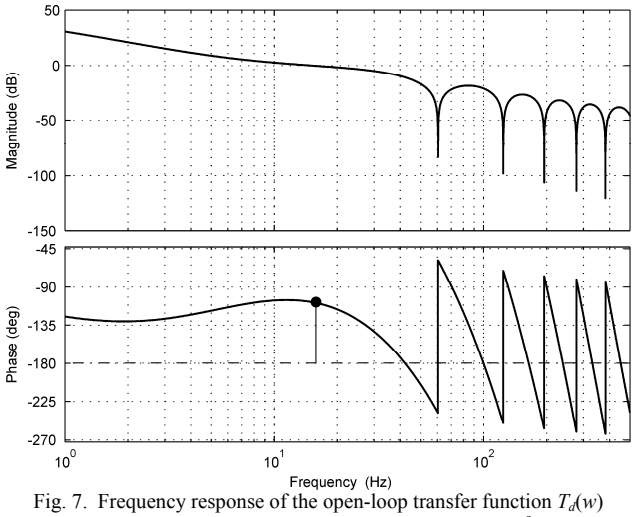

Fig. 7. Frequency response of the open-loop transfer function $T_d(w)$ (gain crossover frequency: 15 Hz; phase margin: 70°).

Thus, the discrete transfer function of the differential voltage compensator is:

$$C_d(z) = \frac{5.031z^2 - 9.676z + 4.651}{z^2 - 1.7285z + 0.7285} \tag{26}$$

Fig. 7 shows the frequency response of the open-loop transfer function $T_d(w)$ with the compensator presented in (25).

V. Simulation Results

This section presents some simulation results obtained with *SimPower Systems* toolbox of the Matlab/Simulink®, using the parameters presented in Table I and compensators designed in Section IV. The performance of the digital control system proposed for the half-bridge rectifier was initially evaluated by connecting a half-bridge inverter with LC-filter (L_o = 1 mH, C_o = 5 μF) to the dc bus, as shown in Fig. 1. Two distinct loads were connected to the inverter output: nominal resistive load and half-wave rectifier with crest factor equal to 3.

Fig. 8 shows the input voltage and current waveforms for nominal resistive load connected to the inverter output. The input current THD is equal to 0.3%, where the THD is calculated considering a harmonic order up to 100th. Fig. 9 presents the input current waveform (THD_i = 0.9%) when a half-wave rectifier is connected to the inverter output. One can clearly seen that the differential voltage loop injects a dc level to the input current to maintain the dc bus voltages balanced, as illustrated in Fig. 10, even with this severe unbalanced load. Moreover, the input current is nearly sinusoidal for both loads, even with gain crossover frequencies equal to 30 Hz and 15 Hz for the total and differential voltage loops, respectively.

On the other hand, resistive loads were connected directly to the dc bus capacitors to evaluate the output dynamic performance of the proposed digital control system. Fig. 11 presents the dc bus voltage waveforms under a sudden change

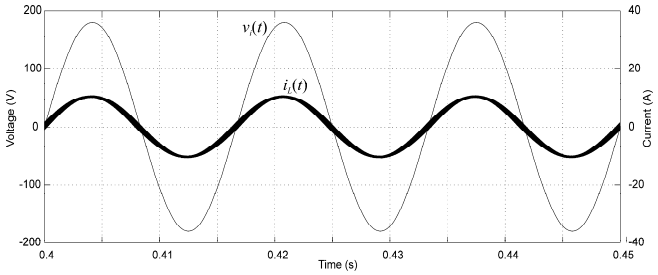

Fig. 8. Proposed digital control system: Input voltage and current waveforms for nominal resistive load connected to the inverter output.

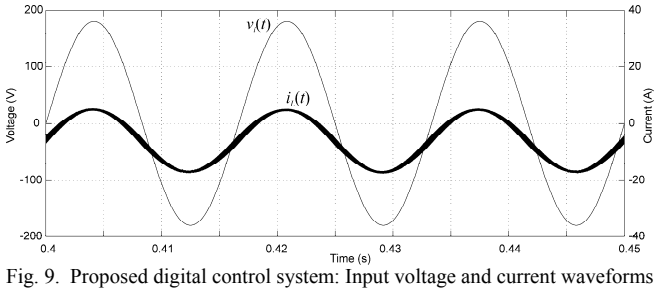

Fig. 9. Proposed digital control system: Input voltage and current waveforms for a half-wave rectifier connected to the inverter output.

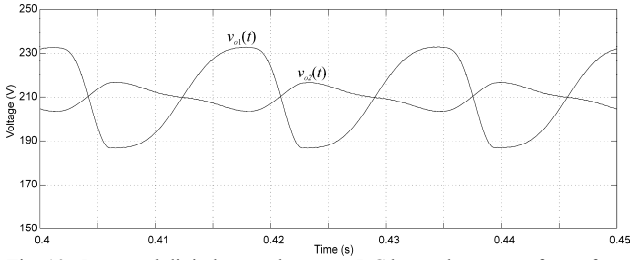

Fig. 10. Proposed digital control system: DC bus voltage waveforms for a half-wave rectifier connected to the inverter output.

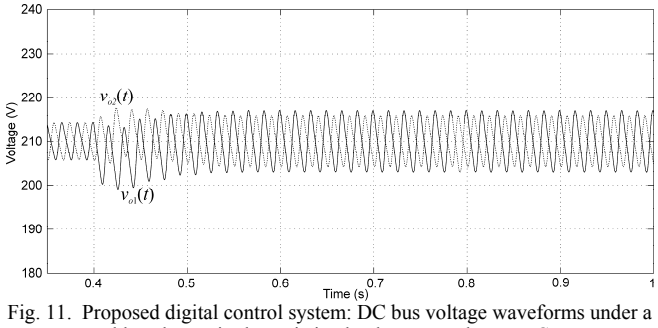

Fig. 11. Proposed digital control system: DC bus voltage waveforms under a sudden change in the resistive load connected across C_{dc1}.

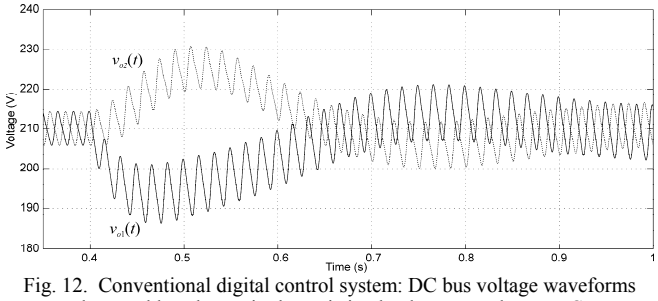

Fig. 12. Conventional digital control system: DC bus voltage waveforms under a sudden change in the resistive load connected across C_{dc1}.

(166 Ω to 88 Ω) in the resistive load connected across C_{dc1}. On the other hand, Fig. 12 shows the transient performance of a conventional digital control system under the same load change. The conventional control system has the same inner current loop, but the total and differential voltage loops do not have moving average filters and, consequently, the gain crossover frequencies were reduced to 6 Hz and 2 Hz, respectively, to maintain a low-THD input current. One can observe from these simulation results that the proposed digital control system has a faster output dynamic response.

VI. Experimental Results

A prototype of the single-phase half-bridge rectifier was built in the laboratory, using the same parameters given in Table I and compensators designed in Section IV.

The proposed digital control system was implemented in a DSP TMS320F2812 from Texas Instruments®. Fig. 13 shows the input voltage (THD_v = 2.6%) and current (THD_i = 3.1%) waveforms and Fig. 14 presents the voltage waveforms across the dc bus capacitors by connecting balanced resistive loads to the dc outputs. On the other hand, Fig. 15 presents the input voltage (THD_v = 2.0%) and current (THD_i = 2.8%) waveforms and Fig. 16 shows the voltage waveforms across the dc bus capacitors with unbalanced resistive loads connected to C_{dc1} and C_{dc2} (100 Ω and 300 Ω, respectively). One can observe that the proposed control system synthesizes a low-THD input current waveform and it maintains the voltages across the dc bus capacitors regulated and balanced by injecting a dc level to the input current.

Moreover, to evaluate the dynamic performance of the proposed control system, Fig. 17 shows the voltage waveforms across the dc bus capacitors under a sudden change (300 Ω to 100 Ω) in the resistive load connected to the top capacitor (C_{dc1}). On the other hand, Fig. 18 presents the dc bus voltage waveforms with the same load change, but using a conventional digital control system, with gain crossover frequencies of the total and differential voltage loops equal to 6 Hz and 2 Hz, respectively, and without including moving average filters to the voltage loops. One can observe from these results that the proposed digital control system has a significantly faster output dynamic response.

VII. Conclusions

The inclusion of digital moving average filters reduces the impact of the voltage ripple across the dc bus capacitors so that it is possible to increase the bandwidths of the outer voltage loops. Consequently, the proposed digital control system improves the output dynamic response of the single-phase half-bridge rectifier and maintains a low-THD input current waveform with distinct load conditions. The proposed control system is simple and it can be easily implemented in low-cost microprocessors, since the control algorithm is composed of simple recursive equations.

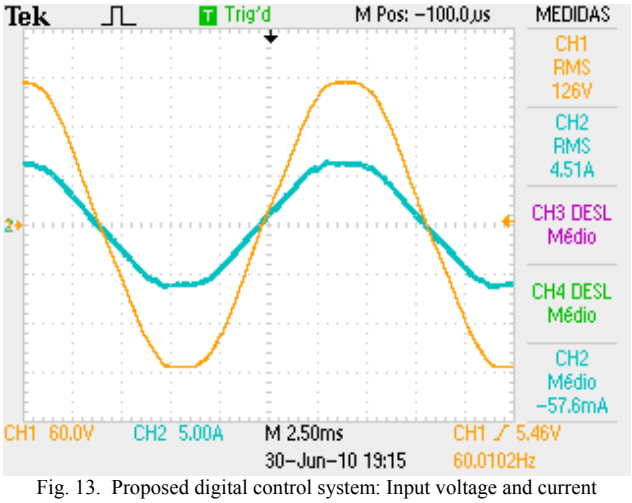

Fig. 13. Proposed digital control system: Input voltage and current waveforms for balanced resistive loads.

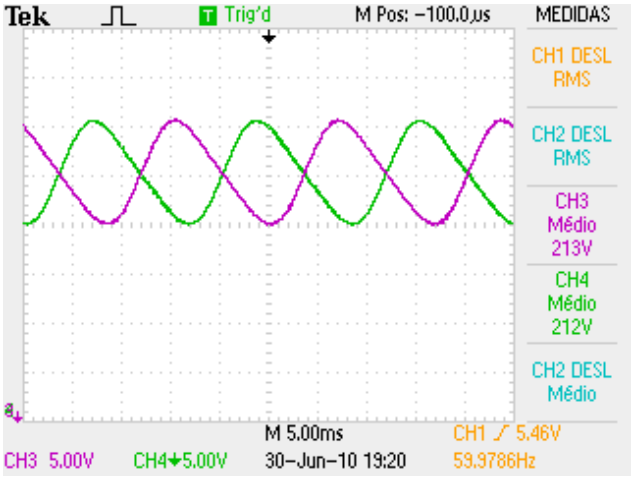

Fig. 14. Proposed digital control system: dc bus voltage waveforms for balanced resistive loads.

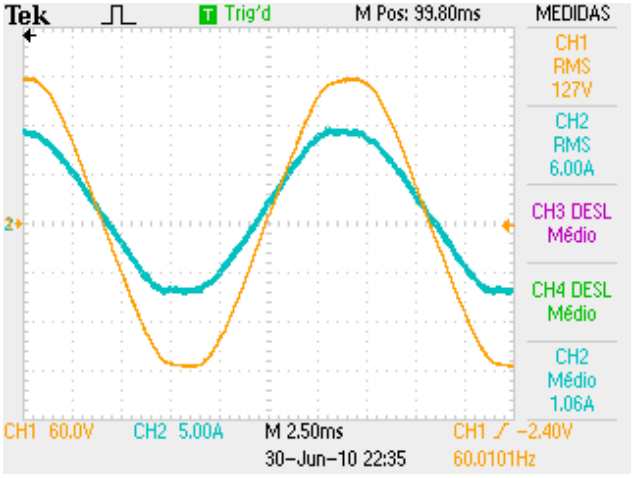

Fig. 15. Proposed digital control system: Input voltage and current waveforms for unbalanced resistive loads.

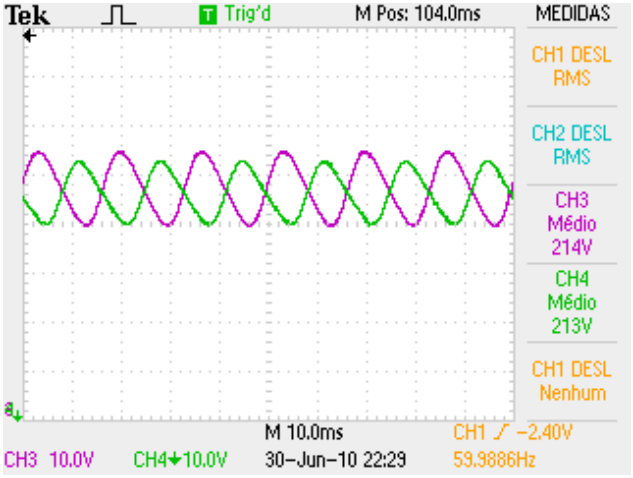

Fig. 16. Proposed digital control system: dc bus voltage waveforms for unbalanced resistive loads.

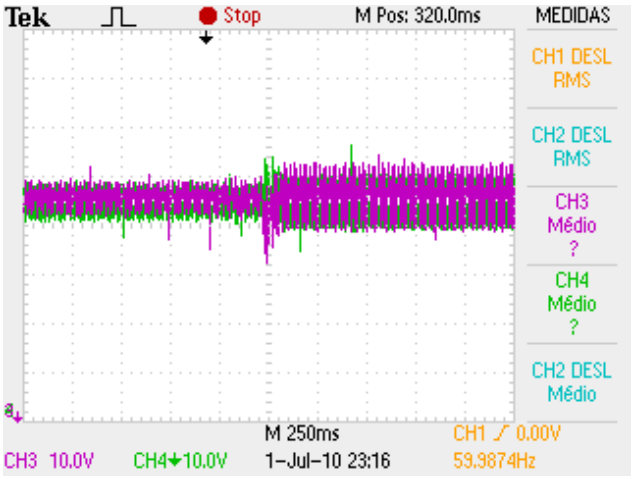

Fig. 17. Proposed digital control system: Voltage waveforms across the dc bus capacitors under a sudden change in the resistive load connected in C_{dc1}.

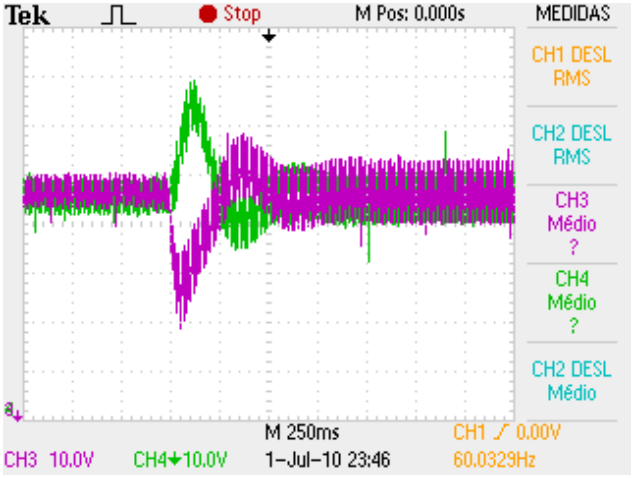

Fig. 18. Conventional digital control system: Voltage waveforms across the dc capacitors under a sudden change in the resistive load connected in C_{dc1}.

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