HYBRID MULTILEVEL CONVERTER EMPLOYING HALF-BRIDGE MODULES

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***Abstract* - A novel hybrid three-phase multilevel converter is proposed for medium-voltage applications. The converter employs a conventional three-phase voltage source inverter (VSI) linking series connected half-bridge modules at each phase. With the proposed connection, a large portion of energy can be processed by the VSI without the need for insulation or by employing a single transformer, while smaller power shares are processed within the half-bridge modules. Thus, the requirements for galvanically insulated dc sources are reduced. Modularity is naturally achieved. A modulation scheme for a four-level version is proposed and analyzed in detail. This scheme allows unidirectional power flow in all dc sources and, consequently enables diode bridges to be employed in the rectification input stage for unidirectional applications.**

***Keywords* - Multilevel converters, Hybrid converters, PWM modulation, Three-phase inverters.**

I. INTRODUCTION

Power electronics applications requiring medium voltage (MV) high power converters have been steadily growing in fields such as power quality, power systems control, adjustable speed drives (ASD), uninterruptible power supplies (UPS), equipment testing, co-generation and others. Most applications demand three-phase multilevel inverters. Various topologies have been proposed in the literature [1–10] in order to improve performance, adapt to requirements and avoid proprietary technologies.

Some topologies find more widespread use in industrial multilevel inverters. Among these are the neutral clamped converters (NPC), the capacitor clamped converter, the cascaded full-bridge converter, the hybrid VSI/NPC plus cascaded full-bridge converter and the active neutral clamped converter(ANPC).

The diode clamped converter, commonly named Neutral Point Clamped (NPC), [1,2] is a multilevel topology, which is widely employed in three-phase power conversion. There is a single dc-link that is split into two or more equal voltages which clamp the maximum voltage of the main switches through fast switching diodes. A high number of diodes is observed as the number of levels increase. Stabilization of the dc-link voltages is typically difficult and is achieved by posing limitations in the output voltages or loads [11].

The capacitor clamped converter, also know as Flying Capacitor converter [6], provides the clamping of the voltages across the switches through capacitors. The stabilization of the clamping voltages is achieved due to the higher number of switching possibilities. Even though the number of clamping diodes is reduced, the number of capacitors increases rapidly with the number of levels, increasing the number of isolated voltage sensors. Another difficulty is that the capacitors precharge process is complex.

Topologies which integrate some advantages of the NPC and FC converters are known as active neutral clamped converters (ANPC) [12–14]. These topologies present a single dc-link and the voltage clamping is achieved with the control of the dc-link and floating capacitors voltages. Thus, the single dc-link of the NPC and the flexibility for voltage stabilization of the FC are observed in these topologies. However, the number of active switches is increased or the voltage ratings of some of them must be higher. The capacitors precharge process is complex. The ANPC topologies are proprietary technologies [15, 16].

Cascaded Full-Bridge (CFB) converters [3, 4] employ dc-side isolated series connected full-bridge modules at each phase allowing high modularity and the lower total number of components when compared to NPC, ANPC or FC. These characteristics make them widely employed in industrial applications. As single-phase full-bridge modules are employed, the pulsating power in each dc-source presents a high low frequency ripple, increasing the storage effort. In addition, all modules and input rectifiers must process their share of the total power, increasing the demands for the rectifier stage transformers. Furthermore, the CFB is proprietary technology for many applications [1, 4, 17–19]. An alternative to the conventional cascaded full-bridge converter has been proposed in [20], where half-bridge modules are connected in a cascade instead of the full-bridge ones. This converter requires a higher number of insulated dc sources for the same number of levels of the CFB. However, lower power levels are processed in the dc sources.

Hybrid topologies employing three-phase VSI or NPC cascaded in each phase with series connected full-bridge modules (H3phCFB) have been proposed [5, 8, 21–23] as an alternative to the CFB. The number of components can be the same as for the CFB for the same number of voltage levels, while the three-phase converter can be directly fed without insulation. Thus, the requirements for the insulation transformers and for the main capacitive dc-link storage are lessened. Both, H3phCFB and CFB have their asymmetric versions [8, 24], presenting advantages and drawbacks depending on the specific applica-

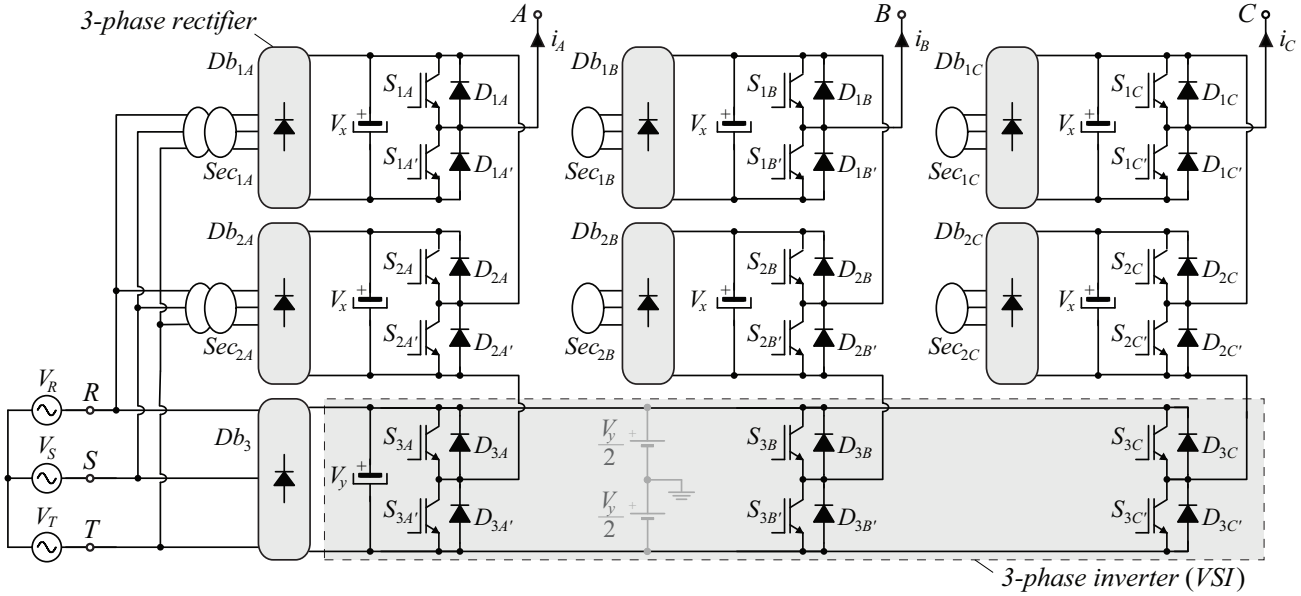

Fig. 1. Circuit schematic of the proposed hybrid multilevel converter employing half-bridge modules and a three-phase inverter. Further pairs of half-bridge modules can be connected in series at each phase-leg. The three-phase inverter can be replaced by other three-phase inverter topologies, for instance an NPC converter.

tion and available switch technology. Hybrid topologies are mainly proprietary technology as well [21, 23].

This work presents a novel hybrid topology (H3phCHB) that makes use of a three-phase inverter (shown as a VSI in Fig. 1), where each output is series connected to a pair, or multiple pairs (cascade), of half-bridge converters connected with inverse polarity as shown in Fig. 1. There, the special connection of the half-bridge modules [20] guarantees that no dc level is observed at the output voltages. As other hybrid topologies, the proposed converter allows the reduction of the demands for insulation and rectification processes. Even though the number of insulated sources is increased, for the same number of voltage levels as for the CFB or H3phCFB, the proposed converter lowers the ratings of these sources. Thus, higher power levels can be achieved for a given transformer/rectifier technology.

II. MULTILEVEL OPERATION

The following assumptions are made for the analysis: (*i*) the switching devices are ideal; (*ii*) the dc sources are constant positive voltages; (*iii*) parasitics are neglected; (*iv*) the virtual center point of the VSIs dc-link (drawn in gray in Fig. 1) is assumed as reference for the voltages. Considering a phase-leg composed of a pair of half-bridge modules and a leg of the VSI, the possible operation stages of the proposed converter are depicted in Fig. 2 for phase A positive values. It is observed that the output voltage v_A can assume six different values, which are given for v_o, with $o = A, B, C$, in Table I. These output voltage levels depend on the dc sources voltages V_x and V_y and on the states of switches S_{jo} and $S_{jo'}$, with $j = 1, 2, 3$. Based on these results, the H3phCHB can be operated with a number of levels N_{level} varying from four to six given that

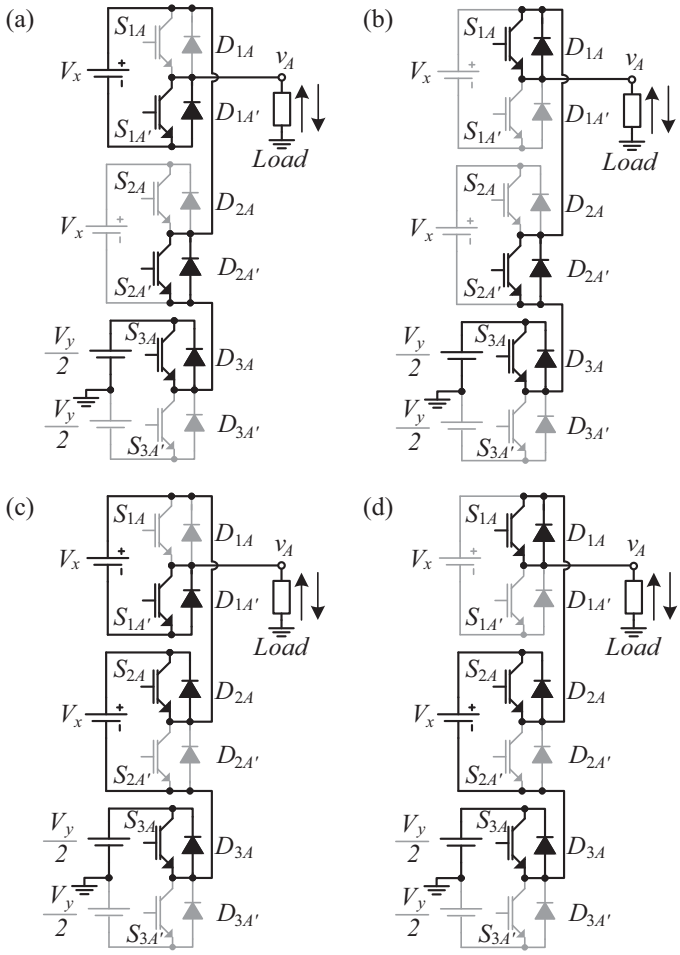

Fig. 2. Operation stages for a phase-leg of the proposed hybrid multilevel converter employing half-bridge modules for a positive output voltage.

TABLE I
Resulting output phase voltage (v_o, with $o = A, B, C$) as a function of the switching states and of the dc sources values V_x and V_y.

S_1	$S_{1'}$	S_2	$S_{2'}$	S_3	$S_{3'}$	v_o	Case 1 $V_x = V_y = V_{cc}$	Case 2 $V_x = V_y/2 = V_{cc}$	Case 3 $V_x = V_y/3 = V_{cc}$
0	1	0	1	0	1	$-V_x - \frac{V_y}{2}$	$\frac{-3V_{cc}}{2}$	$-2V_{cc}$	$\frac{-5V_{cc}}{2}$
1	0	0	1	0	1	$-\frac{V_y}{2}$	$\frac{-V_{cc}}{2}$	$-V_{cc}$	$\frac{-3V_{cc}}{2}$
0	1	1	0	0	1	$-\frac{V_y}{2}$	$\frac{-V_{cc}}{2}$	$-V_{cc}$	$\frac{-3V_{cc}}{2}$
1	0	1	0	0	1	$V_x - \frac{V_y}{2}$	$\frac{+V_{cc}}{2}$	0	$\frac{-V_{cc}}{2}$
0	1	0	1	1	0	$-V_x + \frac{V_y}{2}$	$\frac{-V_{cc}}{2}$	0	$\frac{+V_{cc}}{2}$
1	0	0	1	1	0	$+\frac{V_y}{2}$	$\frac{+V_{cc}}{2}$	$+V_{cc}$	$\frac{+3V_{cc}}{2}$
0	1	1	0	1	0	$+\frac{V_y}{2}$	$\frac{+V_{cc}}{2}$	$+V_{cc}$	$\frac{+3V_{cc}}{2}$
1	0	1	0	1	0	$+V_x + \frac{V_y}{2}$	$\frac{+3V_{cc}}{2}$	$+2V_{cc}$	$\frac{+5V_{cc}}{2}$

$$N_{level} = \begin{cases} 4 & \text{if } \mathrm{V_x = V_y} \\ 5 & \text{if } \mathrm{V_x = V_y/2} \\ 6 & \text{if } \mathrm{V_y \neq V_x \neq V_y/2} \end{cases} . \quad (1)$$

Based on the possible operation stages for a phase-leg, in the considerations given in Table I the available space vectors can be found as shown in Fig. 3(a) for a 4-level H3phCHB employing symmetric dc sources with $V_y = V_x$. The resulting state-space is a composition of the vectors generated by the VSI with the allowable combination of vectors generated by the half-bridge cascades. This is highlighted in Fig. 3(b) for the symmetric case where $V_y = V_x$ and in Fig. 3(c) for the asymmetric case where $V_y > V_x$. Within each half-bridge space it is not necessary to switch the VSI state in order to generate any voltage vector contained in it. It is seen in Fig. 3(c) that relatively increasing the dc voltage for the VSI expands the VSI space and creates a higher number of levels. However, the voltage ratings for the semiconductors is changed accordingly. The number of redundant switching states is also presented in Fig. 3(a) for the four-level converter. The presented number of redundant states is obtained by neglecting the states where one of the half-bridge modules exchange power within each other and assuming that the three-phase inverter switches at low frequency.

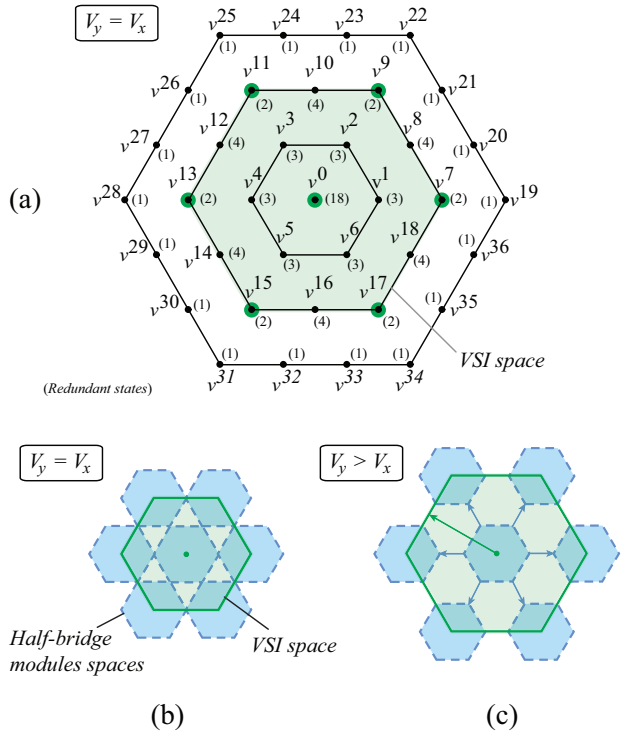

Fig. 3. Space vectors for the proposed converter: (a) space vectors for the 4-level converter employing $V_y = V_x$; (b) contributions for the modulation domain for $V_y = V_x$, and; (c) contributions for the modulation domain for $V_y > V_x$.

III. MODULATION SCHEME FOR THE 4-LEVEL CONVERTER

This section presents a modulation scheme for the four-level operation of the H3phCHB where the switches of the three-phase VSI switch at low frequency in order to reduce its switching losses. The half-bridge modules are switched at high frequency. Switches S_{jo} and $S_{jo'}$, with $o = A, B, C$ and $j = 1, 2, 3$, are switched in a complementary way. The first modulation pattern, named *HM*, for the half-bridge modules is obtained from sinusoidal modulating signals Ref_X compared to three synchronized triangular carriers Car_j as shown in Fig. 4(a) for a generic phase X, with $X = A, B, C$. The VSI switches are driven by the direct comparison of the modulating signals Ref_X to zero. The logic employed to generate the modulation pattern is presented in Fig. 4(b). For the four-level converter, the modulation index is defined as $M = 2V_p/(3V_{cc})$, where V_p is the peak value of the sinusoidal PWM generated output phase voltages.

Focusing in unidirectional applications, it is desirable that all dc sources supply an unidirectional power flow, so that uncontrolled rectifiers can be employed. Table II shows that some switching states cause positive or negative power flow at some of the insulated dc sources depending on the direction of the phase currents. Thus, it is not possible to control the power flow at all dc sources

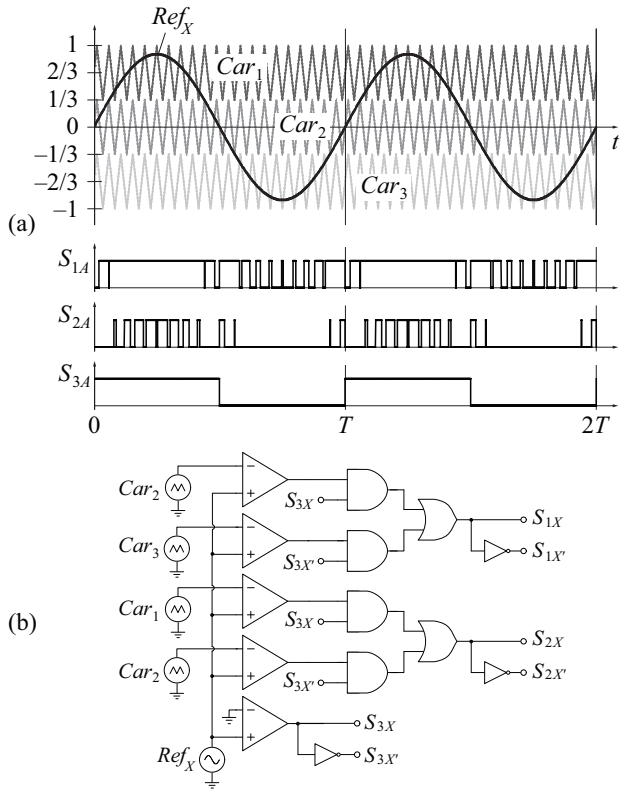

Fig. 4. Modulation strategy *HM*: (a) timing diagram for the 4-level operation, and; (b) PWM generation logic.

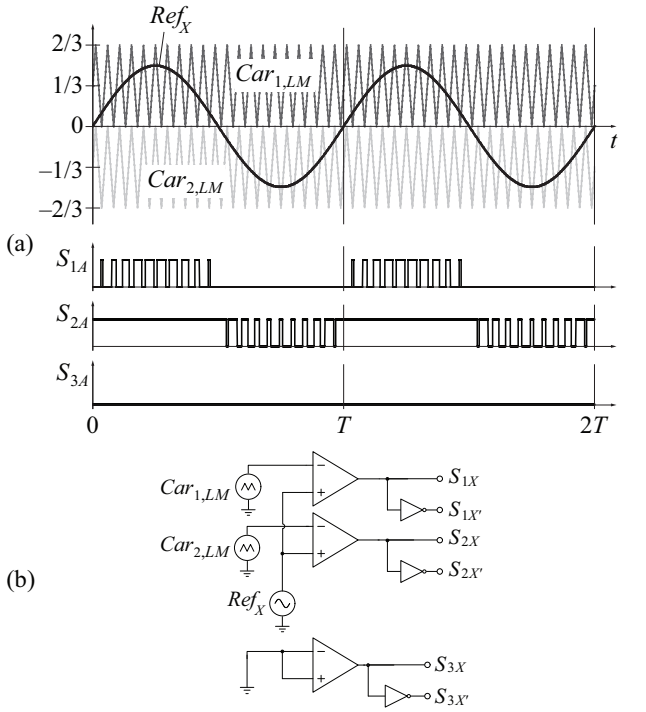

Fig. 5. Modulation strategy *LM*: (a) timing diagram for the 3-level operation, and; (b) PWM generation logic.

only by choosing proper switching states. The modulation pattern previously described is not able to guarantee unidirectional power flow in the dc sources for the half-bridge modules for a modulation index ranging from null to unity. The output voltages of the VSI are kept constant during each half period and this forces the half-bridge modules to process more power and regenerate it to the source for low modulation indexes. This is clearly observed in Fig. 6(a), where the power flow at an insulated dc source V_x becomes negative for $M < 0.42$ and the active power handled by all dc sources is extremely high at low modulation indexes when compared to the total active power transferred to the load. This characteristics prevents the employment of modulation *HM* for the entire modulation index range.

One way to avoid the regenerative power flow in the insulated dc sources is to switch the three-phase VSI at high frequency, generating output PWM voltages with a sinusoidal behavior proportional to the modulation index.

TABLE II

Output phase voltage (v_o, with $o = A, B, C$) and power direction at the dc sources (V_x and V_y) as a function of switching states. The power direction is given for $i_o < 0$ / $i_o > 0$ respectively.

S_1	$S_{1'}$	S_2	$S_{2'}$	S_3	$S_{3'}$	v_o	P_{x1}	P_{x2}
0	1	0	1	0	1	$\frac{-3V_{cc}}{2}$	+/−	Ø
1	0	0	1	0	1	$\frac{-V_{cc}}{2}$	Ø	Ø
0	1	1	0	0	1	$\frac{-V_{cc}}{2}$	+/−	−/+
1	0	1	0	0	1	$\frac{+V_{cc}}{2}$	Ø	−/+
0	1	0	1	1	0	$\frac{-V_{cc}}{2}$	+/−	Ø
1	0	0	1	1	0	$\frac{+V_{cc}}{2}$	Ø	Ø
0	1	1	0	1	0	$\frac{+V_{cc}}{2}$	+/−	−/+
1	0	1	0	1	0	$\frac{+3V_{cc}}{2}$	Ø	−/+

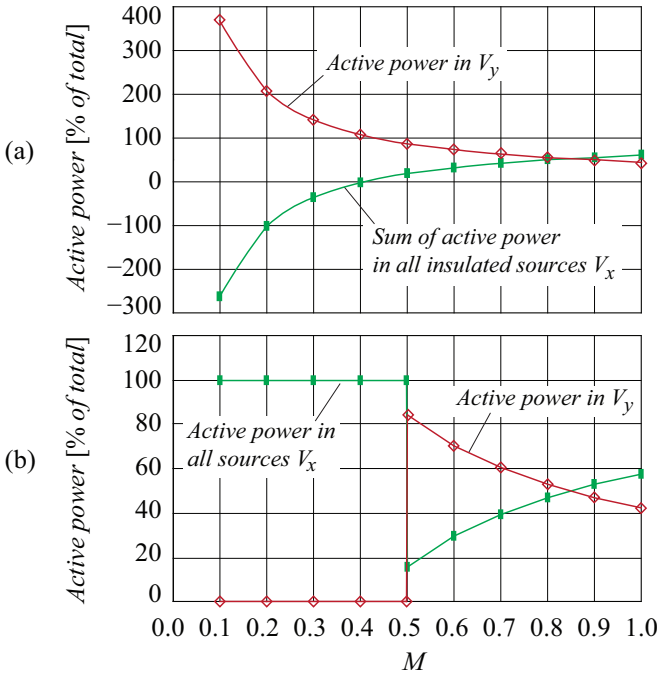

Fig. 6. Active power handled by the dc sources as a percent of the total load power for: (a) the modulation pattern *HM*, and; (b) the proposed modulation scheme employing *HM* for $M \geq 0.5$ and *LM* for $M < 0.5$.

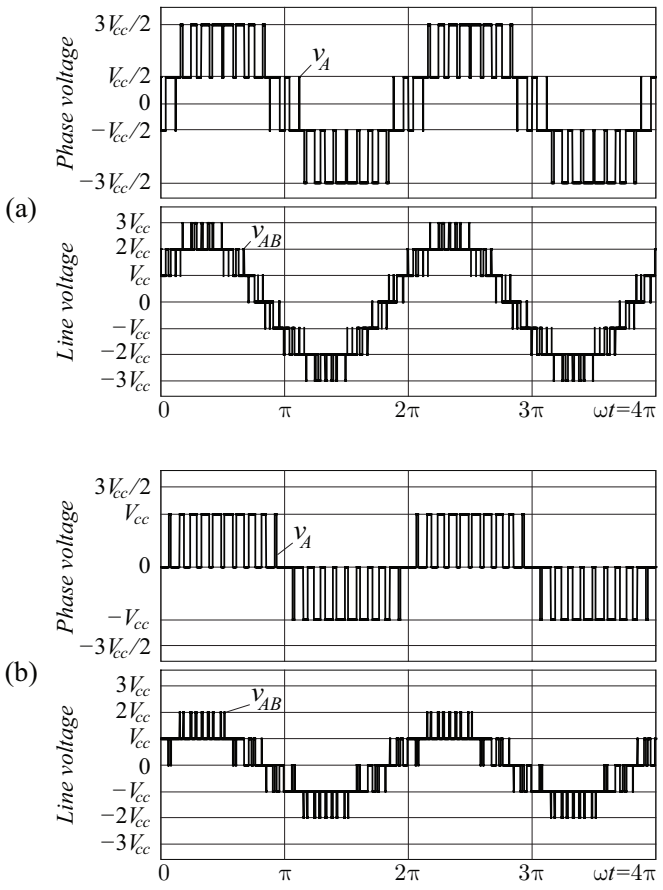

Fig. 7. Phase v_A and line-to-line voltage v_{AB} for: (a) *HM* modulation pattern for $M = 0.9$, and; (b) *LM* modulation pattern for $M = 0.5$.

Nevertheless, switching losses at the VSI would increase accordingly. Thus, a modification of the modulation logic is proposed. The VSI high side or low side switches are kept turned-on during the whole period whenever $M < 0.5$. The modulation pattern for $M < 0.5$ is presented in Fig. 5 and is named modulation *LM*.

The modulation scheme basic algorithm is as follows:

- $\mathbf{0 \leq M \leq 0.5}$ (*LM*): the VSI has all switches either clamped to the positive or the negative rail. The clamping can be changed at every modulation cycle in order to balance the losses at all semiconductors. The half-bridge modules process all the active power transferred to the load.
- $\mathbf{M > 0.5}$ (*HM*): each VSI leg switches a single time per modulation period (cf. Fig. 4) and the half-bridge modules handle a smaller power share (cf. Fig. 6(b)).

This modulation scheme is able to generate three-phase sinusoidal PWM modulated voltages under any modulation index. It presents the advantage of processing larger power levels by the three-phase VSI, which does not require an insulated dc source and switches at low frequency. Furthermore, as seen in Fig. 6(b), it guarantees that active power levels equal or lower than the total load active power are processed within the multilevel subconverters. The phase and line voltages obtained from numeric simulation of the system employing the proposed

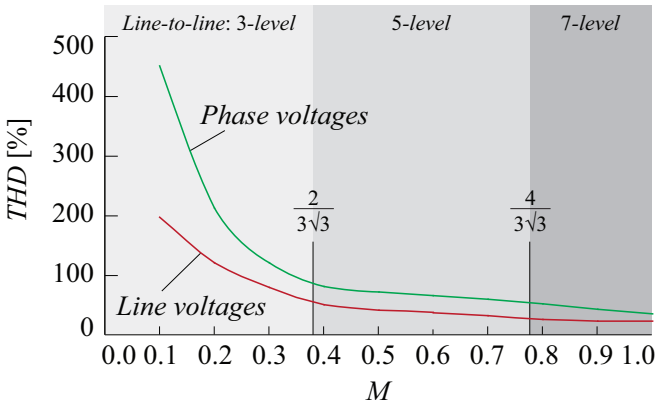

Fig. 8. Phase v_A and line-to-line voltage v_{AB} THD values obtained through simulations. The ratio from the switching frequency f_s to the output voltage reference f_{v_o} is set to 21 to 1, for instance, if $f_{v_o} = 50$ Hz then $f_s = 1,050$ Hz.

modulation index are shown in Fig. 7, exemplarily for phase A and lines A and B. In Fig. 8 it is observed that, both, phase and line voltages present lower total harmonic distortion for $M > 4/(3\sqrt{3})$ due to the line-to-line seven-level operation. Further decreasing the modulation index causes the converter to enter a five-level operation range until $M = 2/(3\sqrt{3})$ where three-level operation is observed and the THD values rapidly increase.

Observing the curves shown in Fig. 6 and Fig. 8, both modulation patterns are able to produce line-to-line voltages with 5-level while all dc sources supply positive active power for the range $0.42 < M < 2/3$. Thus, the modulation change can take place for any modulation index inside this range. Thus, a hysteresis can be programmed in order to avoid oscillations when switching from one modulation pattern to another. For instance, when modulation index is to be reduced, the pattern change takes

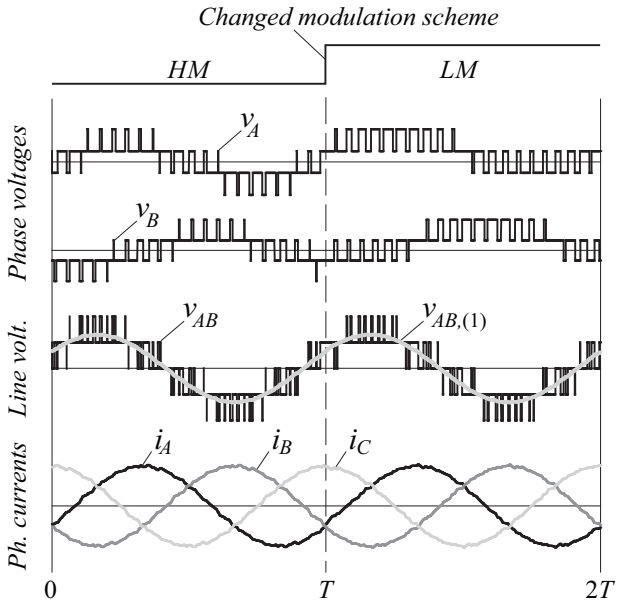

Fig. 9. Waveforms for $M = 0.5$ during a change from *HM* to *LM* modulation: phase voltages v_A and v_B, line-to-line voltage v_{AB} and its fundamental component, and phase currents i_A, i_B and i_C.

place for $M = 0.45$, while it happens for $M = 0.55$ when M increases. In order to verify modulation pattern transition, Fig. 9 shows simulation results for voltages and currents during a modulation change from HM to LM at a modulation index $M = 0.5$. It is observed that the modulation pattern change is smooth and does not cause any oscillation at, both, line voltages and phase currents.

IV. EXPERIMENTAL VERIFICATION

Experimental verification is carried out in a small scale IGBT based prototype that implements a symmetrical four-level ($V_x = V_y$) converter as drawn in Fig. 1. The prototype presents all dc sources with galvanic insulation through three-phase transformers, which are fed by the mains with a three-phase auto-transformer in order to achieve control of the input voltages. Three-phase diode bridges rectify the voltages in the secondary side of the transformers and electrolytic capacitors smooth the rectified voltages in order to achieve low ripple dc voltages in all dc sources with an average value of approximately 400 V. Total of nine IGBT half-bridge modules implement the four-level converter. The employed IGBTs are manufactured by Semikron in half-bridge modules (SKM75GB063D) rated for 600 V and 75 A. The switching frequency for the half-bridge converters is set to 4.08 kHz, while the output fundamental voltage is 60

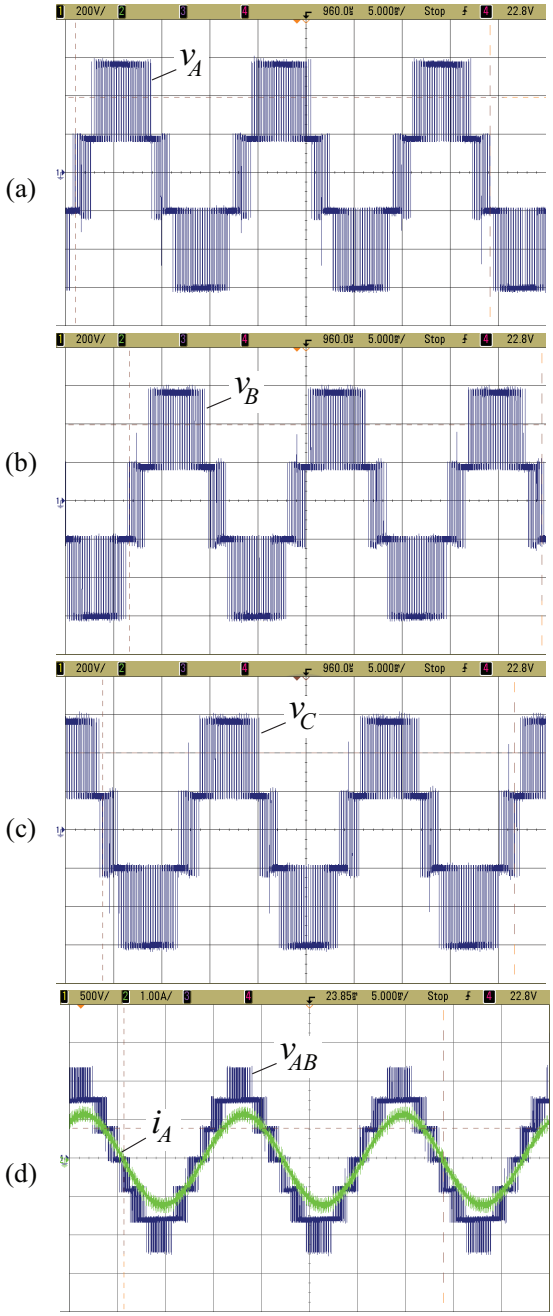

Fig. 10. Experimental results for $M = 0.9$, $f_{vo} \cong 60Hz$ and $f_s \cong 4kHz$ — HM modulation: (a) phase voltage at phase A; (b) phase voltage at phase B; (C) phase voltage at phase C, and; (d) line voltage v_{AB} and phase current i_A.

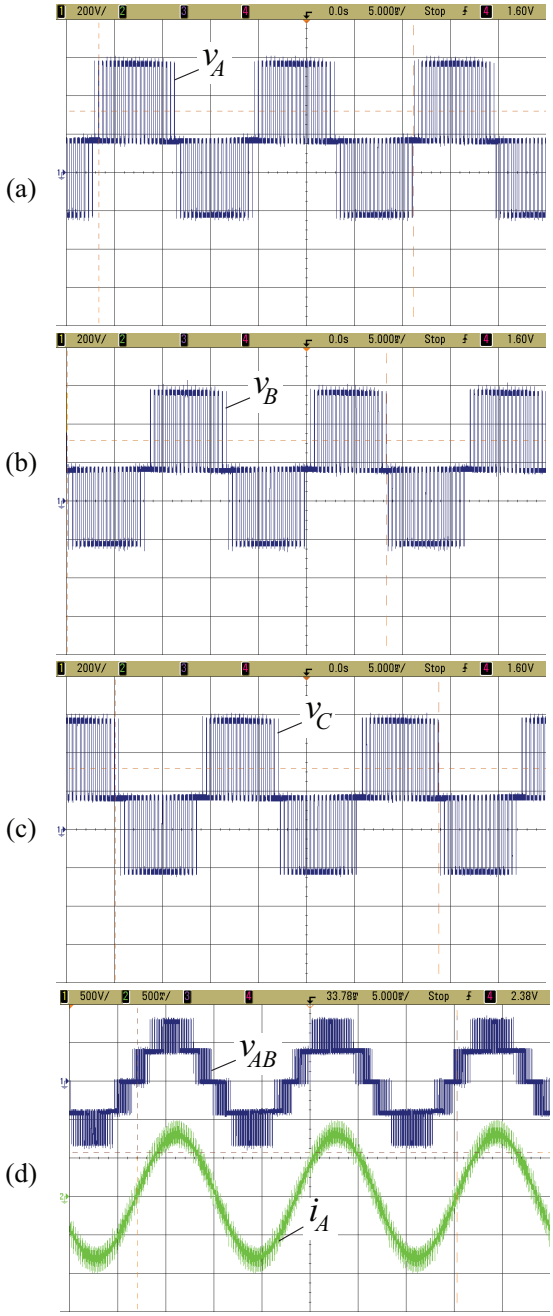

Fig. 11. Experimental results for $M = 0.5$, $f_{vo} \cong 60Hz$ and $f_s \cong 4kHz$ — LM modulation: (a) phase voltage at phase A; (b) phase voltage at phase B; (C) phase voltage at phase C, and; (d) line voltage v_{AB} and phase current i_A.

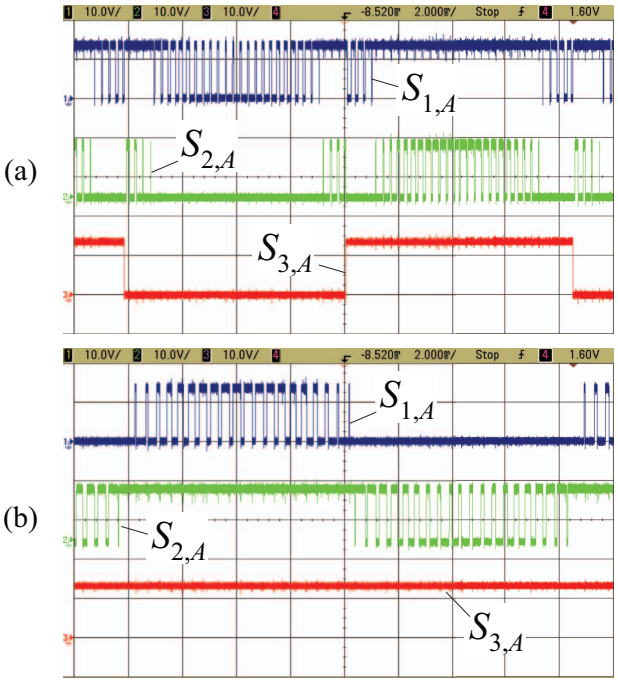

Fig. 12. Implemented gate signal patterns for (a) *HM* modulation ($f_s = 3.6$ kHz), and; (b) *LM* modulation ($f_s = 2.4$ kHz). The switches $S_{jA'}$ are driven by complementary signals with a dead-time of 4 μs.

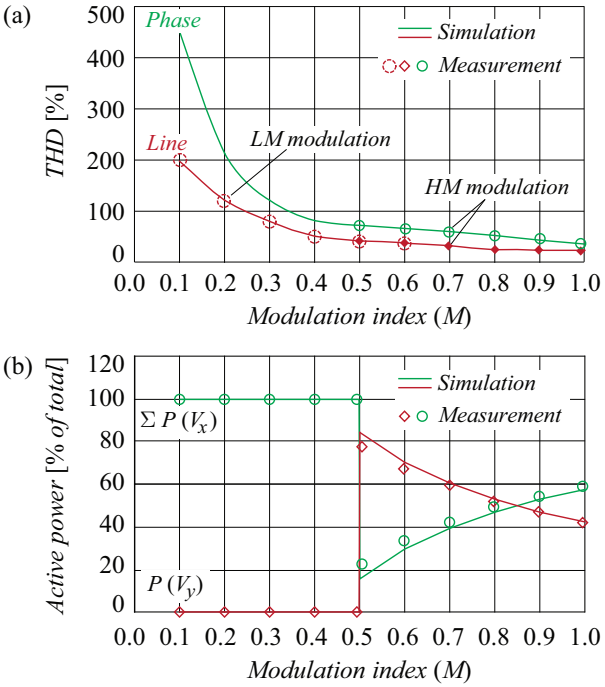

Fig. 13. Measured and simulated (a) THD for line and phase voltages according to the modulation index M, and; (b) active power for the VSI dc source $P(V_y)$ and for the sum of the sources for the half-bridge modules $\sum P(V_x)$. The THD values are computed considering harmonics from 2 to 1000.

Hz. The hardware has been built to offer safe operation margins and flexibility and, thus, is not optimized for specific operation points. The employed RL load presents $R = 740\ \Omega$ and $L = 111$ mH connected in delta, leading to a current displacement angle around 4°@60 Hz.

The practical implementation of both modulation patterns, *LM* and *HM*, is performed in a DSP, model TMS320F2812, where the gate signals are generated in an open-loop scheme. The modulation employs the DSP's event manager (EVA and EVB) and a few I/O pins. The high frequency PWM pulses are produced by the DSP's PWM modules, while the low frequency signals are software generated by comparing the modulating signals to zero. The sinusoidal references are internally computed through a routine that calculates 60 Hz sinusoidal signals displaced by 120°. A zero crossing detector is virtually implemented in order to compare the polarity of the sinusoidal references. Depending on the instantaneous value of the modulating function an algorithm adapts the function levels to the DSP's PWM modulator. The modulation patterns generated by the implemented logic are observed in Fig. 12 for a switching frequency of 3.6 kHz for $M = 0.9$ and 2.4 kHz for $M = 0.5$.

Applying a modulation index $M = 0.9$ lead to the phase voltages, i.e. voltages between the load terminals A, B, C and the mid-point of the VSI's dc-link, as shown in Fig. 10. Fig. 10(a) presents voltage v_A, Fig. 10(b) shows v_B and v_C is seen in Fig. 10(c). It is observed that the phase voltages closely follow the simulated patterns and are displaced by $2\pi/3$ from each other. The measured line voltage v_{AB} is given in Fig. 10(d) together with line current i_{AB} (Δ-connected RL load). Once again the experimental waveforms verify the theoretical analysis demonstrating a seven-level line voltage that is able to supply phase currents with very low distortion.

Applying a modulation index $M = 0.5$ lead to the phase voltages depicted in Fig. 11. It is observed that the three-level phase voltages follow the theoretical *LM* modulation pattern with the dc offset ($\cong 200$ V) due to the measurement from the phase terminals to the center point of the VSI's dc-link. The line voltage v_{AB} is shown in Fig. 11(d) with the line current i_{AB}. The line voltage presents five-levels as expected driving a current with low harmonic distortion.

The modulation index has been varied from close to unity to close to null in order to verify the active power distribution between the insulated dc sources and to measure the THD of line and phase voltages. The *HM* modulation pattern was employed from $M = 1$ down to $M = 0.5$, while the *LM* was used for lower modulation index values. The measurement results are summarized in Fig. 13 along with the theoretical results reported in section III. Regarding voltage THDs, both, theoretical and experimental results are perfectly matched. Errors lower than 10% are observed at the power distribution curves, which do verify the simulation results and show the importance of the modulation scheme for this type of multilevel converter.

V. CONCLUSIONS

A novel hybrid multilevel converter able to achieve four, five or six level operation has been proposed. The main advantage for this solution is the possibility of reduction of the power ratings for insulated dc sources compared to the CFB and to other hybrid solutions such as the VSI

cascaded with full-bridge converters. It presents the same number of power semiconductors as the CFB and the H3phCFB, thus, the smallest possible for a given number of voltage levels. The operation principle of the converter has been clarified and the achievable space vector spaces presented. A four-level modulation scheme has been presented, which allows unidirectional power flow in all dc sources for any modulation index and lowers the power demand on the insulated dc sources for high modulation indexes. Furthermore, the modulation scheme is able to generate, both, phase and line voltages with low THD. The computation of the current efforts has been presented with emphasis on the semiconductors of the half-bridge modules that are asymmetrically loaded. Experimental results based on a built prototype have validated the performed analysis and shown the relevant operating characteristics of the proposed converter.

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