CAPACITOR VOLTAGE BALANCING IN A 5-L FULL-BRIDGE FLYING CAPACITOR INVERTER

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***Abstract* – An active control method to balance the flying capacitor's voltage is presented for a single-phase full-bridge flying capacitor inverter. Based on the equations of flying capacitors, an analytical method that represents the natural capacitor's voltage balancing is introduced. In this technique, the duty cycle of the switches is modified to control the voltage of the capacitors using a proportional integrative controller. This method considers the fact that current direction influences the capacitor's voltage balance. The controller generates small differences between the duty cycles of the switches, which change the charge process of the capacitors. Simulation and experimental implementation results show that the control is efficient, maintaining the capacitor's voltage regulated.**

***Keywords* – Active capacitor voltage balancing, flying capacitor multilevel inverter, phase-shifted pulse width modulation (PS-PWM).**

I. INTRODUCTION

In the last years, multilevel converters have emerged as a solution for higher voltage level and for higher power applications [1]. In such converters, the quality of the output voltage improves as the number of voltage levels increases, so the size of the output filters is decreased and the transformers can be eliminated. In this way, the use of multilevel inverters is also extended to low power applications, such as electrical vehicle propulsion systems, active power filters, photovoltaic systems and UPS devices [2-3].

The flying-capacitor (FC), one of multilevel topology, was proposed by Meynard [4] in 1992. The FC converter uses capacitors to perform voltage clamping, while the neutral-point-clamped (NPC) uses diodes instead. The advantages of the FC converter over the NPC inverter are a higher number of redundant states and the direct clamp-voltage across all switches, avoiding overvoltage in the internal semiconductors [5].

The voltage balancing of the fly capacitor is very important for the operation of the FC converter. When a voltage unbalance occurs, some devices may not function properly, compromising the converter's functionality. For this reason, the secure operation of power devices cannot be ensured.

Unbalanced voltage can be generated by many non-linearities and non-idealities, such as semiconductor voltage drops, finite rise and fall times, drivers' dead time, digital control delay time etc. If this unbalanced voltage is not controlled, the fly capacitor can be damaged. Different methods have been introduced in the literature to maintain voltage balancing. These methods can be divided into two groups: natural balance control or closed-loop control [6].

Recent researches show that natural balance control has been used in FC converters [7-8]. This is a simple control method because no voltage or current sensor is necessary. Most natural balance control techniques use the phase-shifted pulse-width modulation (PS-PWM), equally distributing the current through the semiconductors, maintaining voltage balance under ideal conditions. In practice, there are many non-idealities and non-linearities, which prevent these methods from yielding good results. Other negative factors, such as the difficulty in maintaining the voltage on capacitors at low modulation indexes and unbalanced three-phase systems, have rendered this control technique unattractive and not much discussed in the literature [6].

For these reasons it is preferable to use loop-control for flying capacitor's voltage balance. The closed-loop control techniques for capacitor voltage balance is divided into two categories. One consists of conventional active control techniques, which use classical controllers to adjust the duty cycles of the switches according to the reference signal of the controller. Another is the selectivity control techniques, where the flying capacitor's voltage is controlled by choosing one of the redundant switching states that will maintain the voltage on capacitors [9-11].

Some papers approach different techniques for conventional active control. The method presented in [12] is based on the implementation of a proportional controller using PS-PWM modulation, which can be applied to n-level FC converters. In this paper, the effects between the current of the capacitors and the duty cycle of the switches are measured and used to regulate the voltage on the capacitors

A modified PS-SPWM control has been proposed in [13]. In this paper, the active control to maintain the voltage on the capacitors is based in proportional integral (PI) controllers and a digital algorithm. The algorithm adjusts the time duration of the switching states, according to the unbalanced voltage level. In [14], the voltage balance of a three-level flying capacitor converter is controlled by a closed-loop control, which compensates the duty cycles of the switches in proportion to the unbalanced voltage error signal.

Another classic control strategy has been proposed in [6], for a four-level full-bridge multilevel FC converter. This technique uses a PI control to modify the modulation signal for each switch balancing the capacitor's voltage. This method does not consider the effect of the output current in the charge process of the flying capacitors, decreasing the efficiency of the controller.

Based on these studies, this article approaches a simple close-loop control using a PS-PWM modulation that is

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efficient and can be used in any n-level FC converter . The proportional integrative controller (PI) presented in this paper is used to modify the duty cycle of the switches, maintaining the voltage balance on the flying capacitors. The fact that the output current direction influences in the capacitor's voltage balance is not discussed in the international papers and this article introduces an analytical method that represents the natural capacitor's voltage balance for controller design, considering the output current direction. The proposed technique is applied to a single-phase 5-level full-bridge flying capacitor (FC-FC) that is shown in Figure 1.

II. BASICS OF OPERATION OF A FIVE-LEVEL FC-FC

Figure 1 presents the Five-level full-bridge flying capacitor inverter topology. The switches are activated by the comparison between the triangular carriers and the sinusoidal reference. The carriers have a high frequency and are shifted one to another by 90°. The reference signal has the same frequency that is desired in the output of the converter. Figure 2 presents the PS-PWM modulation for the FC-FC inverter.

Table I shows the switching states of a five-level FC-FC converter and the flying capacitor's charge condition. Where $C_x\uparrow$ represents that the capacitor is charging, $C_x\downarrow$ represents that the capacitor is discharging and i_o represents the output current. Notice that the capacitors' charge process is modified by the switching states and the direction of i_o.

The output voltage can be calculated from expression (1), where S_x (x = 1, 2, 3 or 4) is 1 if the switch state is on or 0 if the switch is off, and V_{CC} is the dc-link voltage. On ideal and steady state conditions, the voltage across the flying capacitor and the switches is V_{CC} /2.

$$V_o = V_{CC}(S_1 - S_3) + V_{C1}(S_2 - S_1) + V_{C2}(S_3 - S_4) \quad (1)$$

III. FC-FC 5-L MODELLING AND CONTROL

A. Analysis of Flying Capacitor's Voltage Balance

To control the capacitor's voltages, it is necessary to understand the process of charge and discharge of the flying capacitors. With these variables it is possible to control the unbalanced voltages on the FC converter.

It is known that the voltage variation on the capacitors depends on the average current through these devices. Therefore, to control the fly capacitor's voltage, it is necessary to study the instantaneous currents through the capacitors. Current in the capacitors is represented by:

$$i_{C1}(t) = i_{S1}(t) - i_{S2}(t) \quad (2)$$

$$i_{C2}(t) = i_{S3}(t) - i_{S4}(t) \quad (3)$$

The current through a flying capacitor is affected by the switch state of the two adjacent switches.

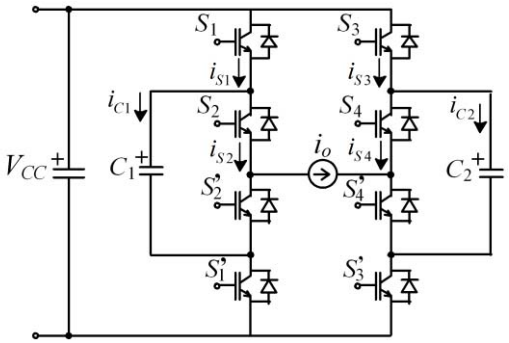

Fig. 1. Five-level full-bridge flying capacitor inverter topology.

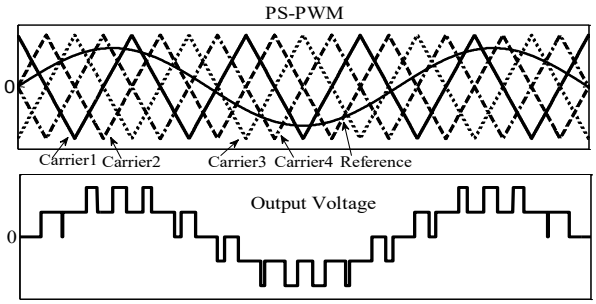

Fig. 2. PS-PWM modulation and the output voltage for a five-level FC-FC.

TABLE I
Switching states of a five-level FC-FC converter and the flying capacitor's charge condition.

Output Voltage	S_1	S_2	S_3	S_4	$i_o > 0$		$i_o < 0$	
V_{CC}	1	1	0	0	-	-	-	-
$V_{CC}/2$	1	1	1	0	-	$C_2\downarrow$	-	$C_2\uparrow$
$V_{CC}/2$	1	1	0	1	-	$C_2\uparrow$	-	$C_2\downarrow$
$V_{CC}/2$	1	0	0	0	$C_1\uparrow$	-	$C_1\downarrow$	-
$V_{CC}/2$	0	1	0	0	$C_1\downarrow$	-	$C_1\uparrow$	-
0	1	1	1	1	-	-	-	-
0	1	0	1	0	$C_1\uparrow$	$C_2\downarrow$	$C_1\downarrow$	$C_2\uparrow$
0	1	0	0	1	$C_1\uparrow$	$C_2\uparrow$	$C_1\downarrow$	$C_2\downarrow$
0	0	1	1	0	$C_1\downarrow$	$C_2\downarrow$	$C_1\uparrow$	$C_2\uparrow$
0	0	1	0	1	$C_1\downarrow$	$C_2\uparrow$	$C_1\uparrow$	$C_2\downarrow$
0	0	0	0	0	-	-	-	-
$-V_{CC}/2$	1	0	1	1	$C_1\uparrow$	-	$C_1\downarrow$	-
$-V_{CC}/2$	0	1	1	1	$C_1\downarrow$	-	$C_1\uparrow$	-
$-V_{CC}/2$	0	0	1	0	-	$C_2\downarrow$	-	$C_2\uparrow$
$-V_{CC}/2$	0	0	0	1	-	$C_2\uparrow$	-	$C_2\downarrow$
$-V_{CC}$	0	0	1	1	-	-	-	-

The current through the switches is calculated from equation (4)

$$i_{S_x}(t) = D_{Sx}(t)\, i_o(t) \quad (4)$$

where D_{Sx} (t) is the instantaneous duty cycle of the switch x and $i_o(t)$ is the output current. Replacing (4) in (2) and (3):

$$i_{C1}(t) = \left[D_{S1}(t) - D_{S2}(t)\right] i_o(t) \quad (5)$$

$$i_{C2}(t) = -\left[D_{S3}(t) - D_{S4}(t)\right] i_o(t) \quad (6)$$

These equations show that the current through capacitors C_1 and C_2 depends on the output current and the difference of duty cycle between the adjacent switches of each FC leg. In an ideal situation, the duty cycles of the switches are equal. Therefore, the average current through the flying capacitor is zero and the voltage is still balanced. Otherwise, the difference between the command signals of the switches (caused by non-idealities) results in an unbalance voltage on the capacitors, compromising the quality of the output voltage and the converter functionality.

This analysis shows that it is possible to control the voltage of the capacitors generating a small difference between the duty cycles of the switches, which can be used to control the voltage unbalances.

B. Voltage Balancing Method

To control the flying capacitor's voltages, adding a control signal to each switch duty cycle is proposed, according to (7). The command signals of switches S_1 and S_3 are formed from the duty cycle of switch D (generated by the PS-PWM) added to a control signal Δd_S. On adjacent switches S_2 and S_4, control Δd_S is subtracted from signal D, generating a small difference of $2.\Delta d_S$ between the duty cycles of the switches. The Δd_S becomes the control signal and the voltages on the capacitors are the variables to be controlled.

To complement this control technique, it is necessary to insert a k_S flag for the controller identifying the direction of the output current. This flag takes values 1 if $i_o > 0$ or -1 if $i_o < 0$. As previously mentioned, current i_o changes the charge process of the flying capacitors and this variable must be considered to improve the efficiency of the controller. Like so, it is necessary to multiply the logic k_S by the control signal. Figure 3 shows the full control diagram for the voltage balance of the FC-FC converter.

$$\begin{aligned} D_{S1,3}(t) &= D + \Delta d_S \\ D_{S2,4}(t) &= D - \Delta d_S \end{aligned} \tag{7}$$

.

C. Voltage Balance Modeling Equations

To implement the present control, it is necessary to know the analytical model, which can be derived replacing (7) in (5) and (6):

$$i_{C1}(t) = 2\ k_s\ \Delta d_S\ i_o(t) \tag{8}$$

$$i_{C1}(t) = -2\ k_s\ \Delta d_S\ i_o(t) \tag{9}$$

Where k_S is 1 for $i_o > 0$ and -1 for $i_o > 0$. The expression that connect the currents $i_{C1}(t)$ and $i_{C2}(t)$ with the capacitors voltage are represented by the expression (10). Substituting (10), and applying the Laplace transform in the equations (8) and (9), it is possible to evaluate the relation between the capacitor voltage and the duty cycle variation Δd_S. The transfer functions that represent the capacitor voltages balancing behavior are represented by the equation (11).

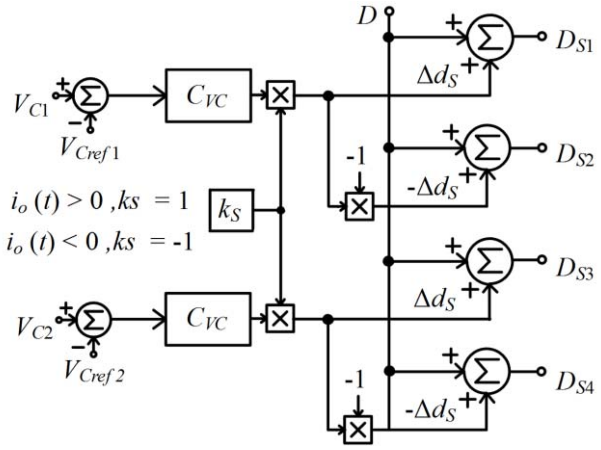

Fig. 3. Control diagram for the proposed method to balance the flying capacitor's voltage

The expression (11) has a positive sign for C_1 analytical voltage model and negative sing for C_2. The output current peak is expressed by I_P. The flying capacitors voltage balance analytical model, can be simplify inserting the flag k_S in the control block, as show in the Figure 3. With this variable is possible to use just one equation for the control project. In this way, the capacitor voltage behavior is expressed by (12).

$$i_{Cx}(t) = C_x \frac{dV_{Cx}}{dt} \tag{10}$$

$$\frac{V_{C1,2}(s)}{\Delta d_S(s)} = \pm k_s \frac{2\,I_P}{s\,C_1} \tag{11}$$

$$Gvc(s) = \frac{2\,I_P}{s\,C_{1,2}} \tag{12}$$

D. Digital Control Project

After defining the control strategy and the capacitor's voltage model, it is necessary to design the controller. In this application, the implemented controller is a digital one using a TMS28335 from Texas Instruments. The full digital control diagram blocks for the flying capacitor's voltage controller is shown in Figure 4. Table II presents the parameters used to design the digital controller for the flying capacitor's voltage balance.

Converting the transfer function s to w plane and multiplying the expression by the gain of the sensor, the gain of the filters and the digital delays arrives in the expression (13), where $k = H_{CV}\ K_{FLP}\ K_{ADC}$.

The w plane control project with bode techniques needs to comply with the following requirements: phase margin between 45° and 120°, steady state zero error, slope of the gain curve must be -20 dB/dec at 0 dB crossing and the frequency at 0 dB crossing must be sufficiently low to keep the system stable. With these preconditions and the parameters shown in Table I, the voltage control is projected. The Figure 5 and Figure 6 present the bode diagram for the

maximum and minimum output power conditions, respectively. The dotted line represents the natural voltage balance behavior (Gvc_w), the controlled balanced voltage is represented by the continuous line (Gc_w) and the controller by the dashed line (Cvc_w).

From the bode frequency analysis, it can be deduced that the natural voltage balance has low gain at low frequency and the frequency at 0 db is very low. The proportional integrative controller (PI), for both cases, is designed for the 0 dB crossing to be at the frequency of 1.0Hz, avoiding instabilities on the system and achieving a good control dynamic. A high frequency pole is added to filter the electromagnetic noise.

With the two controllers designed, is necessary to choose one that has the best response for booth conditions of power load. In this case, the controller for minimum power conditions has the best dynamics to maintain the voltage balance of the flying capacitors. The transfer function of the PI controller is shown in (14).

$$G_{VC}(w) = \frac{2I_P}{C_{1,2}} k \left(\frac{\frac{-wT_a}{2}+1}{w} \right) \left(\frac{\frac{-wT_a}{2}+1}{\frac{wT_a}{2}+1} \right) \quad (13)$$

$$C_{VC}(w) = \frac{2.185w+1.235}{w(w+3777)} \quad (14)$$

IV. SIMULATIONS

To validate and verify the effectiveness of the flying capacitor control, a numerical simulation is used. The main parameters used in the simulations are the same given in Table II. It is used 5 kHz as the switching frequency of the semiconductor, with a modulation index of 0,76. The simulation results are shown just for one capacitor, once the capacitors have independent controllers, but the same behavior.

A. Control Method Validation.

Causing variations in the main variables that are associated with the flying capacitor's voltage balance is necessary to test the control performance.

First, a voltage step is applied to the flying capacitor's voltage to check the dynamics of the controller. Figure 7 shows the controller signal and the voltage results for the maximum power load condition, when a voltage step of 15 V on the flying capacitor C_1 occurs at time t = 1. 48 s. The results show that the controller has good dynamic, balancing the voltage efficiently. The controller signal shows the function of the control variable k_S, changing the sign of the controller to maintain the capacitor charge process. Figure 8 presents the output voltage and the output current after the control balances the flying capacitor's voltage. The results show that the controller maintains the quality of the output voltage and the proper functioning of the converter.

TABLE II
Parameters to design the controller of the flying capacitor's voltage.

Parameter	Value	Description
V_{CC} (V)	400	dc Link Voltage
Ip_min (A)	11.0	Minimum Output Current Peak
Ip_max (A)	19.3	Maximum Output Current Peak
$C_{1,2}$ (µF)	1410	Flying Capacitor
H_{CV}	0.01	Voltage Sensor Gain
K_{FLP}	67.0	Low-Pass Filter Gain
K_{ADC}	1365	AD Converter Gain
T_a (µs)	50.0	Sample Time

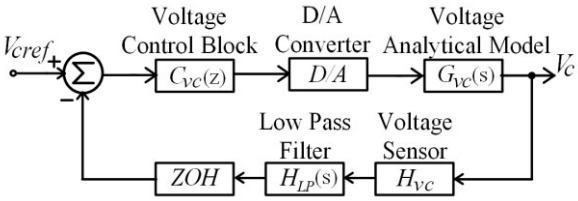

Fig. 4. Digital control diagram that is used to design the controller.

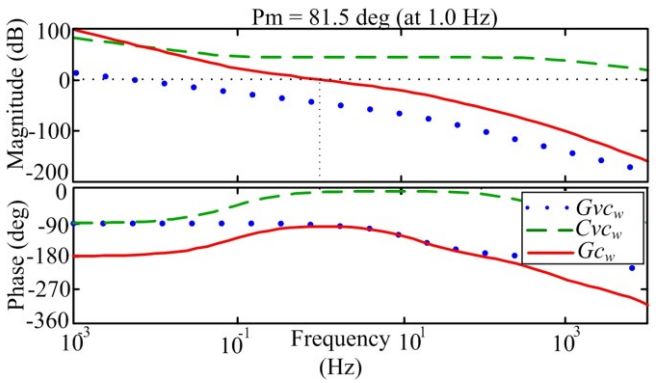

Fig. 5. Bode diagram with the frequency response of the natural capacitor's voltage (Gvc_w), the controller (Cvc_w) and the balanced controlled voltage (Gc_w) with maximum output power.

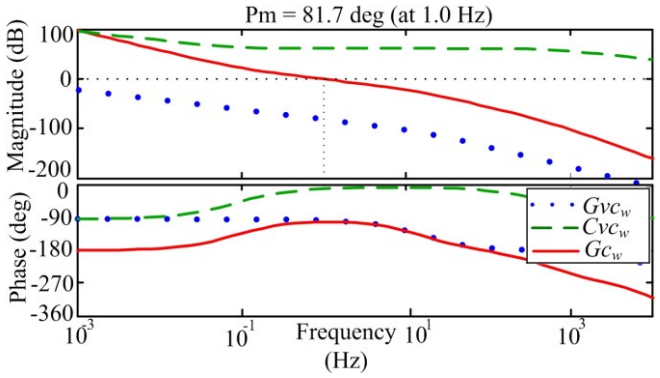

Fig. 6. Bode diagram with the frequency response of the natural capacitor's voltage (Gvc_w), the controller (Cvc_w) and the balanced controlled voltage (Gc_w) with minimum output power.

Figure 9 show the control behavior without the k_S flag when the same voltage step of 15 V occurs at time t = 1. 48 s. It is visible that the control is less efficient, more unstable and the capacitor's voltage take more time to reach the set point, if compared with the proposed control method.

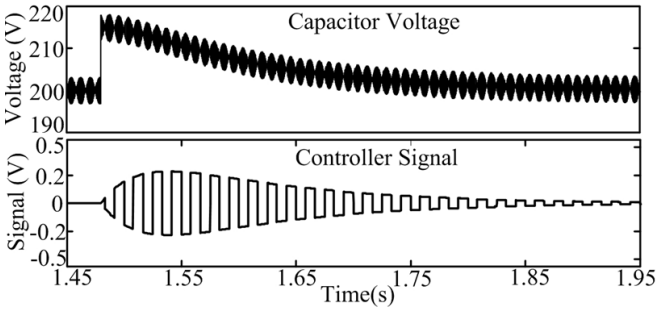

Fig. 7. Flying Capacitor's voltage and control signal under the presents control method when a voltage step of 15V on the capacitor occurs at t = 1, 48 s, for maximum power load condition.

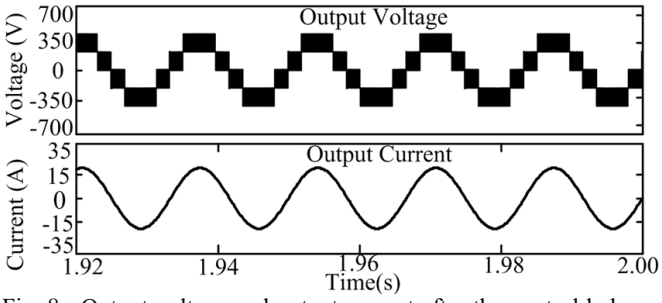

Fig. 8. Output voltage and output current after the control balance the flying capacitor's voltage when a voltage step of 15V on the capacitor occurs at t = 1, 48 s, for maximum power load condition.

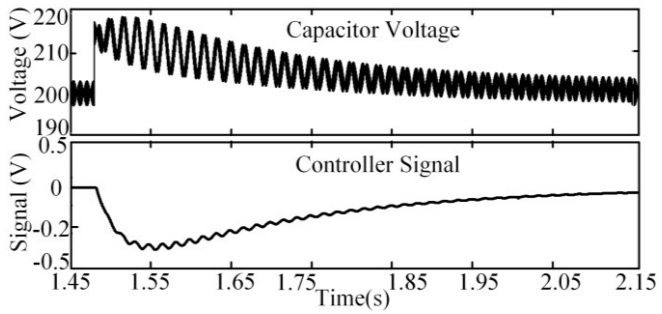

Fig. 9. Flying Capacitor's voltage and control signal under the presents control without the variable k_S when the same voltage step of 15V on the capacitor occurs at t = 1, 48 s, for maximum power load condition.

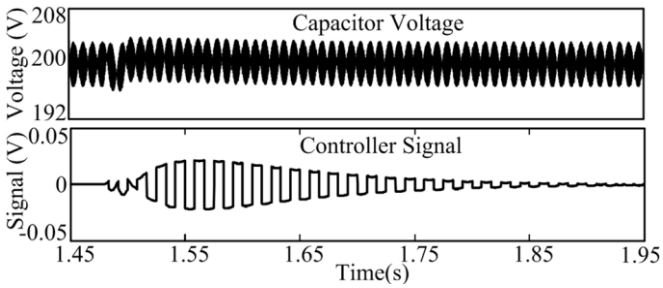

Fig. 10. Flying Capacitor's voltage and control signal when a signal is inserted to generate a difference between the duty cycles of the two adjacent switches at t = 1, 48 s.

On the second test, a signal is inserted to generate a difference between the duty cycles of the two adjacent switches to simulate a non-linear real condition. At time t = 1. 48 s, a disturb signal is introduced in the switches command. The control quickly responds, balancing the capacitor's voltage as shown in Figure 10.

V. EXPERIMENTAL RESULTS

To verify the performance of the present voltage balance control method, a prototype of a single-phase three-level Flying Capacitor inverter was implemented. Figure 11 show the test setup.

The TMS28335 from Texas Instruments is used for the digital control implementation. The Table III show the test parameters. The experimental results are shown just for the flying capacitor of one FC-FC leg, once the capacitors have independent controllers.

The test executed to validate the control method is presented in the Figure 12. It consists in several steps on the flying capacitor voltage reference to check the efficiency of the control method. The voltage reference chance between 35V to 45V, 45V to 50V, 50V to 40V and 40V to 50V. When the reference is increased, the control charge the flying capacitor reaching the set point voltage. The control show a good dynamic, either in the situation when the reference voltage is decreased.

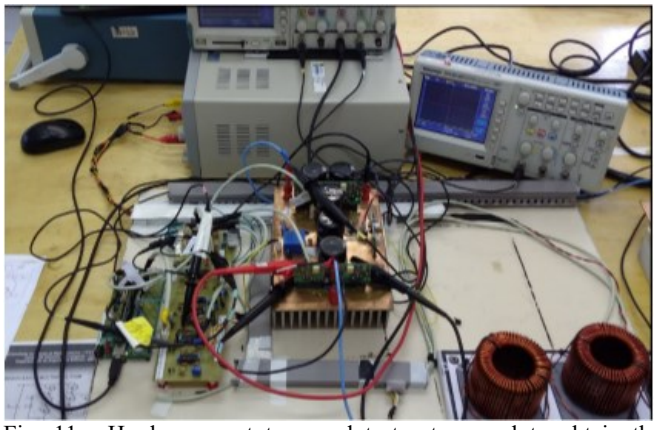

Fig. 11. Hardware prototype and test setup used to obtain the experimental results.

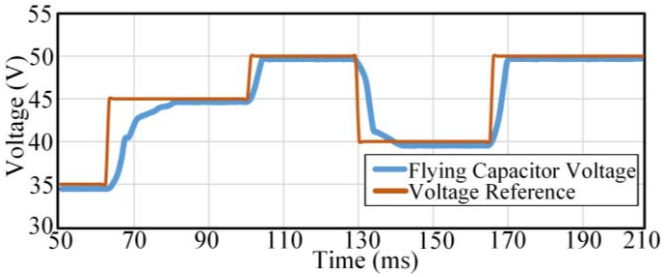

Fig. 12. Experimental results presents the control response for different steps voltages on the flying capacitor voltage reference.

TABLE III
Parameters used in the experimental results.

Parameter	Value	Description
V_{CC} (V)	100	dc Link Voltage
$C_{1,2}$ (μF)	1410	Flying Capacitor
R_{LOAD} (Ω)	45	Load Resistance
L_{LOAD} (mH)	1.0	Load Inductance
F_S (kHz)	5.0	Switching Frequency
m_a	0.76	Modulation Index

VI. CONCLUSIONS

This paper presents a voltage balancing technique for an n-level FC-FC inverter operating with Phase shift modulation. An easy analytical model of the capacitor's voltage is introduced, simplifying the control design.

The proportional integrative controller (PI) is used to modify the duty cycle of the switches, maintaining the voltage balance on the flying capacitors. Besides that, the variable k_S is inserted into the control blocks to identify the direction of the output current, improving the efficiency of the controller.

The simulation and experimental results show that the technique is efficient and the method can regulate the flying capacitor's voltage, maintaining the voltage equal to the reference signal.

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