A ZVS PWM Inverter With Active Voltage Clamping Using the Reverse Recovery Energy of the Diodes

Marcello Mezaroba, Denizar Cruz Martins, and Ivo Barbi

***Abstract*—This paper presents a zero-voltage-switching (ZVS) pulsewidth modulated inverter with active voltage clamping using only a single auxiliary switch. The structure is particularly simple and robust. It is very attractive for single-phase high-power applications. Switching losses are reduced due to implementation of the simple active snubber circuit that provides ZVS conditions for all switches, including the auxiliary one. Its main features are: simple modulation strategy, robustness, low weight and volume, low harmonic distortion of the output current and high efficiency. The principle of operation for steady-state conditions, mathematical analysis and experimental results from a laboratory prototype are presented.**

***Index Terms*—Active clamping, inverters, soft commutation.**

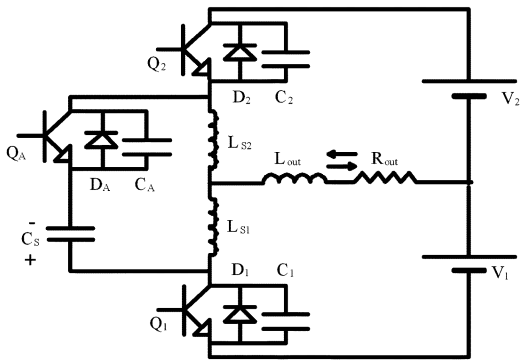

Fig. 1. Proposed circuit.

I. Introduction

MUCH effort has been exerted by researchers all over the world in an attempt to reduce harmonic distortion and audible noise in the output of inverters. Their objectives have been attained through an increase in inverter commutation frequencies and an appropriate modulation strategy. These measures have provided some benefits, such as a reduction in the weight and volume of the magnetic elements. However, they have caused some difficulties due to the high commutation losses in the switches and the appearance of electromagnetic interference. These factors occur mainly in inverter topologies that use the bridge inverter configuration. At the moment that the main switch turns on, the anti-parallel diode of the bridge complementary switch begins its reverse recovery phase. During this stage, the switches are submitted to a high current ramp rate (di/dt) and a high peak-reverse recovery current i_r. Both contribute significantly to increasing the commutation losses and produce electromagnetic interference.

To solve this problem, diverse works have been developed by the scientific community in recent years and can be divided into two groups: passive techniques and active techniques. The passive techniques are characterized by the absence of controlled switches in the switching aid circuit, while the active techniques are characterized by circuits that use controlled switches. Among the passive solutions, perhaps the most widely known is the Undeland snubber [1]. This snubber provides good performance in the majority of its applications, but is not capable of regenerating the energy lost in switching. To try to minimize these losses, some works have considered modifications to the Undeland snubber, aiming at the regeneration of the energy lost in switching [2]–[4] and [5]. The active solutions are already distinguished by the use of controlled switches to obtain soft commutation. The main ones are those that use conventional pulsewidth modulation (PWM), without the need for special control circuits. One of these works is the auxiliary resonant auxiliary resonant diode pole inverter (ARDPI) [6]. This topology matches the use of PWM modulation, with the soft switching attained through a relatively simple circuit. On the other hand, it needs a high current circulating in the circuit, about 2.5 times the load current, raising the current stress in the switches. A topology very similar to the previous one is the auxiliary resonant pole inverter (ARPI) [7]. Theoretically, this circuit reduces the current levels necessary for switching, but it involves a complex control strategy. Another circuit found in literature is the auxiliary resonant commutated pole inverter (ARCPI) [8], [9], and [10]. This inverter has auxiliary switches that are only turned on when the load current is not sufficient to effect the soft switching, causing the control circuit to become very complex and dependent on the sensors.

Recently, some research was carried out using the reverse recovery energy from the diodes to obtain soft commutation in the switches of the pre-regulated rectifiers with high power factor [11] and [12].

In this paper, a zero-voltage-switching (ZVS) PWM inverter with voltage clamping across the switches, using only a single auxiliary switch, is presented. The proposed structure uses the diode reverse recovery energy technique to obtain soft commutation in all switches, such as the rectifier shown in [12].

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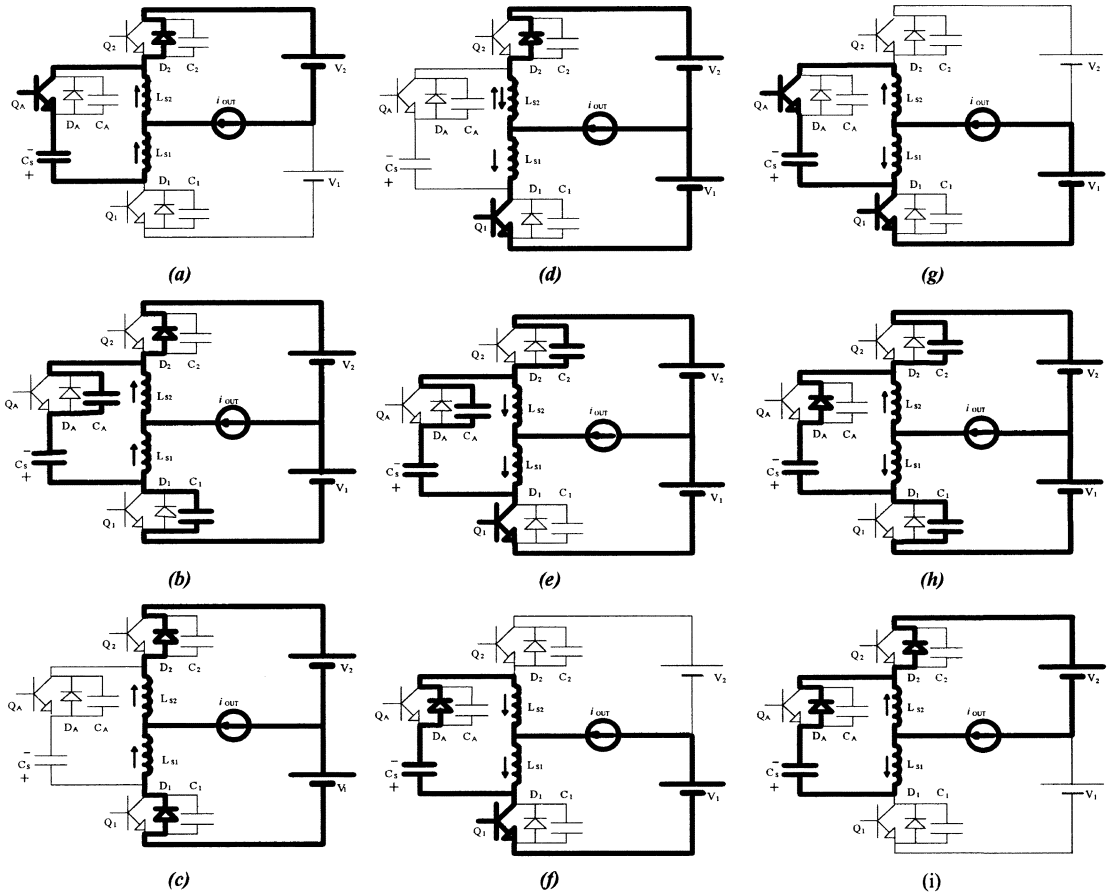

Fig. 2. Operation stages. (a) First state (t0-t1). (b) (b) Second stage (t1-t2). (c) Third stage (t2-t3). (d) Fourth stage (t3-t4). (e) Fifth stage (t4-t5). (f) Sixth stage (t5-t6). (g) Seventh stage (t6-t7). (h) Eighth stage (t7-t8). (i) Ninth stage (t8-t0).

II. Proposed Circuit

The proposed circuit is shown in Fig. 1. It presents a half-bridge inverter configuration, where Q_1, Q_2 are the main switches. The snubber circuit is formed by one switch Q_A, one small center-tapped inductor L_{S1}, L_{S2} and one capacitor C_S. C_1, C_2, and C_A are the commutation capacitors. Capacitor C_S is responsible for the storage of the diode reverse recovery energy and for the clamping of the voltage across the switches. Inductors L_{S1} and L_{S2} are responsible for the control of the di/dt during the diode reverse recovery time.

III. Operation Stages (for First Half-Cycle)

To simplify the analysis, the following assumptions are made: the circuit operates in steady state; the components are considered ideal; the voltage across capacitor C_S and the current through the output inductor $L_{\rm OUT}$ are considered constant during the switching period.

In the following paragraphs, the operation stage (Fig. 2) of the first positive half-cycle of the output current is described in detail.

First Stage (t0–t1): At t0, switch Q_A is turned on. During this interval, the output current, $i_{\rm OUT}$, is delivering energy to source V_2 via diode D_2. At the same time, additional current iL_{S1} circulates through the mesh, formed by L_{S2}, Q_A, C_S, and L_{S1}. At the end of this stage, the current through inductor L_{S1} reaches its maximum value, i_f (Fig. 3)

$$vC_1(t) = E + vC_S \tag{1}$$

$$vC_2(t) = 0 \tag{2}$$

$$vC_A(t) = 0 \tag{3}$$

$$iL_{S1}(t) = \frac{vC_S}{L_S} \cdot t \tag{4}$$

$$iL_{S2}(t) = iL_{S1}(t) + i_{\rm OUT}. \tag{5}$$

This stage was chosen to initiate the converter analysis because it precedes the commutation process of the main switch, Q_1, during the half-cycle of operation. At time t0 current iL_{S1} becomes positive and increases linearly. At the end of the first stage this current is responsible for the soft commutation process of Q_1.

Second Stage (t1-t2): This stage starts when auxiliary switch Q_A is blocked. Current iL_{S1} charges capacitor C_A from *zero* to $E + vC_S$, and discharges C_1 from $E + vC_S$ to *zero*. $E = V_1 + V_2$. During this stage the current, iQ_1, circulates through the intrinsic capacitor of switch Q_1

$$vC_1(t) = (E + vC_s) - \frac{i_f}{2 \cdot C_1} \cdot t \tag{6}$$

where i_f is the maximum current through L_{S1}. Thus

$$i_f = iL_{S1}(t_1) \tag{7}$$

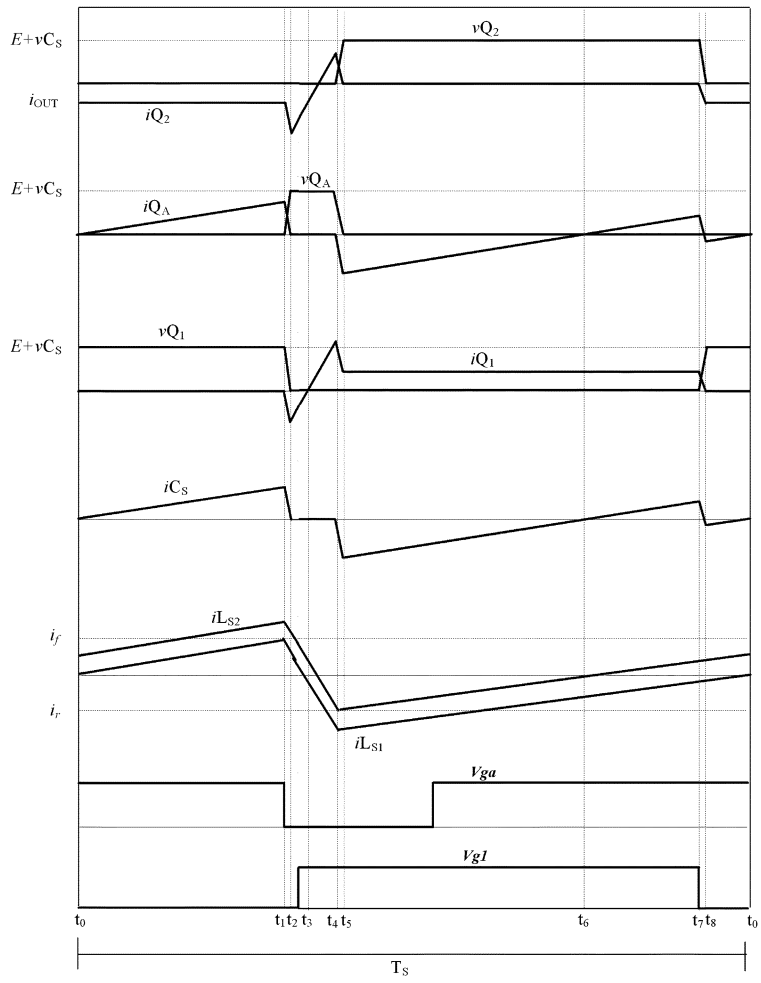

Fig. 3. Main waveforms.

$$vC_2(t) = 0 \tag{8}$$

$$vC_A(t) = \frac{i_f}{2 \cdot C_A} \cdot t \tag{9}$$

$$iL_{S2}(t) = i_f + i_{\mathrm{OUT}}. \tag{10}$$

Third Stage (t2-t3): At t2, the voltage across C_1 reaches *zero* and is clamped by diode D_1. At this moment, the voltage $E = V_1 + V_2$ is applied across inductors L_{S1} and L_{S2} and currents iL_{S1} and iL_{S2} decrease linearly. In this stage, switch Q_1 must be turned on

$$vC_1(t) = 0 \tag{11}$$

$$vC_2(t) = 0 \tag{12}$$

$$vC_a(t) = E + vC_S \tag{13}$$

$$iL_{S1}(t) = i_f - \frac{E}{L_S} \cdot t \tag{14}$$

where $L_S = L_{S1} + L_{S2}$.

$$iL_{S2}(t) = iL_{S1}(t) + i_{\mathrm{OUT}}. \tag{15}$$

Fourth Stage (t3-t4): This stage begins when current iL_{S1} inverts its direction and flows through switch Q_1. The turn-on occurs at zero voltage. Current iL_{S2} continues to decrease until inverting its direction, which begins the reverse recovery phase of diode D_2. The auxiliary inductors limit the reverse recovery di/dt

$$vC_1(t) = 0 \tag{16}$$

$$vC_2(t) = 0 \tag{17}$$

$$vC_a(t) = E + vC_S \tag{18}$$

$$iL_{S1}(t) = -\frac{E}{L_S} \cdot t \tag{19}$$

$$iL_{S2}(t) = i_{\mathrm{OUT}}(t) + i_{L1}(t). \tag{20}$$

Fifth Stage (t4-t5): This stage starts when diode D_2 stops conducting. Current iL_{S2} begins charging capacitor C_2 from *zero* to $E + vC_S$ and discharging C_A from $E + vC_S$ to *zero*

$$vC_1(t) = 0 \tag{21}$$

$$vC_2(t) = \frac{i_r}{2 \cdot C_2} \cdot t \tag{22}$$

where i_r is the maximum negative current through L_{S2}. So, $i_r = iL_{S2}(t_4)$

$$vC_A(t) = (E + vC_S) - \frac{i_r}{2 \cdot C_A} \cdot t \tag{23}$$

$$iL_{S1}(t) = -i_{\mathrm{OUT}} - i_r \tag{24}$$

$$i_{Ls2}(t) = -i_r. \tag{25}$$

Sixth Stage (t5-t6): At t5, the voltage across capacitor C_A reaches *zero* and is clamped by diode D_A. Currents iL_{S1} and iL_{S2} increase, due to the application of voltage vC_S across inductors L_{S1} and L_{S2}. In this stage, switch Q_A must be turned on. It is important to emphasize that the drive time of switch Q_A is estimated previously and kept constant during the entire inverter operation range. So, the use of current sensor is not necessary

$$vC_1(t) = 0 \tag{26}$$
$$vC_2(t) = E + vC_S \tag{27}$$
$$vC_A(t) = 0 \tag{28}$$
$$iL_{S1}(t) = -i_{\mathrm{OUT}} + iL_{S2}(t) \tag{29}$$
$$iL_{S2}(t) = \frac{vC_S}{L_S} \cdot t - i_r. \tag{30}$$

Seventh Stage (t6-t7): This stage begins when current iL_{S2} changes its direction and flows through switch Q_A. Current iL_{S1} continues to increase linearly

$$vC_1(t) = 0 \tag{31}$$
$$vC_2(t) = E + vC_S \tag{32}$$
$$vC_A(t) = 0 \tag{33}$$
$$iL_{S1}(t) = \frac{vC_S}{L_S} \cdot t - i_{\mathrm{OUT}} \tag{34}$$
$$iL_{S2}(t) = \frac{vC_S}{L_S} \cdot t. \tag{35}$$

Eighth Stage (t7-t8): During this stage, switch Q_1 is blocked and the current through C_S inverts its direction and flows through diode D_A. Capacitor C_1 charges itself from *zero* to $E + vC_S$ and capacitor C_2 discharges from $E + vC_S$ to *zero*

$$vC_1(t) = \frac{i_{\mathrm{OUT}}}{2 \cdot C_1} \cdot t \tag{36}$$
$$vC_2(t) = (E + vC_S) - \frac{i_{\mathrm{OUT}}}{2 \cdot C_2} \cdot t \tag{37}$$
$$vC_A(t) = 0 \tag{38}$$
$$iL_{S1}(t) = \frac{vC_S}{L_S} \cdot \Delta t_7 - i_{\mathrm{OUT}} \tag{39}$$
$$iL_{S2}(t) = \frac{vC_S}{L_S} \cdot \Delta t_7 \tag{40}$$
$$\Delta t_7 = D \cdot Ts - \frac{i_r \cdot L_s}{vC_S}. \tag{41}$$

Ninth Stage (t8-t0): This stage begins when the voltage across capacitor C_2 reaches *zero* and is clamped by diode D_2. Current iL_{S1} continues to increase. This stage finishes when iL_{S1} inverts its direction and flows through auxiliary switch Q_A, restarting the first operation stage

$$vC_1(t) = E + vC_S \tag{42}$$
$$vC_2(t) = 0 \tag{43}$$
$$vC_A(t) = 0 \tag{44}$$
$$iL_{S1}(t) = \frac{vC_S}{L_S} \cdot t + \frac{vC_S}{L_S} \cdot \Delta t_7 - i_{\mathrm{OUT}} \tag{45}$$
$$iL_{S2}(t) = \frac{vC_S}{L_S} \cdot t + \frac{vC_S}{L_S} \cdot \Delta t_7. \tag{46}$$

For the second half-cycle, the operation stage is analogous and can be described in an identical way.

The main operation stages are shown in Fig. 2. Fig. 3 shows the main waveforms.

IV. Mathematical Analysis of Commutation

To guarantee the ZVS conditions, it is necessary, in the second stage, that the stored energy in inductor $L_S = L_{S1} + L_{S2}$ be sufficient to discharge capacitor C_1 and to charge C_A. Thus, by inspection of Fig. 3 (Interval t1–t2), the following condition can be formulated:

$$L_S \cdot i_f^2 \geq (C_A + C_1)(E + vC_S)^2 \tag{47}$$

where i_f is the maximum current in L_{S1} and vC_S is maintained constant during the switching period. The current i_f must be sufficient to promote the charge and discharge of the commutation capacitors.

Assuming that $vC_S \ll E$, we have

$$i_{f\,\min} \geq E\sqrt{\frac{C_1 + C_A}{L_S}}. \tag{48}$$

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor C_S.

In steady-state conditions, the clamping capacitor average current must be *zero*. Thus

$$iC_{\mathrm{Sav}} = \frac{1}{T_S}\left[\int_{t_5}^{t_7}\left(\frac{vC_S}{LS}t - i_r\right)dt + \int_{t_7}^{\mathrm{Ts}}\left(\frac{vC_S}{LS}\,t - i_{\mathrm{OUT}} - i_r\right)dt\right] \tag{49}$$

where Ts is the switching period.

In relation to the switching period, the commutation time is very short. Therefore, the following simplifications can be made:

$$t_5 \approx t_1 = 0 \tag{50}$$
$$t_7 - t_5 = D \cdot T_S \Rightarrow t_7 = D \cdot T_S. \tag{51}$$

From (50) and (51), (49) can be re-written as follows:

$$iC_{\mathrm{Sav}} = \frac{1}{T_S}\left[\int_{0}^{D\cdot T_S}\left(\frac{vC_S}{L_S}\,t - i_r\right)dt + \int_{D\cdot T_S}^{T_S}\left(\frac{vC_S}{L_S}\,t - i_{\mathrm{OUT}} - i_r\right)dt\right]. \tag{52}$$

Solving the integral equation, and considering

$$iC_{\mathrm{Sav}} = 0 \tag{53}$$

we have

$$vC_S = \frac{2 \cdot L_S}{T_S}[i_r + i_{\mathrm{OUT}}(1 - D)]. \tag{54}$$

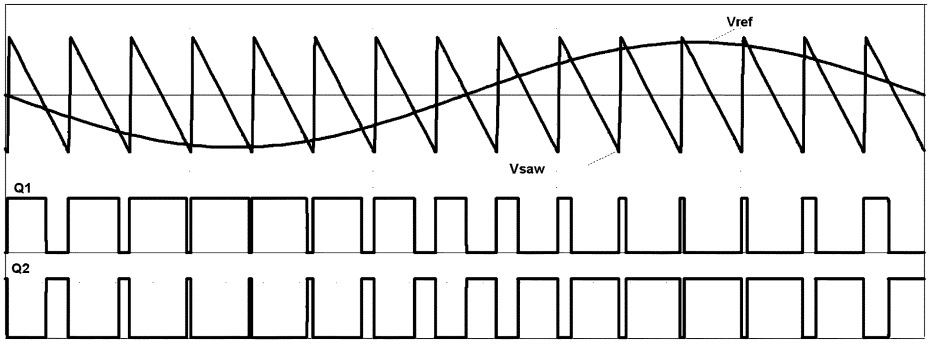

Fig. 4. Modulation strategy.

Considering that the load current is a sinusoidal function and is in phase with the output voltage, then

$$i_{\mathrm{OUT}}(\omega t) = \frac{E \cdot ma}{2 \cdot Z_{\mathrm{OUT}}} \cdot \sin \omega t \tag{55}$$

where Z_{OUT} is the load impedance.

Fig. 4 shows some signals of the modulation strategy used to drive the main switches.

The sawtooth waveform is lined on the left edge. This facilitates the synchronism between the auxiliary switch and the main switches.

The converter output voltage is controlled by the amplitude modulation factor (ma), which is obtained through the relation between the peak value of the sinusoidal reference signal and the peak value of the sawtooth waveform

$$ma = \frac{v_{\mathrm{ref}}\, pk}{V_{\mathrm{SAW}\, pk}}. \tag{56}$$

The inverter output voltage for a switching period can be expressed by

$$v_{\mathrm{OUT}} = E\left(D - \frac{1}{2}\right). \tag{57}$$

From (57) we can obtain the duty cycle D, that is

$$D = \frac{v_{\mathrm{OUT}}}{E} + \frac{1}{2}. \tag{58}$$

The inverter output voltage for an output period is given by

$$v_{\mathrm{OUT}}(\omega t) = \sqrt{2} \cdot v_{\mathrm{OUT_{rms}}} \cdot \sin \omega t \tag{59}$$

where ω is expressed by

$$\omega = 2 \cdot \pi \cdot f. \tag{60}$$

f—Output Frequency

The maximum output voltage is given by

$$v_{\mathrm{OUT}_{pk}} = \frac{E \cdot ma}{2}. \tag{61}$$

The RMS output voltage is obtained from

$$v_{\mathrm{OUT_{rms}}} = \frac{E \cdot ma}{2 \cdot \sqrt{2}}. \tag{62}$$

Equation (63) shows the inverter duty cycle obtained from (58), (59), and (62)

$$D(\omega t) = \frac{ma}{2} \cdot \sin \omega t + \frac{1}{2}. \tag{63}$$

Combining (54), (55), and (63), we obtain the expression of the snubber capacitor voltage, vC_S, given by

$$vC_S(\omega t) = \frac{2 \cdot L_S}{T_S}\left[i_r + \frac{E \cdot ma}{4 \cdot Z_{\mathrm{OUT}}} + \sin \omega t - \frac{E \cdot ma^2}{4 \cdot Z_{\mathrm{OUT}}} \cdot \sin^2 \omega t\right] \tag{64}$$

where i_r is the peak reverse recovery current of the anti-parallel diode, which can be given by [16]

$$i_r = \sqrt{\frac{4}{3} \cdot Q_{\mathrm{rr}} \cdot \frac{E}{L_s}}. \tag{65}$$

Q_{rr} represents the reverse recovery charge of the diode.

From the analysis of the current behavior in capacitor C_S, the expression of current i_f can be obtained

$$i_f(\omega t) = \frac{vC_s(\omega t)}{L_s} \cdot T_s - i_{\mathrm{OUT}}(\omega t) - i. \tag{66}$$

Combining (64) with (66), and making some simplifications, we obtain the expression that represents the evolution of current i_f

$$i_f(\omega t) = i_r - \frac{E \cdot ma^2}{2 \cdot Z_{\mathrm{OUT}}} \cdot \sin^2 \omega t. \tag{67}$$

To guarantee the ZVS condition in all load ranges, the minimum value of current i_f obtained from (67) must be greater than the value obtained from (48).

V. Design Example

A. Input Data

$E = 400$ V	bus voltage;
$V_{\mathrm{OUT}} = 127$ V	RMS output voltage;
$\mathrm{P_{OUT}} = 1000$ VA	output power;
$i_{\mathrm{OUT}} = 7.88$ A	output current;
fs = 20 kHz	switching frequency;
f = 60 Hz	output frequency;
$L_{\mathrm{OUT}} = 2.5$ mH	load inductance;
$\mathrm{R_{OUT}} = 16\ \Omega$	load resistance;
$ma = 0.9$	modulation factor.

B. Calculation of the Auxiliary Inductors

The auxiliary inductors are responsible for the di/dt limit during the turn-off of the main diodes. The di/dt is directly related to the peak reverse recovery current i_r of the anti-parallel diodes. A "snappy" di/dt produces a large amplitude transient voltage and contributes significantly to electromagnetic interference.

In the design procedure, a di/dt that is usually found in the diode datasheet was chosen. This is a simple way to obtain the diode's fundamental parameter for the design of the inverter. In this case, the di/dt chosen for the example was 40 A/μs. We know that the current ramp rate is determined by the external circuit, thus

$$L_s = \frac{E}{di/dt} = \frac{400\ \text{V}}{40\ \text{A}/\mu\text{s}} = 10\ \mu\text{H}. \tag{68}$$

The auxiliary inductors are given by

$$L_{S1} = L_{S2} = \frac{L_S}{2} = 5\ \mu\text{H}. \tag{69}$$

C. Load Impedance

The load impedance is obtained from

$$Z_{\text{OUT}} = \sqrt{16\ \Omega^2 + (2 \cdot \pi \cdot 60\ \text{Hz} \cdot 2.5\ \text{mH})^2} \cong 16\ \Omega. \tag{70}$$

D. Diode Choice

For satisfactory performance of the inverter, it is important to choose a slow diode. Therefore, we opted to use the body diode of MOSFET IRFP460, which has the following characteristics:

$V_{\text{dss}} = 500$ V maximum reverse voltage;
$i_S = 20$ A diode average current;
$Q_{\text{rr}} = 5.7\ \mu$C reverse recovery charge.

E. Switching Period

$$T_S = \frac{1}{f_s} = \frac{1}{20\ \text{kHz}} = 50\ \mu\text{s}. \tag{71}$$

F. Reverse Recovery Current

The reverse recovery current is given by (65)

$$i_r = \sqrt{\frac{4}{3} \cdot 5.7\ \mu C \cdot \frac{400\ \text{V}}{10\ \mu\text{H}}} = 17.4\ \text{A}. \tag{72}$$

G. Capacitor Clamping Voltage Behavior

Using (64), the curves described in Fig. 5 are obtained.

For $Z_{\text{out}} = 16\ \Omega$ and $ma = 0.9$, the maximum clamping voltage is 8 V.

We can observe that the voltage increment across the switches is smaller than in a conventional inverter.

H. Behavior of Current i_f

The behavior of current i_f, obtained from (67) and (48), can be seen in Fig. 6.

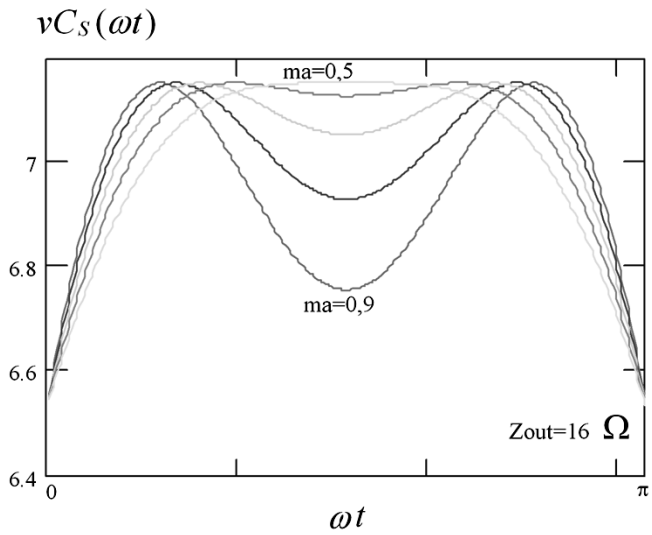

Fig. 5. Capacitor clamping voltage behavior.

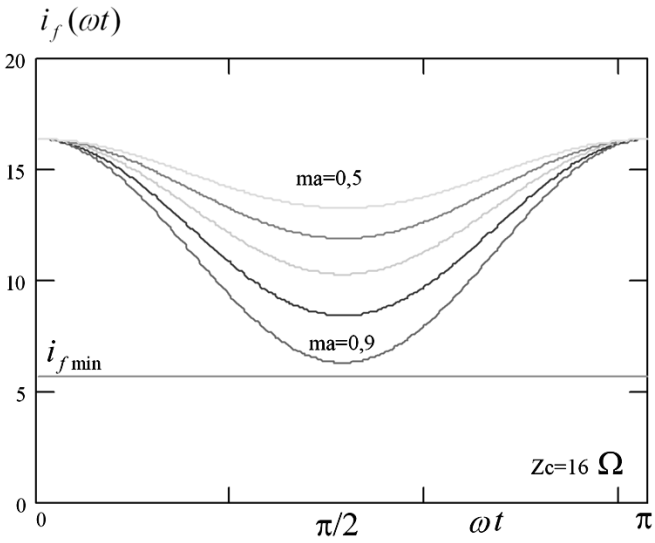

Fig. 6. Current i_f behavior.

It can be seen that current i_f has a minimum point that is located at $\pi/2$, and the intensity of the current diminishes with the increase of the load. To guarantee a ZVS condition in all load ranges, the minimum value of current i_f, obtained from (67), must be greater than the value of the traced straight line from (48).

VI. Experimental Results

An inverter prototype rated 1 kVA, operating with PWM commutation, was built to evaluate the proposed circuit. The main components are given below:

A. Prototype Specifications

Q_1, Q_2, Q_A (IGBT IRG4PC50W);
D_1, D_2, D_A (MOSFET body diode IRFP460);
C_1, C_2, C_A (component's intrinsic capacitance = 8 nF);
L_{S1}, L_{S2} (5uH each; ferrite Core EE30/7; $N = 16$ turns, 13 wires #20 AWG);
C_S (220 uF/35 V; electrolytic capacitor);
L_{OUT} (2.5 mH, output inductor);
R_{out} (16 Ω; output resistor).

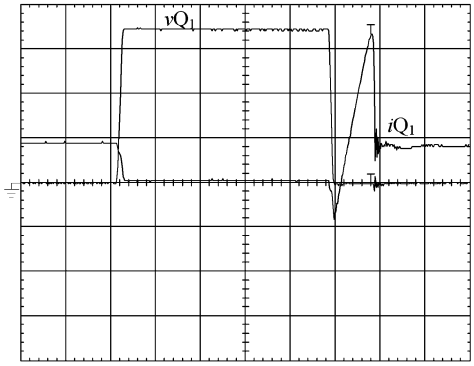

Fig. 7. Voltage and current in Q_1, D_1, C_1. (100 V/div, 5 A/div, 1 us/div).

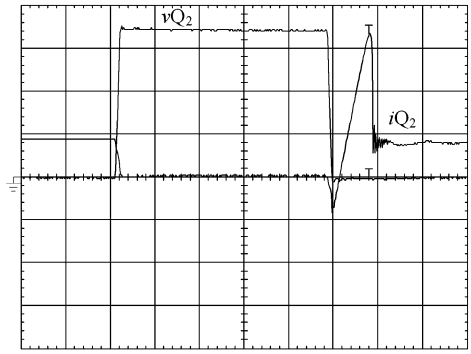

Fig. 8. Voltage and current in Q_2, D_2, C_2. (100 V/div, 5 A/div, 1 us/div).

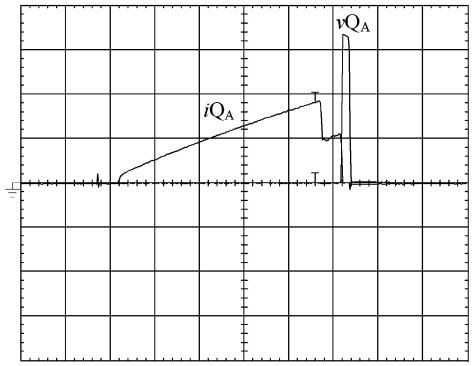

Fig. 9. Voltage and current in Q_A, C_A. (100 V/div, 5 A/div, 1 us/div).

B. Experimental Waveforms

In the figures presented, we can observe the experimental waveforms obtained from the laboratory prototype. Figs. 7–9 show the voltage and current in the switches. We can observe that for all the switches, including the auxiliary one, the commutation occurs under ZVS conditions, confirming the theoretical analysis. In Fig. 10, the current in the commutation auxiliary inductors for a switching period can be observed. A proportionality of values between the currents in both inductors can be observed. The difference between them is the load current.

The voltage across clamping capacitor C_S is shown in Fig. 11. We can note a very low voltage across C_S, which represents a minimal voltage stress across the devices. The output voltage and current are presented in Fig. 12. Fig. 13 shows the efficiency as a function of the load range for both hard and soft commutation. The converter efficiency with soft commutation was improved by approximately 5% for all load ranges.

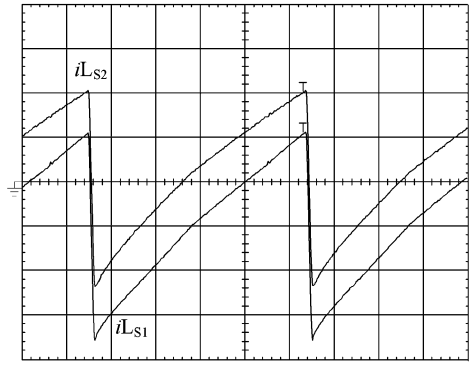

Fig. 10. Current through L_{S1} and L_{S2}. (5 A/div, 10 us/div).

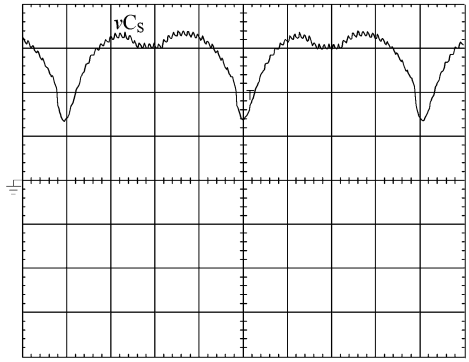

Fig. 11. Voltage in C_S. (2 V/div, 2 ms/div).

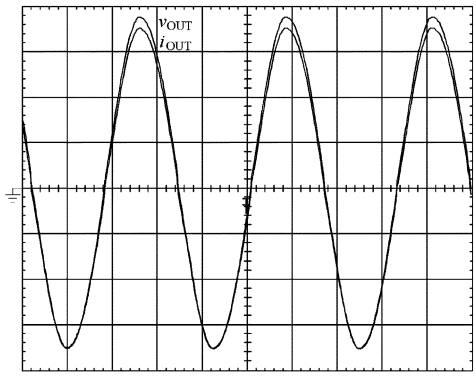

Fig. 12. Output voltage and current. (50 V/div, 5 A/div, 5 ms/div).

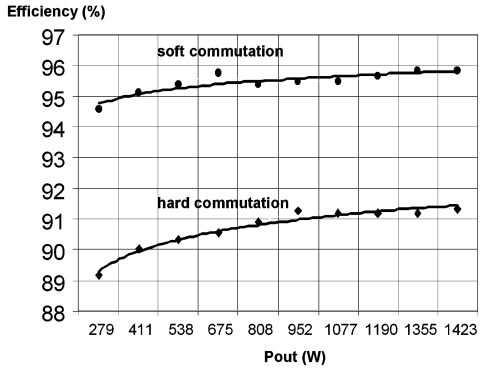

Fig. 13. Efficiency versus the output power.

VII. Conclusion

A ZVS PWM inverter with voltage clamping using a single auxiliary switch has been developed. The operation stages for a

steady-state condition, mathematical analysis, main waveforms and experimental results were presented. The experimental results show low voltage across the clamping capacitor. Switching losses are reduced due to the implementation of a simple active snubber circuit, which provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability and make it suitable for practical applications. The proposed circuit presents soft commutation for all load ranges, confirming the theoretical studies.

This topology presents certain advantages when compared to the conventional soft commutation inverters studied in literature, which are:

- soft commutation in all load ranges;
- simple structure with a low number of components;
- use of a classical PWM modulation;
- auxiliary switch works with a constant duty cycle in all operation stages;
- use of slow and low-cost rectifier diodes;
- low clamping voltage across the capacitor;
- low current stress through the main switches;
- simple design procedure with few restrictions;
- high efficiency.

With these characteristics, the authors believe that the proposed inverter circuit can be very useful for several industrial applications, such as: ac drive systems, power factor correction, UPS, active filters, induction heating etc.

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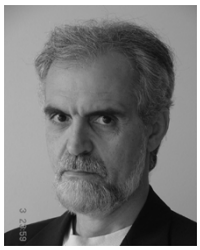

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